



# 3.3V CMOS 18-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

IDT74LVCR16501A

## FEATURES:

- Typical  $t_{sk(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP  
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

## Drive Features for LVCR16501A:

- Balanced Output Drivers:  $\pm 12mA$
- Low switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

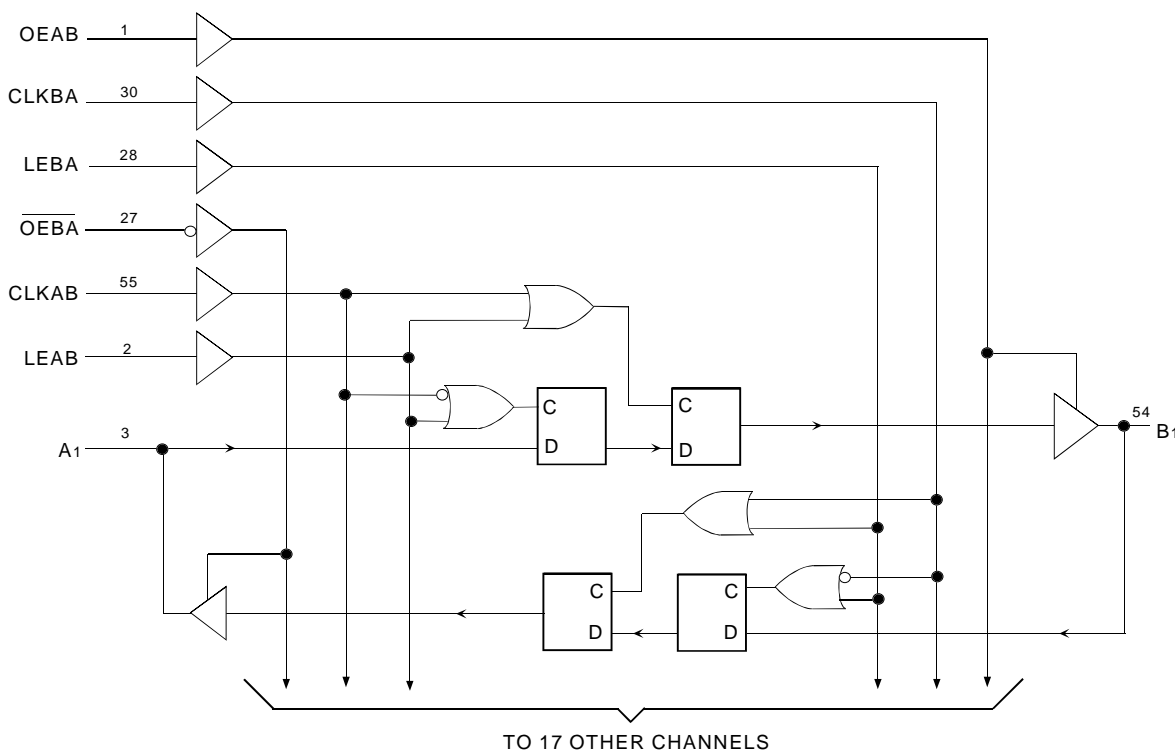
## DESCRIPTION:

The LVCR16501A 18-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power, 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using  $\overline{OEBA}$ , LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The LVCR16501A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive  $\pm 12mA$  at the designated thresholds.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system

## FUNCTIONAL BLOCK DIAGRAM



EXTENDED COMMERCIAL TEMPERATURE RANGE

OCTOBER 1999

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
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SSOP/ TSSOP/ TVSOP  
TOP VIEW

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

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### NOTES:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
			$I_{OH} = -4\text{mA}$	1.9	—	
		$V_{CC} = 2.7\text{V}$	$I_{OH} = -6\text{mA}$	1.7	—	
			$I_{OH} = -4\text{mA}$	2.2	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -8\text{mA}$	2	—	
			$I_{OH} = -6\text{mA}$	2.4	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OL} = 0.1\text{mA}$	—	0.2	V
			$I_{OL} = 4\text{mA}$	—	0.4	
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.55	

## OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$ , $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	$C_L = 0pF$ , $f = 10MHz$		pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled			pF

## SWITCHING CHARACTERISTICS <sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
				Min.	Max.	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Ax to Bx or Bx to Ax	1.5	7	1.5	6	ns
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	8	1.5	7	ns
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	8	1.5	6.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx	1.5	8.2	1.5	7.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx	1.5	8	1.5	7	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	2.5	—	2.5	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	2.5	Clock LOW	2.5	—	ns
			Clock HIGH	2.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	ns
t <sub>w</sub>	LEAB or LEBA Pulse Width HIGH	3	—	3	—	ns
t <sub>w</sub>	CLKAB or CLKBA Pulse Width HIGH or LOW	3	—	3	—	ns
t <sub>sk(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

### NOTES:

- See test circuits and waveforms.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- Skew between any two outputs of the same package and switching in the same direction.

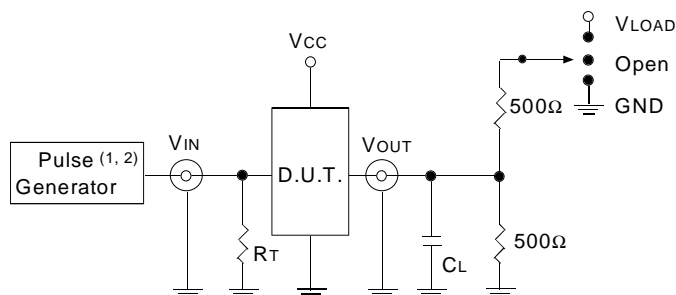
## TEST CIRCUITS AND WAVEFORMS:

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

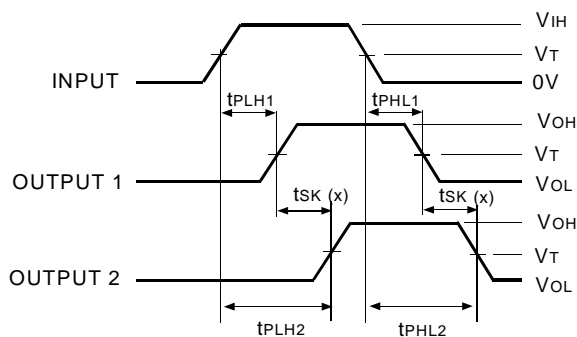
1. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_f \leq 2\text{ns}$ ;  $t_r \leq 2\text{ns}$ .

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other tests	Open

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### OUTPUT SKEW - $t_{SK}(x)$



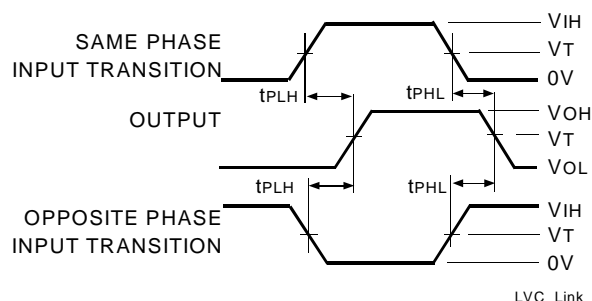
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

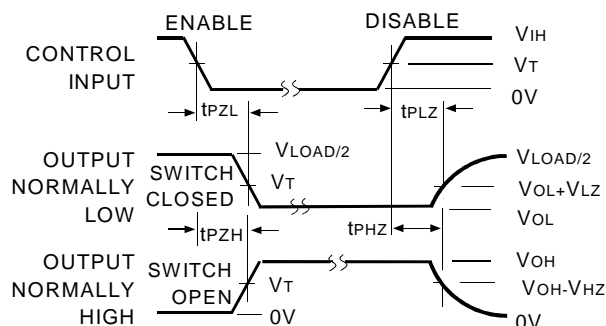
1. For  $t_{SK}(a)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $t_{SK}(b)$  OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

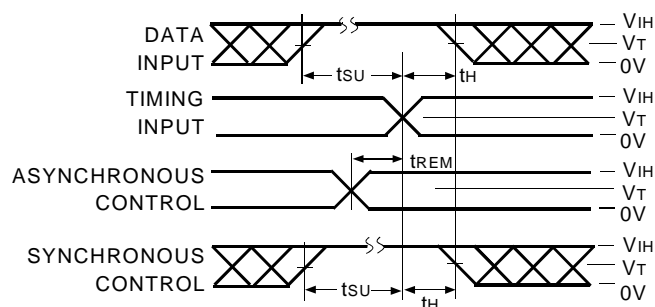


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#### NOTE:

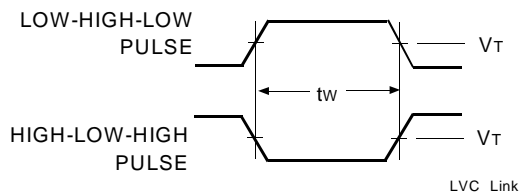
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					501A		18-bit Registered Transceiver with 3 State Outputs
				R16			Double-Density with Resistors, $\pm 12\text{mA}$
				Blank			No Bus-hold
				74			-40°C to +85°C



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