INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8706R

Special General Purpose I/O

Preliminary Specification V0.1

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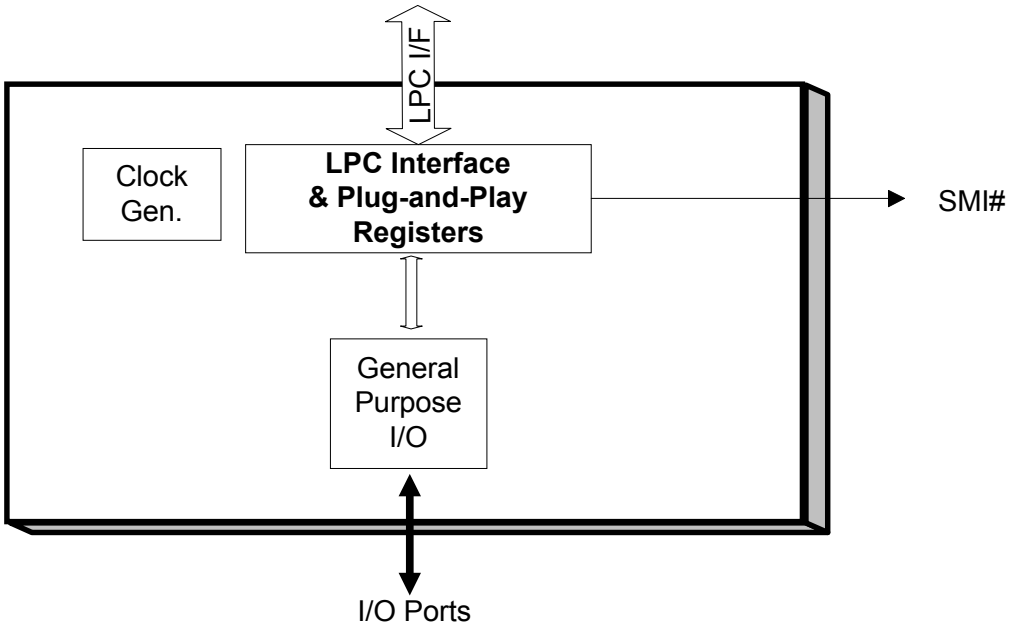
1. Features

- **Low Pin Count Interface**
  - Complies with Intel Low Pin Count Interface Specification Rev. 1.0
- **18 General Purpose I/O Pins**
  - Input mode supports switch de-bounce
  - Simple Input/Output function
- **Single +5V Power Supply**
- **28-pin SOP**

2. General Description

The IT8706R is a Low Pin Count Interface-based General Purpose I/O (GPIO) chip. The IT8706R provides 18 GPIO ports with internal button de-bounced circuits and SMI generation circuit. The device operates with only single +5V power supply. The IT8706R is available in 28-pin SOP package.

3. Block Diagram



4. Pin Configuration

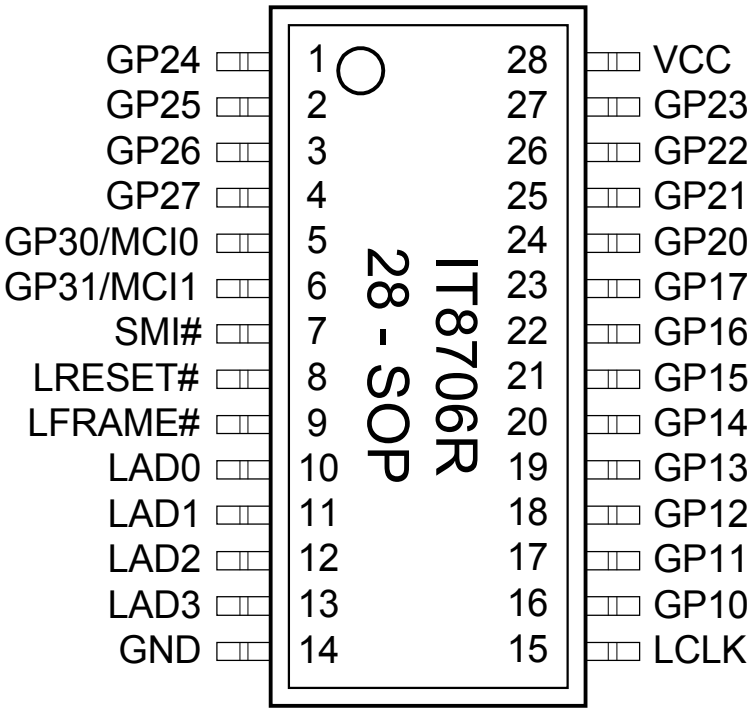


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GP24	8	LRESET#	15	LCLK	22	GP16
2	GP25	9	LFRAME#	16	GP10	23	GP17
3	GP26	10	LAD0	17	GP11	24	GP20
4	GP27	11	LAD1	18	GP12	25	GP21
5	GP30/MCI0	12	LAD2	19	GP13	26	GP22
6	GP31/MCI1	13	LAD3	20	GP14	27	GP23
7	SMI#	14	GND	21	GP15	28	VCC

Table 4-2. Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GND	14	GP16	22	GP25	2	LAD2	12
GP10	16	GP17	23	GP26	3	LAD3	13
GP11	17	GP20	24	GP27	4	LCLK	15
GP12	18	GP21	25	GP30/MCI0	5	LFRAME#	9
GP13	19	GP22	26	GP31/MCI1	6	LRESET#	8
GP14	20	GP23	27	LAD0	10	SMI#	7
GP15	21	GP24	1	LAD1	11	VCC	28

5. IT8706R Pin Descriptions (26 signal pins + 2 VCC/GND)

Table 5-1. Pin Description of LPC Bus Interface

Symbol	Pin(s) No.	Attribute	Description
Supplies			
VCC	**28**	PWR	***+5V Power Supply.***
GND	**14**	GND	***Ground.***
LPC Bus Interface Signals			
LRESET#	**8**	DI	***LPC RESET #***.
LFRAME#	**9**	DI	***LPC Frame #.*** This signal indicates the start of LPC cycle.
LAD[0:3]	**10 – 13**	DIO8	***LPC Address/Data 0 - 3.*** 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
LCLK	**15**	DI	***LPC Clock.*** 33 MHz PCI clock input.
SMI#	**7**	DOD8	***System Management Interrupt #.*** SMI# is an active low output asserted by this chip to inform the system that some active inputs are detected.
GPIO Signals			
GP1[7:0]	**23 – 16**	DIOD8	***General Purpose I/O 1 [7:0].*** Including input detecting and simple I/O functions.
GP2[7:0]	**4 – 1, 27 – 24**	DIOD8	***General Purpose I/O 2 [7:0].*** Including input detecting and simple I/O functions.
GP3[1:0]/ MCI[1:0]	**6 – 5**	DIOD8/DI	***General Purpose I/O 3 [1:0]/MCI[1:0].*** Including input detecting and simple I/O functions. *During LRESET#, these pins are inputs for MCI[1:0] power-on strapping options.*

IO Cell:
DOD8: 8mA Digital Open-Drain Output buffer

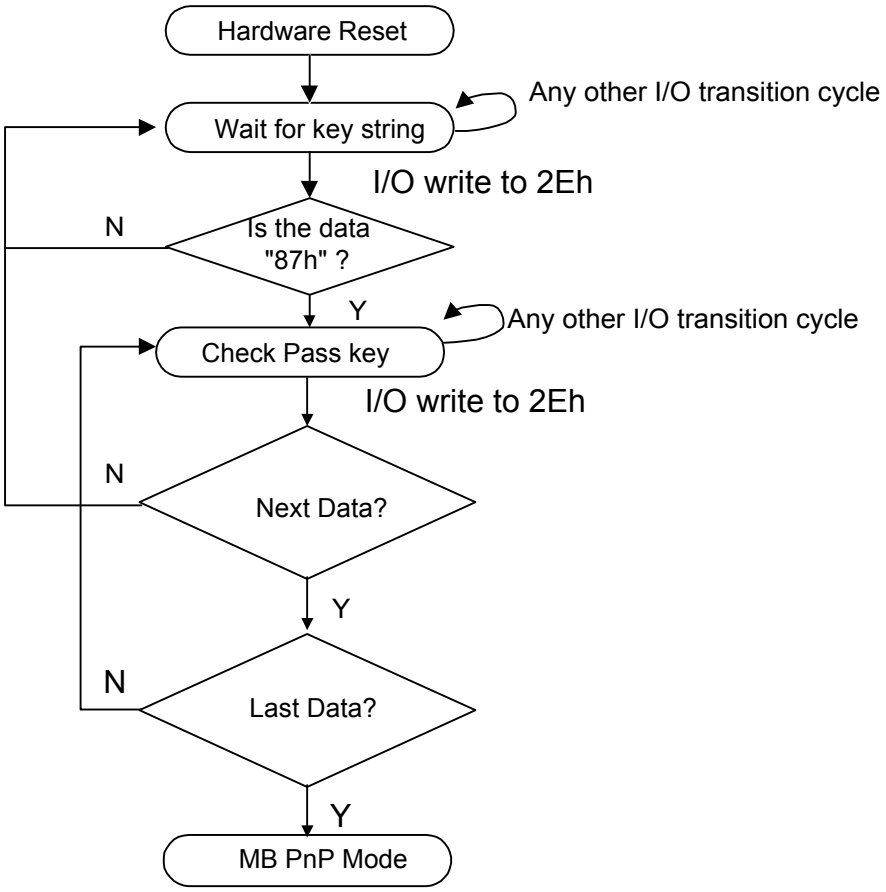
DIO8: 8mA Digital Input/Output buffer
DIOD8: 8mA Digital Open-Drain Input/Output buffer

DI: Digital Input

6. System Configuration

6.1 Overview

After the hardware reset or power-on reset (LRESET#), the IT8706R enters the normal mode.



There are three steps to completing the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

	Address port	Data port
87h, 06h, 55h, 55h;	2Eh	2Fh
or 87h, 06h, 55h, AAh;	4Eh	4Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to "1" to exit the MB PnP Mode.

6.2 Register Descriptions

Table 6-1. Configuration Register List

Register Name	R/W	LDN	Index	Default
Configure Control	W	All	02h	-
Logic Device Number (LDN)	R/W	All	07h	00h
Chip ID Byte 1	R	All	20h	87h
Chip ID Byte 2	R	All	21h	06h
Chip Version	R/W[Note1]	All	22h	00h
Test Mode Register	R/W	F4h	2Fh	00h
Simple I/O Base Address MSB Register	R/W	10h	60h	00h
Simple I/O Base Address LSB Register	R/W	10h	61h	00h
Panel Button De-bounce Base Address MSB Register	R/W	10h	62h	00h
Panel Button De-bounce Base Address LSB Register	R/W	10h	63h	00h
GPIO Set 1 Pin Polarity Register	R/W	10h	F0h	00h
GPIO Set 2 Pin Polarity Register	R/W	10h	F1h	00h
GPIO Set 3 Pin Polarity Register	R/W	10h	F2h	00h
Simple I/O Set 1 Output Enable Register	R/W	10h	F3h	00h
Simple I/O Set 2 Output Enable Register	R/W	10h	F4h	00h
Simple I/O Set 3 Output Enable Register	R/W	10h	F5h	00h
Panel Button De-bounce Control Register	R/W	10h	F5h	00h
Panel Button De-bounce Set 1 Enable Register	R/W	10h	F7h	00h
Panel Button De-bounce Set 2 Enable Register	R/W	10h	F8h	00h
Panel Button De-bounce Set 3 Enable Register	R/W	10h	F9h	00h

Note 1: Bits 5-4 in the register are write only. Bits 3-0 are read only.

6.2.1 Configure Control — Index 02h

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	R/W	Default	Description
7-2	-		**Reserved**
1	W		Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	-		**Reserved**

6.2.2 Logical Device Number (LDN) — Index 07h

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

Bit	R/W	Default	Description
7-0	R/W	00h	**LDN**

6.2.3 Chip ID Byte 1 — Index 20h

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=87h when read.

Bit	R/W	Default	Description
7-0	R	87h	**Chip ID 1**

6.2.4 Chip ID Byte 2 — Index 21h

This register is the Chip ID Byte 2 and is **read only**. Bits [7:0]=06h when read.

Bit	R/W	Default	Description
7-0	R	06h	**Chip ID 2**

6.2.5 Chip Version — Index 22h

Bit	R/W	Default	Description
7-6	-		**Reserved**
5-4	W		**Multi-chips selection.** These two bits can be written. When these bits are written, the MB PnP mode will be forced to exit if the given values do not match the MCI[1:0]. The MB PnP will be remained if the given values match the MCI[1:0].
3-0	R	0h	**Chip Version.** Read only.

6.2.6 Test Mode Register — Index 2Fh

This register is the Test Mode Register and is reserved for ITE. It should not be set.

6.2.7 Simple I/O Base Address MSB Register — Index 60h

Bit	R/W	Default	Description
7-4	R	0h	READ only as “0h” for Base Address [15:12].
3-0	R/W	0h	READ/WRITE, mapped as Base Address [11:8].

6.2.8 Simple I/O Base Address LSB Register — Index 61h

Bit	R/W	Default	Description
7-0	R/W	00h	Mapped as Base Address [7:0].

6.2.9 Panel Button De-bounce Base Address MSB Register — Index 62h

Bit	R/W	Default	Description
7-4	R	0h	Read only as “0h” for Base Address [15:12].
3-0	R/W	0h	READ/WRITE, mapped as Base Address [11:8].

6.2.10 Panel Button De-bounce Base Address LSB Register — Index 63h

Bit	R/W	Default	Description
7-0	R/W	00h	Mapped as Base Address [7:0]

6.2.11 GPIO Pin Set 1, 2 and 3 Polarity Registers — Index F0h, F1h and F2h

These registers are used to program the GPIO pin type as polarity inverting or non-inverting.

Bit	R/W	Default	Description
7-0	R/W	00h	1: Inverting 0: Non-inverting

6.2.12 Simple I/O Set 1, 2, and 3 Output Enable Registers — Index F3h, F4h and F5h

These registers are used to determine the direction of the Simple I/O.

Bit	R/W	Default	Description
7-0	R/W	00h	0: Input mode 1: Output mode

6.2.13 Panel Button De-bounce Control Register — Index F6h

Bit	R/W	Default	Description
7-3	R/W	0h	**Reserved**
2	R/W	0b	**SMI# Output Enable.** 0: Disable 1: Enable
1-0	R/W	00b	**De-bounce Time Selection** 00: 8ms (6ms ignored, 8ms passed) 01: 16ms (12ms ignored, 16ms passed) 10: 32ms (24ms ignored, 21ms passed) 11: 64ms (48ms ignored, 64ms passed)

6.2.14 Panel Button De-bounce Set 1, 2, and 3 Enable Registers — Index F7h, F8h and F9h

These registers are used to enable Panel Button De-bounce for each pin.

Bit	R/W	Default	Description
7-0	R/W	00h	1: Enable 0: Disable

7. Functional Description

7.1 LPC Interface

The IT8706R supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29, 1997). The IT8706R supports the required signals LAD3-0, LFRAME#, LRESET#, LCLK (LCLK is the same as PCICLK.).

7.1.1 LPC Transactions

The IT8706R supports some parts of the cycle types described in the LPC I/F specification. I/O read and I/O write cycles are used for the programmed I/O cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the IT8706R processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on the result.

7.2 General Purpose I/O

The IT8706R provides three sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions include the simple I/O function and Panel Button De-bounce.

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into three registers. The accessed I/O ports are programmable and are three consecutive I/O ports (Base Address+0, Base Address+1, and Base Address+2). The Base Address is programmed on the registers of Simple I/O Base Address LSB and MSB registers (LDN=10h, Index=60h and 61h).

The Panel Button De-bounce is an input function. After the panel button de-bounce is enabled, a related status bit will be set when an active pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. SMI# will be issued if any one of the status bit is set. However, the new setting status will not issue another interrupt unless the previous status bit is cleared before being set. When an active pulse is continuous active after status bits are cleared, another de-bounce operation will be started.

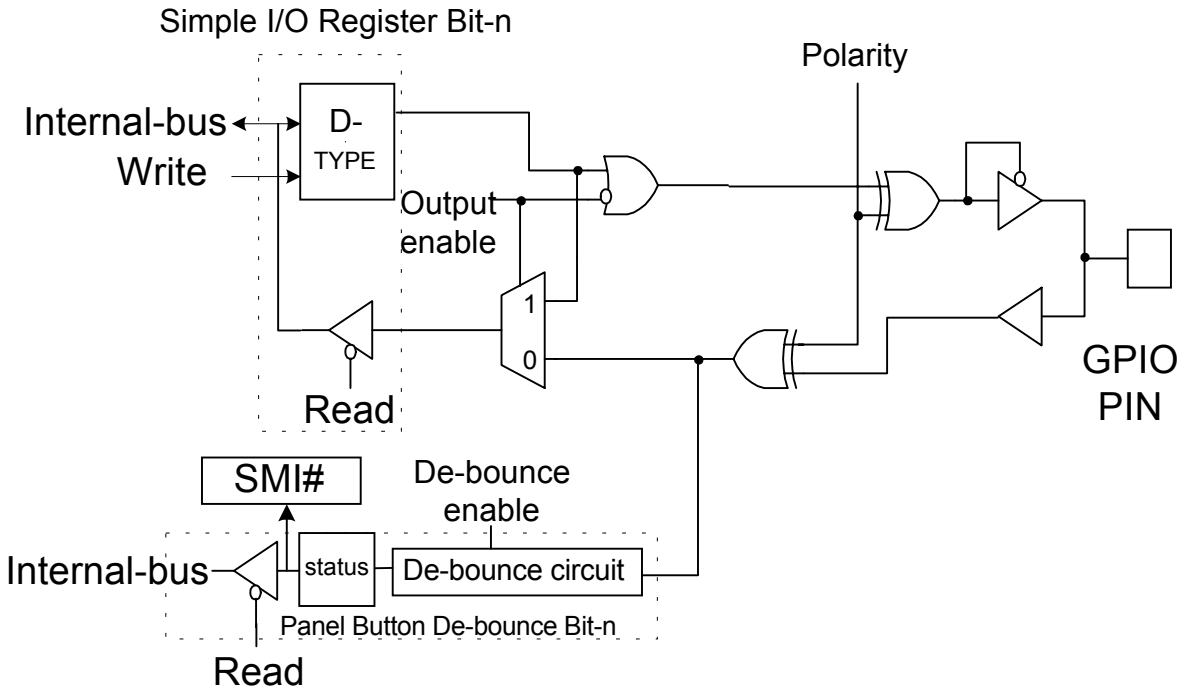


Figure 7-1. General Logic of GPIO Function

7.3 Power On Strapping Options

	Symbol	Description
MCI[1:0]	Multi-Chips Identification [1:0]	These two power-on strapping bits are used to clarify multiple IT8706Rs in a system. Please refer to the register description for details.

8. DC Characteristics

Absolute Maximum Ratings

Power Supply (V_{CC}).....-0.5V to 7.0V

Input Voltage.....-0.5V to VCC + 0.5V

Output Voltage.....-0.5V to VCC + 0.5V

Storage Temperature.....-55°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=5V ± 5%, Ta = 0°C to + 70°C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
DIO8 Type Buffer						
V_{IL}	Input Low Voltage		-	-	0.8	V
V_{IH}	Input High Voltage		2.2	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=8mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-8mA	2.4	-	-	V
I_{IL}	Input Leakage current	V_{IN}=0	-	10	-	uA
I_{IH}	High Input Leakage current	V_{IN}=VCC	-	-	-10	uA
I_{OZ}	Tri-state leakage current		-	-	20	uA
DIOD8 Type Buffer						
V_{IL}	Input Low Voltage		-	-	0.8	V
V_{IH}	Input High Voltage		2.2	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=8mA	-	-	0.4	V
I_{IL}	Low Input Leakage current	V_{IN}=0	-	10		uA
I_{IH}	High Input Leakage current	V_{IN}=VCC	-	-	-10	uA
I_{OZ}	Tri-state leakage current		-	-	20	uA
DI Type Buffer						
V_{IL}	Input Low Voltage		-	-	0.8	V
V_{IH}	Input High Voltage		2.2	-	-	V
I_{IL}	Input Leakage current	V_{IN}=0	-	10	-	uA
I_{IH}	High Input Leakage current	V_{IN}=VCC	-	-	-10	uA

9. AC Characteristics

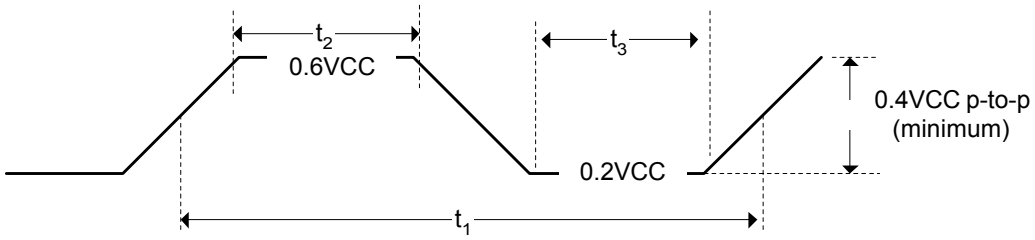


Figure 9-1. LCLK Waveform

Table 9-1. LCLK and LRESET# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			µsec

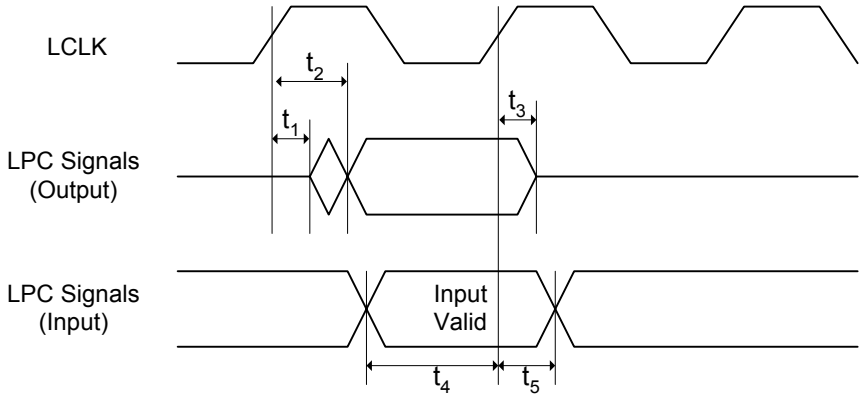


Figure 9-2. LPC Waveform

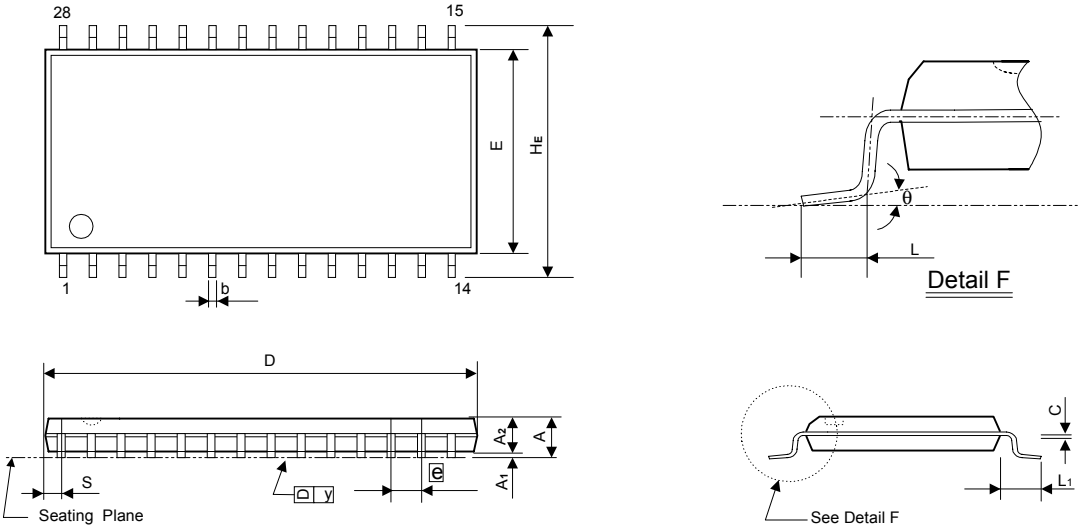
Table 9-2. LPC AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

10. Package Information

SOP 28 Outline Dimensions

unit: inches/mm



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.012	0.20	0.25	0.30
D	—	0.713	0.728	—	18.11	18.49
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_1	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°		8°	0°		8°

11. Ordering Information

Part No.	Package
IT8706R	28 SOP