INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8661F & IT8661RF

Plug and Play Super AT I/O

Preliminary Specification V0.6

INTEGRATED TECHNOLOGY EXPRESS, INC.

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1. Features

- **PC97/98 Compliant Hardware (PC99 Ready)**
  - Unique PnP device ID for each logical device compliant with Plug and Play specification V1.0a
  - Built-in resource data ROM
  - Five (5) logical devices
  - 16-bit address decoding
  - Seven (7) selectable IRQs
  - Four (4) selectable DMA channels
  - Flexible resource configure and dynamic disable
  - IRQ sharing supported 2.88MB floppy disk controller
  - Base address 0x0100h-0x0FF8h, seven IRQ and four DMA options
  - 48mA direct output driver
  - Enhanced digital data separator
  - A and B drives can be logically swapped via registers
  - 3-mode drives supported
  - Supports automatic write protection via software
  - Supports two (2) 360K/ 720K/ 1.2M/ 1.44M/2.88M floppy disk drives
- **Multi-mode High Performance Parallel Port**
  - Base address 0x0100h-0x0FFCh, seven IRQ and four DMA options
  - Standard mode -- bi-directional SPP
  - Enhanced mode – EPP V1.7 and EPP V1.9 compliant
  - High Speed mode -- ECP, IEEE1284 compliant
  - Backdrive current protection
  - Printer power-on damage protection
- **Serial Ports**
  - Base address 0x100h-0x0FF8h, seven (7) IRQ options
  - Supports two 16C550 standard compatible enhanced serial ports
  - Supports send/receive 16-byte FIFOs
  - MIDI standard compatible
- **Infrared Communication Controller**
  - Base address 0x0100h-0x0FF8h, seven(7) IRQ and four (4) DMA options
  - Supports HPSIR or ASKIR infrared interface
  - Only IT8661RF supports MIR or FIR
  - Dedicated 16C550 standard UART supporting infrared communication
  - Single or dual DMA channel mode for FIR (RF version only)
  - Back-to-back packet transmission and reception for FIR (RF version only)
  - Supports 2-input FIR transceiver or 1-input FIR transceiver interface (RF version only)
- Provides thirteen (13) General Purpose I/O pins
- Only one (1) 24MHz or 48MHz crystal needed
- 5-volt operation
- 100-pin QFP package

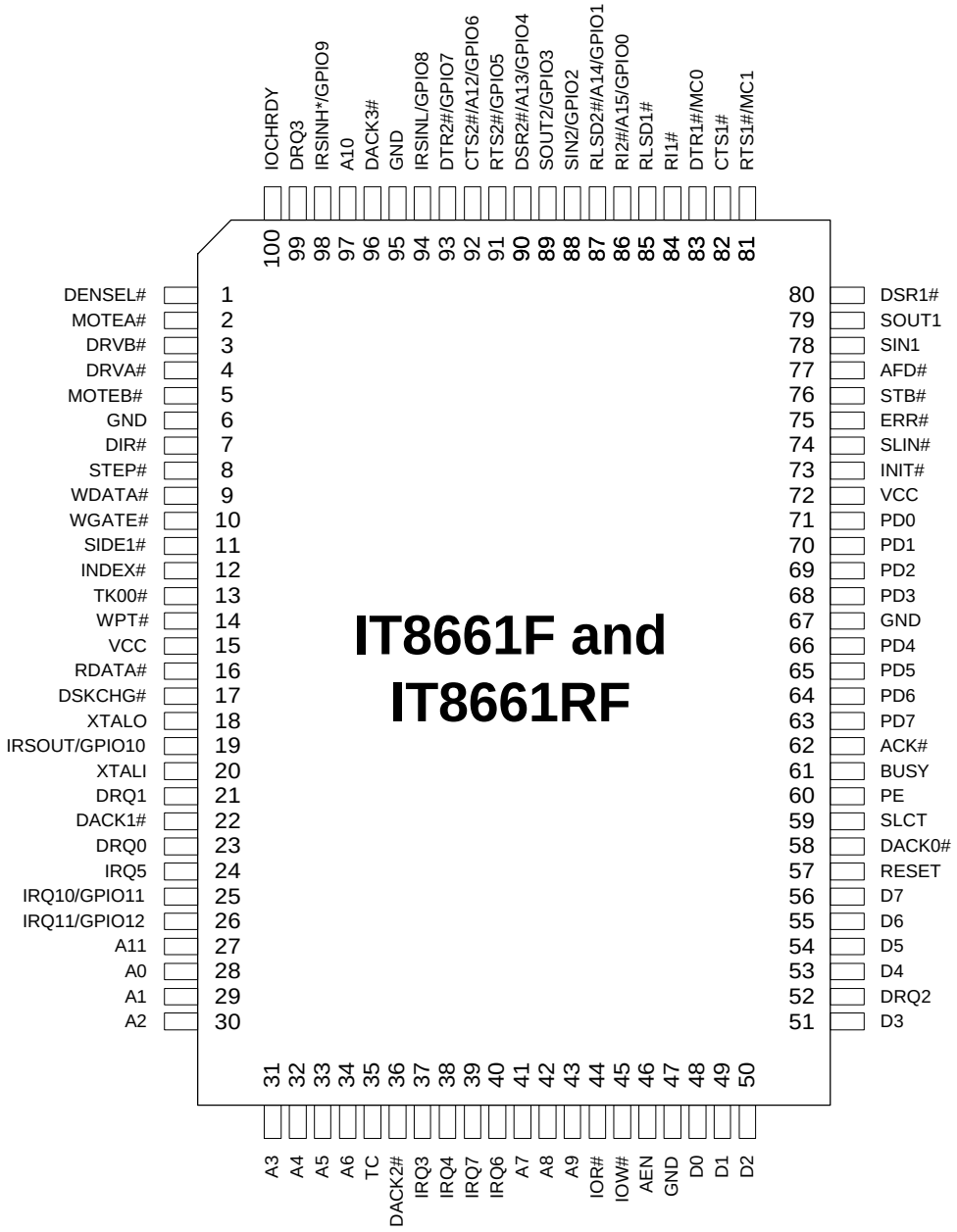
2. General Description

The IT8661F and IT8661RF Plug and Play Super AT I/O chip are user-friendly, low cost peripheral controllers. They provide an ideal solution for Microsoft PC97/98 (PC99 ready) system requirements. A programmable IRQ sharing function is supported to comply with Microsoft PC97/98 (PC99 ready) requirements. No N.V. memory is needed to store resource data for Plug and Play system applications.

The IT8661F and IT8661RF consist of five (5) logical devices. One (1) high performance 2.88MB floppy disk controller, with digital data separator, supports two (2) 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives. One multi-mode high performance Parallel Port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP. V1.7 and v1.9 are supported), and IEEE 1284 compliant Extended Capabilities Port (ECP). Two (2) 16C550 standard compatible enhanced UARTs perform asynchronous communication for serial ports. One (1) highly integrated infrared communication controller is capable of supporting HPSIR, MIR, FIR or ASKIR with a built-in dedicated 16C550 standard compatible UART (MIR and FIR are available only on the RF version).

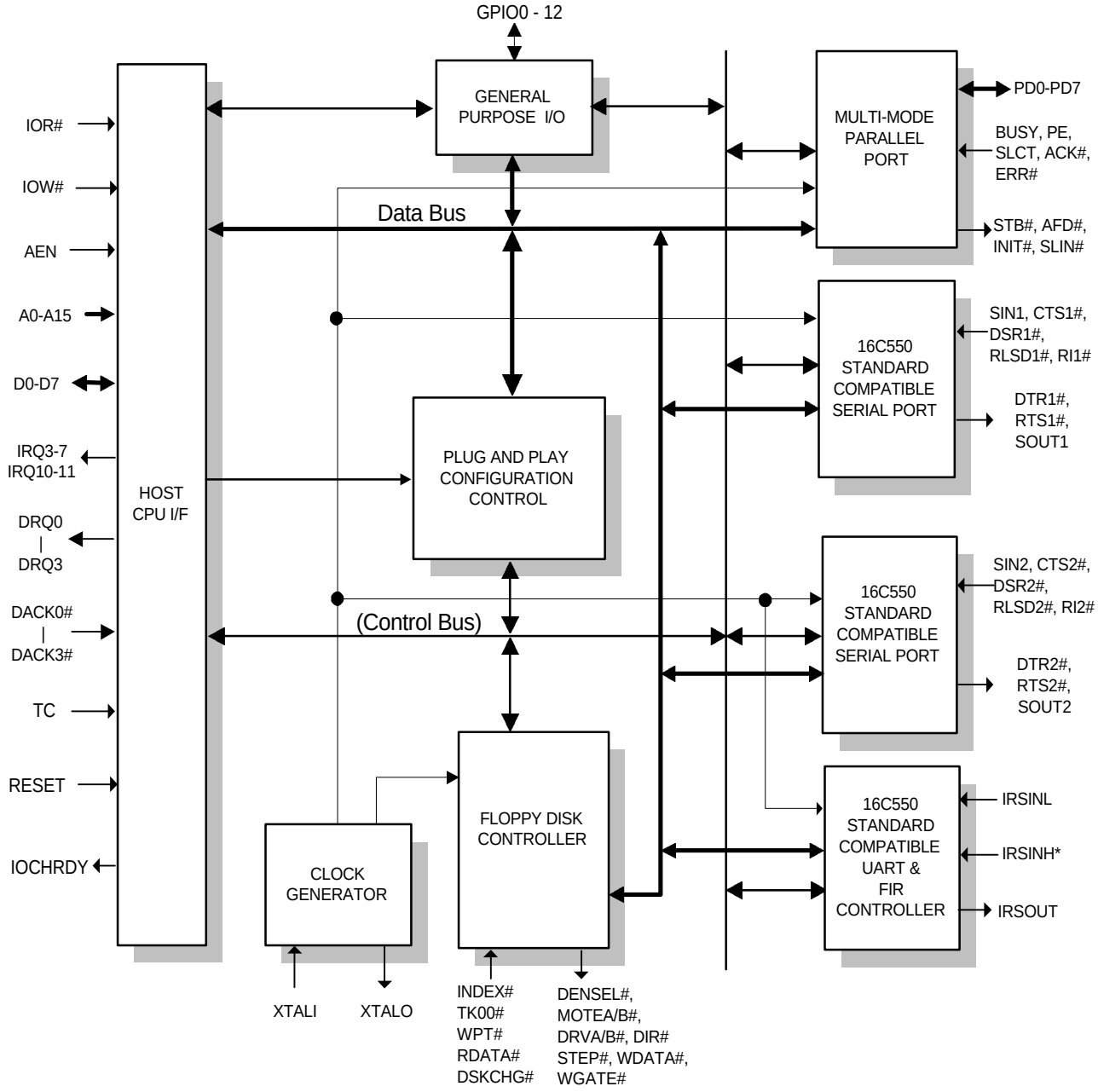
These five (5) logical devices can be individually enabled or disabled via software configuration registers. The IT8661F and IT8661RF utilize power saving circuitry to reduce power consumption. Once a logical device is disabled, its related inputs are gate inhibited, outputs are tristated, and input clock is disabled. The Parallel Port includes a specifically designed circuit to reduce damage or backdrive current when a printer or another parallel port device is powered-on. In effect, the IT8661F and IT8661RF are high-performance, low-power consumption I/O device.

3. Pin Configuration



*** Note**: IRSINH is available for IT8661RF only.

4. Block Diagram



*** Note**: IRSINH is available for IT8661RF only.

5. IT8661F and IT8661RF Pin Descriptions

Table 5-1. Signal Names (by pin numbers in alphabetical order)

Pin No.	Symbol	I/O	Description
1	DENSEL#	O48	DENSEL# is high for high data rate (500 Kbps/1 Mbps) DENSEL# is low for low data rate (250/300 Kbps)
2	MOTEA#	O48	FDD Motor A Enable, active low
3	DRVB#	O48	FDD Drive B Enable, active low
4	DRVA#	O48	FDD Drive A Enable, active low
5	MOTEB#	O48	FDD Motor Enable, active low
7	DIR#	O48	FDC Head Direction. Step in when low, step out when high during a SEEK operation.
8	STEP#	O48	FDC Step Pulse Output to the drive during a SEEK operation, active low.
9	WDATA#	O48	FDC Write Serial Data to the drive, active low
10	WGATE#	O48	FDC Write Enable Identify, active low
11	SIDE1#	O48	Floppy Disk Side 1 Select, active low
12	INDEX#	IS	FDC Index, active low. Indicates the beginning of a disk track.
13	TK00#	IS	Floppy Disk Track 0, active low. Indicates that the head of the selected drive is on track zero (0).
14	WPT#	IS	FDD Write Protect, active low. Indicates that the disk of the selected drive is write-protected.
16	RDATA#	IS	Read Disk Data, active low, serial data input from the FDD
17	DSKCHG#	IS	Floppy Disk Change, active low. This is an input pin that senses whether the drive door has been opened or a diskette has been changed.
18	XTALO	OCLK	24 MHz or 48 MHz Crystal Oscillator Output. If an external clock is used, this pin is left disconnected.
19	IRSOUT/GPIO10	I/O24	Infrared data output of SIR or FIR. The second function is General Purpose I/O.
20	XTALI	ICLK	24 MHz or 48 MHz Crystal Oscillator Input. An external clock in use must be connected to this pin.
23, 21 52, 99	DRQ0 - 3	OP12	DMA Request 0, 1, 2, 3. The logical devices of the IT8661F and IT8661RF can be mapped to individual DRQx via configuration register(0x74). These signals are cleared by the going-low of DACK 0, 1, 2, and 3# signals.
22, 58 36, 96	DACK0 - 3#	IS	DMA Acknowledge 0, 1, 2, 3. The logical devices of the IT8661F and IT8661RF can be mapped to individual DACKx.
25	IRQ10/GPIO11	OD24 I/O24	Interrupt Request 10. The logical devices of the IT8661F and IT8661RF can be mapped to the individual IRQx via configuration register (0x70). The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.

Table 5-2. Signal Names (by pin numbers in alphabetical order) [cont'd]

Pin No.	Symbol	I/O	Description
26	IRQ11/GPIO12	OD24 I/O24	Interrupt Request 11. The logical devices of the IT8661F and IT8661RF can be mapped to the individual IRQx via configuration register (0x70). The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
97, 27, 41-43, 28-34	A0 - A11	IS	12-bit I/O Address bus
35	TC	IS	Terminal Count, active high to indicate that data transfer is completed
40, 39 37, 38 24	IRQ3 - 7	OD24	Interrupt Request 3, 4, 5, 6, 7. The logical devices of the IT8661F and IT8661RF can be mapped to the individual IRQx via configuration register(0x70).
44	IOR#	IS	Read Strobe, active low
45	IOW#	IS	Write Strobe, active low
46	AEN	IS	Address Enable, active high to indicate that the system is in DMA transfer mode
53-56 48-51	D0 - D7	I/O24	8-bit bi-directional data bus
57	RESET	IS	SYSTEM RESET, active high. At the falling edge of RESET, the voltage level of MC0 (pin 83) and MC1 (pin 81) are latched.
59	SLCT	IS	Printer Select. This signal goes high when the line printer has been selected.
60	PE	IS	Printer Paper End. This signal is set high by the printer when it runs out of paper.
61	BUSY	IS	Printer Busy. This signal goes high when the line printer has a local operation in progress and cannot accept data.
62	ACK#	IS	Printer Acknowledge. This signal goes low to indicate that the printer has already received a character and is ready to accept another.
68-71 63-66	PD7 - PD0	I/O24	Parallel Port Data Bus. This bus provides a byte-wide input or output to the system. The eight (8) lines are held in high-impedance state when the port is deselected.
73	INIT#	O24	Printer Initialize. Active low, this signal is derived from bit 2 of the printer control register, and is used to initialize printer.

Table 5-3. Signal Names (by pin numbers in alphabetical order) [cont'd]

Pin No.	Symbol	I/O	Description
75	ERR#	IS	Printer Error. Active low to indicate that the printer has encountered an error. The error message can be read from bit 3 of the printer status register.
76	STB#	O24	Printer Strobe. Active low, this signal is derived from the complement of bit 0 of the printer control register. It is used to strobe printer data into the printer.
77	AFD#	O24	Printer Autofeed. Active low, this signal is derived from the complement of bit 1 of the printer control register. It is used to inform the printer to advance one line after previous lines are printed.
78	SIN1	IS	Serial Port 1, Data Input.
79	SOUT1	O12	Serial Port 1, Data Output.
80	DSR1#	IS	Serial Port 1, Data Set Ready, active low.
81	RTS1#/MC1	O12/I	Serial Port 1, Request to Send Output, active low. During the hardware reset, this pin and pin 83 become input and DTR1# is tristated, then latches the voltage level of MC1 to clarify systems that use the same IT8661F and IT8661RF I/O controller. (Refer to the general description of the configuring sequence on Page9.)
82	CTS1#	O12/I	Serial Port 1, Clear to Send Input, active low.
83	DTR1#/MC0	O12/I	Serial Port 1, Data Terminal Ready Output, active low. During the hardware reset, this pin and pin 81 become input and DTR1# is tristated, then latches the voltage level of MC0 to clarify systems that use the same IT8661F and IT8661RF I/O controller. (Refer to the general description of the configuring sequence on Page 9.)
84	RI1#	IS	Serial Port 1, Ring Indicator, active low.
85	RLSD1#	IS	Serial Port 1, Receive Line Signal Detect, active low.
86	R12#/A15/GPIO0	I/O12	Serial Port 2, Ring Indicator, active low. The second function is I/O Address 15. The third function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
87	RLSD2#/A14/ GPIO1	I/O12	Serial Port 2, Receive Line Signal Detect, active low. The second function is I/O Address 14. The third function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
88	SIN2/GPIO2	I/O12	Serial Port 2, Data Input. The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
89	SOUT2/GPIO3	I/O12	Serial Port 2, Data Output. The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
90	DSR2#/A13/ GPIO4	I/O12	Serial Port 2, Data Set Ready, active low. The second function is I/O Address 13. The third function is General Purpose I/O. This pin is internally pulled up to 50KΩ.

Table 5-4. Signal Names (by pin numbers in alphabetical order) [cont'd]

Pin No.	Symbol	I/O	Description
92	CTS2#/A12/GPIO6	I/O12	Serial Port 2. Clear to Send Input, active low. The second function is I/O Address 12. The third function is General Purpose I/O.
93	DTR2#GPIO7	I/O12	Serial Port 2, Data Terminal Ready Output, active low. The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
94	IRSINL/GPIO8	I/O12	The first function is one of the following: (1) Infrared data input pin or (2) Low frequency infrared data input pin of 2-input FIR transceiver (HP-like) or (3) Infrared data input pin of 1-input FIR transceiver (IBM-like). The second function is General Purpose I/O. This pin is internally pulled up to 50KΩ.
98	IRSINH*/GPIO9	OD12	The IT8661F is a high-frequency infrared data input pin of 2-input FIR transceiver(HP-like) or mode select output pin of 1-input FIR transceiver (IBM-like). The second function for both IT8661F and IT8661RF is General Purpose I/O. This pin is internally pulled up 50KΩ.
100	IOCHRDY	OD24	EPP mode, pulled low to extend the READ/WRITE command
15, 72	VCC		+5V power pin
6, 47 67, 95	GND		Ground

*** Note**: IRSINH is available for IT8661RF only.

6. Configuring Sequence Description

6.1 General Description

After hardware reset or power-on reset, the IT8661F and IT8661RF enter the normal mode with all logical devices disabled. There are two configuration modes for IT8661F and IT8661RF, MB PnP mode and ISA PnP mode.

The MC0 (pin 83) and MC1 (pin 81) are used to clarify different systems that use the same IT8661F and IT8661RF I/O controller. In ISA PnP mode, the latched values of MC0 and MC1 can be used as the serial number LSB of to clarify different systems that use the same IT8661F and IT8661RF I/O controller. In MB PnP mode, if bits 5 and 4 of global configuration register index 22h are written and the values of bits 5 and 4 equal the corresponding latch-reversed values of MC1 and MC0, then the MB PnP configuration mode can be entered. This can clarify different systems that use the same IT8661F and IT8661RF I/O controller in MB PnP mode.

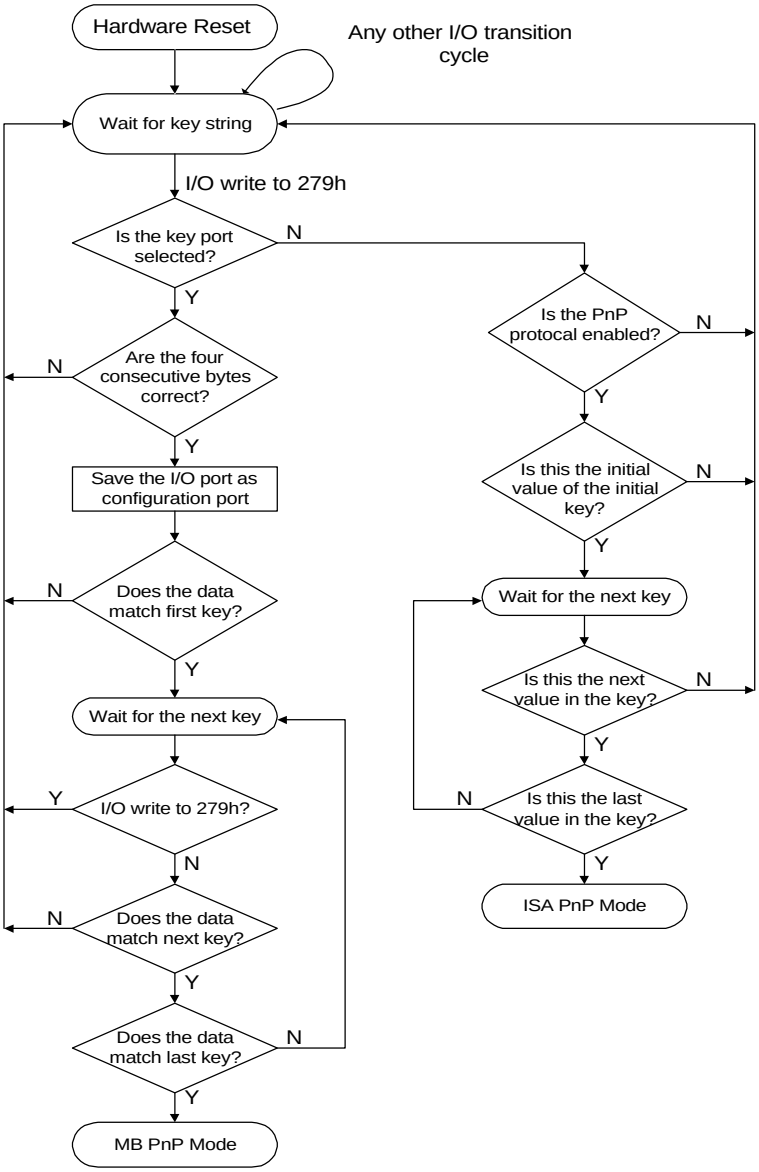


Figure 6-1. Configuration Sequence Flow Chart

6.2 MB PnP Mode

There are three (3) steps to complete the configuration setup: (1) Enter the MB PnP mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP mode. Unless normal exiting is done, the configuration setup may cause undesired results.

(1) Enter the MB PnP Mode

To enter the MB PnP mode, 36 special I/O write operations are to be performed during the Wait for Key state. To ensure the initial state of the key-check logic, it is first necessary to perform two write operations to Address port (279h) of the ISA PnP.

The Entering Key includes two (2) steps. The first FOUR (4) bytes are used to determine the I/O address and data port of configuration register. If the other 32 bytes are not written properly and sequentially, it will cause a failure in the MB PnP mode while performing any IOR/IOW command to other I/O ports. To avoid this situation, we suggest that programmers disable interrupts while performing the 36 write operations. The corresponding sequential data for the first four (4) bytes are:

	I/O Address port	Data port
86h, 61h, 55h, 55h;	3F0h;	3F1h
or 86h, 61h, 55h, AAh;	3BDh;	3BFh
or 86h, 61h, AAh, 55h;	370h;	371h

The sequential data for the other 32 bytes (same as the initial key of ISA PnP, but written to different I/O ports) are listed below in hexadecimal numeration:

6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61,
B0, 58, 2C, 16, 8B, 45, A2, D1
E8, 74, 3A, 9D, CE, E7, 73, 39

(2) Modify the Data of Configuration Registers

After entering the MB PnP mode, all configuration registers can be accessed. However, modifying the data of the registers marked only for ISA PnP may cause undesired errors. Before the access to a selected register, the content of Index 07h must be changed to be consistent with the LDN to which the register belongs. Some registers, with Index 25h, 26h, 2Eh, and 2Fh, can be affected unless the last step is completed.

(3) Exit the MB PnP mode

Set bit 1 of the configure control register (Index 02h) to “1” to exit the MB PnP mode.

6.3 ISA PnP Mode

This mode is ISA PnP standard compliant. (Please refer to Plug and Play, ISA Spec V1.0a for detailed descriptions.) In this mode, only some configuration registers of this chip can be accessed. The enable register for PnP logical device must be asserted prior to entering the MB PnP mode. Since the LDNs are dynamic, users can assign logical devices to be configured by ISA Plug and Play V1.0a protocol because they always remain enabled in PC systems and thus utilize fixed resources.

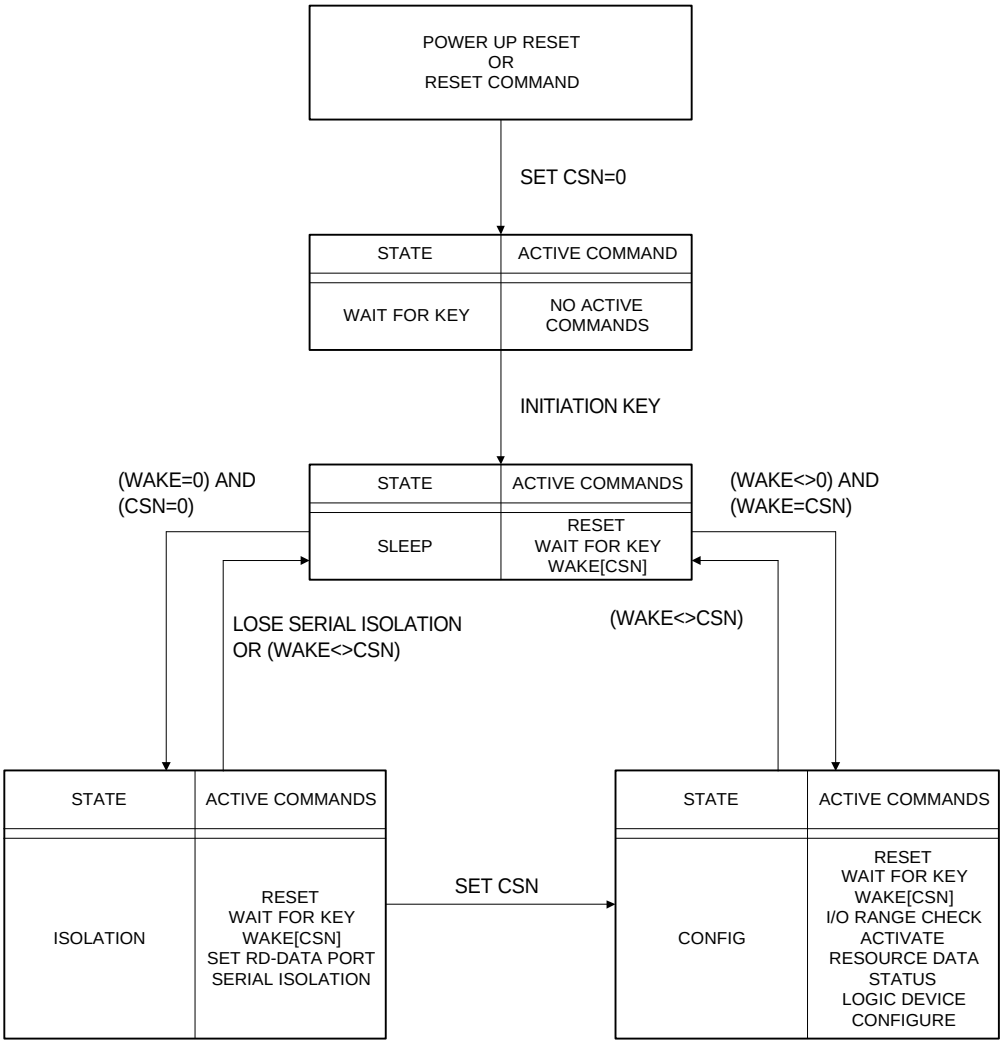


Figure 6-2. PnP State Transition

6.4 Plug and Play Operation Sequence

Refer to Figure 6-2. PnP State Transition. Here is an example of a procedure to be followed for IT8661F and IT8661RF setup. It is optional and not the only sequence of events that may occur. For any state and at any time, all valid commands can be received and followed with proper feedback or response.

a. At power-on or when the RESET signal is activated:
- The Card Select Number (CSN) sets to "0X00".
- All configuration registers for logical devices are set to their internal power-on default values.

b. The Linear Feedback Shift Register (LFSR) is reset to its initial state (0X6A).

c. Entering the "Wait for Key" state.

The IT8661F and IT8661RF enter this state within 1.5ms after RESET signal or RESET command. The initiation key is written to IT8661F and IT8661RF. Each value of the initiation key is calculated after shifting the LFSR by one clock for each write, and the written data is compared with the calculated (expected) data. In this state, the chip will reset the LFSR to "0X6A" whenever it receives a write from the address port that does not match the current value in the LFSR.

d. Once the initiation key is correctly received, the chip enters the "Sleep" state (the auto configuration ports are enabled.)

e. The system sends a WAKE[CSN=0] command to switch the chip into the "Isolation" state.

f. The system sets the RD_DATA port to an arbitrary address.

g. The system performs the isolation protocol by sending a sequence of 72 pairs of I/O READ operations. (Refer to Hardware Protocol in ISA PnP Spec V1.0a.)

h. Provided IT8661F and IT8661RF pass the isolation protocol, the system sets the CSN to a non-zero value (assigned OUR_CSN) and IT8661F and IT8661RF enter the "Configuration" state.

I. The system reads the resource data from the IT8661F and IT8661RF.

j. The system switches IT8661F and IT8661RF into "Sleep" state by sending a "WAKE" command with a CSN that is different from OUR_CSN. When IT8661F and IT8661RF are in "Sleep" state, the system can perform operations from other Plug and Play chips.

k. The system sends a "WAKE[OUR_CSN]" command, and the IT8661F and IT8661RF return to the "Configuration" state.

l. The system sets the logical device information and activates each of the logical devices.

m. The system sends other commands.

n. The system sends a "WAIT FOR KEY" command, and the IT8661F and IT8661RF returns to the "Wait for Key" state (the auto-configuration ports are disabled).

Notes:

* At power-on or when the RESET signal is activated, go to step a.

** When a "WAIT FOR KEY" command is received, go to step b.

6.5 Description of the Configuration Registers

All the registers will be reset to the default state when RESET is activated. When the RESET command is asserted (configure control bit 0), the test registers and the registers which can be accessed during the ISA PnP mode, will be reset to their initial values (default values) in either the ISA PnP mode or the MB PnP mode; while the others (cannot be accessed during the ISA PnP mode) will be reset to the default values only in the MB PnP mode. Other registers with Index=22h, 23h, 24h, or 25h, are reset by the RESET command.

Configuration Port	0X0279h	write-only
Write-data Port	0X0A79h	write-only

Table 6-1. Global Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
All	00h	W	NA	ISA PnP	Set RD_DATA port
All	01h	R	NA	ISA PnP	Serial Isolation
All	02h	W	NA	ISA PnP/MB PnP	Configure Control
All	03h	W	NA	ISA PnP	WAKE[CSN]
All	04h	R	NA	ISA PnP	Resource Data
All	05h	R	NA	ISA PnP	Status
All	06h	R/W	00h	ISA PnP	Card Select Number(CSN)
All	07h	R/W	NA	ISA PnP/MB PnP	Logical Device Number(LDN)
All	20h	R	86h	MB PnP	Chip ID Byte 1
All	21h	R	61h	MB PnP	Chip ID Byte 2
All	22h	R-R/W	00h	MB PnP	Chip Version/Multi-chips clarification
All	23h	R/W	00h	MB PnP	PnP Logical Device Enable Register
All	24h	R/W	00h	MB PnP	SOFTWARE SUSPEND/Input Clock Select Register
All-05h[*2]	25h	R-R/W	00h	MB PnP	GPIO Function Enable Register[12:8]
All-05h[*2]	26h	R-R/W	00h	MB PnP	GPIO Function Enable Register[7:0]

Table 6-2. FDC Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
00h	30h	R/W	00h	ISA PnP/MB PnP	FDC Activate
00h	31h	R/W	00h	ISA PnP	FDC I/O Range Check
00h	60h	R/W	03h	ISA PnP/MB PnP	FDC Base Address MSB Register
00h	61h	R/W	F0h	ISA PnP/MB PnP	FDC Base Address LSB Register
00h	70h	R/W	06h	ISA PnP/MB PnP	FDC Interrupt Level Select
00h	71h	R	02h	ISA PnP	FDC Interrupt Type
00h	74h	R/W	02h	ISA PnP/MB PnP	FDC DMA Channel Select
00h	F0h	R/W	00h	MB PnP	FDC Special Configuration Register

Table 6-3. Serial Port 1 Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
01h	30h	R/W	00h	ISA PnP/MB PnP	Serial Port 1 Activate
01h	31h	R/W	00h	ISA PnP	Serial Port 1 I/O Range Check
01h	60h	R/W	03h	ISA PnP/MB PnP	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	ISA PnP/MB PnP	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	ISA PnP/MB PnP	Serial Port 1 Interrupt Level Select
01h	71h	R	02h	ISA PnP	Serial Port 1 Interrupt Type
01h	F0h	R/W	00h	MB PnP	Serial Port 1 Special Configuration Register

Table 6-4. Serial Port 2 Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
02h	30h	R/W	00h	ISA PnP/MB PnP	Serial Port 2 Activate
02h	31h	R/W	00h	ISA PnP	Serial Port 2 I/O Range check
02h	60h	R/W	02h	ISA PnP/MB PnP	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	ISA PnP/MB PnP	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	ISA PnP/MB PnP	Serial Port 2 Interrupt Level Select
02h	71h	R	02h	ISA PnP	Serial Port 2 Interrupt Type
02h	F0h	R/W	00h	MB PnP	Serial Port 2 Special Configuration Register

Table 6-5. Parallel Port Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
03h	30h	R/W	00h	ISA PnP/MB PnP	Parallel Port Activate
03h	31h	R/W	00h	ISA PnP	Parallel Port I/O Range Check
03h	60h	R/W	03h	ISA PnP/MB PnP	Parallel Port Base Address 1 MSB Register
03h	61h	R/W	78h	ISA PnP/MB PnP	Parallel Port Base Address 1 LSB Register
03h	62h	R/W	07h	ISA PnP/MB PnP	Parallel Port Base Address 2 MSB Register
03h	63h	R/W	78h	ISA PnP/MB PnP	Parallel Port Base Address 2 LSB Register
03h	70h	R/W	07h	ISA PnP/MB PnP	Parallel Port Interrupt Level Select
03h	71h	R	02h	ISA PnP	Parallel Port Interrupt Type
03h	74h	R/W	03h	ISA PnP/MB PnP	Parallel DMA Channel Select[*3]
03h	F0h	R/W	03h[*4]	MB PnP	Parallel Port Special Configuration Register

Table 6-6. IR Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
04h	30h	R/W	00h	ISA PnP/MB PnP	IR Activate
04h	31h	R/W	00h	ISA PnP	IR I/O Range Check
04h	60h	R/W	02h	ISA PnP/MB PnP	IR Base Address 1 MSB Register
04h	61h	R/W	E8h	ISA PnP/MB PnP	IR Base Address 1 LSB Register
04h	62h	R/W	03h	ISA PnP/MB PnP	IR Base Address 2 MSB Register (IT8661RF Only)
04h	63h	R/W	00h	ISA PnP/MB PnP	IR Base Address 2 LSB Register (IT8661RF Only)
04h	70h	R/W	0Ah	ISA PnP/MB PnP	IR Interrupt Level Select 1
04h	71h	R	02h	ISA PnP	IR Interrupt Type 1
04h	72h	R/W	0Bh	ISA PnP/MB PnP	IR Interrupt Level Select 2 (IT8661RF Only)
04h	73h	R	02h	ISA PnP	IR Interrupt Type 2 (IT8661RF Only)
04h	74h	R/W	01h	ISA PnP/MB PnP	IR DMA Channel Select 1 (IT8661RF Only)
04h	75h	R/W	00h	ISA PnP/MB PnP	IR DMA Channel Select 2 (IT8661RF Only)
04h	F0h	R/W	00h	MB PnP	IR Special Configuration Register

Table 6-7. GPIO & Alternate Function Configuration Registers

LDN[*1]	Index	R/W	Reset	Access Mode	Configuration Register or Action
05h	60h	R/W	00h	MB PnP	CS0 Base Address MSB Register
05h	61h	R/W	00h	MB PnP	CS0 Base Address LSB Register
05h	62h	R/W	00h	MB PnP	CS1 Base Address MSB Register
05h	63h	R/W	00h	MB PnP	CS1 Base Address LSB Register
05h	64h	R/W	00h	MB PnP	CS2 Base Address MSB Register
05h	65h	R/W	00h	MB PnP	CS2 Base Address LSB Register
05h	66h	R/W	00h	MB PnP	Simple I/O Base Address MSB Register
05h	67h	R/W	00h	MB PnP	Simple I/O Base Address LSB Register
05h	70h	R/W	00h	MB PnP	GPIO Interrupt Level Select
05h	F0h	R/W	00h	MB PnP	GPIO[7:0] Pin Polarity Register
05h	F1h	R/W	00h	MB PnP	CS0 Control Register
05h	F2h	R/W	00h	MB PnP	CS1 Control Register
05h	F3h	R/W	00h	MB PnP	CS2 Control Register
05h	F4h	R/W	00h	MB PnP	GPIO[7:0] Function Selection Register
05h	F5h	R/W	00h	MB PnP	Simple I/O[7:0] Direction Selection Register
05h	F6h	R/W	00h	MB PnP	Zero Wait State & High Address Qualification Control
05h	F7h	R/W	00h	MB PnP	Device Zero Wait State Enable Register
05h	F8h	R/W	00h	MB PnP	GPIO[12:8] Pin Polarity Register
05h	F9h	R/W	00h	MB PnP	GPIO[12:8] Function Selection Register
05h	FAh	R/W	00h	MB PnP	Simple I/O[12:8] Direction Selection Register
05h	FBh	R/W	00h	MB PnP	High Address Qualification inputs 1 & 2 Selection
05h	FCh	R/W	00h	MB PnP	High Address Qualification inputs 3 & 4 Selection

Notes:

*1: In the ISA PnP mode, the LDNs are dynamic. For example: When the enable register (Index 23h) of a PnP logical device obtains 0Fh (i.e. FDC, Serial Port 1,2 & Parallel Port are enabled); by LDN mapping, 00h stands for FDC; 01h for Serial Port 1; 02h for Serial Port 2; and 03h for Parallel Port. When 06h is given to the register index 23h (only Serial Port 1, 2); by LDN mappings, 00h stands for Serial Port 1, and 01h for Serial Port 2.

*2: Both of these two registers can be read from all LDNs but can only be written if LDN=05h.

*3: When the ECP mode is not enabled, this register is READ-only as “04h”, and cannot be written.

*4: When the bit 2 of the base address of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

6.5.1 Logical Device Base Address

The base I/O range of logical devices shown below is stored in the built-in resource data ROM. PnP BIOS or OS will read this data from the resource data ROM to locate the base I/O address range of each logical device. If there are any I/O port conflicts, PnP OS will automatically re-allocate one of the conflicting ports within the base I/O range.

Table 6-8. Base Address of Logical Devices

Logical Devices	Base I/O Range	Fixed Base Offsets
LDN=0 FDC	[0X0100:0X0FF8] ON 8-BYTE BOUNDARIES	+2H : DOR +4H : MSR/DSR +5H : FIFO +7H : DIR/DCR
LDN=1 SERIAL PORT 1	[0X0100:0X0FF8] ON 8-BYTE BOUNDARIES	+0H : RBR/TBR/DLL div +1H : IER/DLM div +2H : IIR/FCR +3H : LCR +4H : MCR +5H : LSR +6H : MSR +7H : SCR
LDN=2 SERIAL PORT 2	[0X0100:0X0FF8] ON 8-BYTE BOUNDARIES	+0H : RBR/TBR/DLL div +1H : IER/DLM div +2H : IIR/FCR +3H : LCR +4H : MCR +5H : LSR +6H : MSR +7H : SCR
LDN=3 PARALLEL PORT	[0X0100:0X0FF8] ON 8-BYTE BOUNDARIES (SPP : ON 4-BYTE BOUNDARIES) (EPP : ON 8-BYTE BOUNDARIES) [0X0100:0X0FFC] ON 4-BYTE BOUNDARIES	+0H : DATA/ecpAfifo +1H : STATUS +2H : CONTROL +3H : EPP address +4H : EPP data 0 +5H : EPP data 1 +6H : EPP data 2 +7H : EPP data 3 +0H : cfifo/ecpDfifo/cnfgA +1H : cnfgB +2H : ecr +3H : Reserved
LDN=4 IR	[0X0100:0X0FF8] ON 8-BYTE BOUNDARIES [0X0100:0X0FF8] ON 8-BYTE BOUNDARIES	+0H : RBR/TBR/DLL div +1H : IER/DLM div +2H : IIR/FCR +3H : LCR +4H : MCR +5H : LSR +6H : MSR +7H : SCR +0H : MCR +1H : MSR(MISC)/ADDR/Icnfg1 +2H : R(T)fifo/RxBCLR/ITCR +3H : TxC1R/RxBCHR/Icnfg2 +4H : TxC2R/RxRFPLR/TMR +5H : TxSR/RxRFPHR/Icnfg3 +6H : RxC1R/TxBCLR +7H : RxSR(RCR)/TxBCHR

6.6 Global Configuration Registers (LDN: All)

6.6.1 Set RD_DATA Port (Index=00h, ISA PnP)

Writing to this location modifies the address of the port used for reading from the ISA Plug and Play cards. Bits[7:0] are mapped as bits[9:2] of I/O READ port. The I/O READ port address bits[1:0] contain always "11b". This register is write-only and is only used in the ISA PnP mode. It cannot be written under the MB PnP mode.

6.6.2 Serial Isolation (Index=01h, ISA PnP)

A read from this register results in a switch to the "Isolation" state for the Plug and Play card, and then compares with one bit of the card ID. This register is READ-only, and used only in the ISA PnP mode.

6.6.3 Configure Control (Index=02h, ISA PnP/MB PnP)

This register is write-only. Their values are not sticky; i.e., a hardware reset will clear the bits automatically without the help of software.

Bit	Description
7-3	Reserved
2	Reset CSN to 0. This bit is only used in the ISA PnP mode, and should not be written with a "1" in the MB PnP mode.
1	Return to the "Wait for Key" state. This bit is used for both the ISA PnP and MB PnP modes when configuration sequence is completed.
0	Reset all logical devices and restore configuration registers to their power-on states. In the ISA PnP mode, writing a "1" to this bit only resets those registers that can be accessed in the ISA PnP mode.

6.6.4 Wake[CSN] (Index=03h, ISA PnP)

Writing to this port will assign all cards with a CSN to go from the "Sleep" state to either the "Isolation" state (if data[7:0]=00h) or the "Configuration" state (if data[7:0]=00h), when the CSN matches the write data[7:0]. This register is write-only, and used only in the ISA PnP mode.

6.6.5 Resource Data (Index=04h, ISA PnP)

This register is READ-only and used only in the ISA PnP mode.

6.6.6 Status (Index=05h, ISA PnP)

Bits[7:1] are reserved. Setting bit 0, it indicates ready to fetch the next data byte from the Resource Data register.

6.6.7 Card Select Number (CSN, Index=06h, Default=00h, ISA PnP)

Upon writing to this register, a card's CSN is given. A CSN is a value uniquely assigned to each ISA card after the serial identification process, so that each card may be individually selected during a WAKE[CSN] command. This register is READ/WRITE, and is only used in the ISA PnP mode.

6.6.8 Logical Device Number (LDN, Index=07h, ISA PnP/MB PnP)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical device can be accessed. In addition, the I/O RANGE CHECK and ACTIVATE commands are effective only on the selected logical devices. This register is READ/WRITE and used in both the ISA PnP and MB PnP modes.

6.6.9 Chip ID Byte 1 (Index=20h, Default=86h, MB PnP)

This register is the Chip ID byte 1 and for READ-only. Bits[7:0]=86h when read.

6.6.10 Chip ID Byte 2 (Index=21h, Default=61h, MB PnP)

This register is the Chip ID byte 2 and for READ-only. Bits[7:0]=61h when read.

6.6.11 Chip Version & Multi-Chips Clarification (Index=22h, Default=00h, MB PnP)

This register is the Chip Version. Bits 7,6,3,2,1 are reserved and READ-only. Bits 5 and 4 are writeable and used to clarify different systems that use the same IT8661F or IT8661RF I/O

controller in MB PnP mode. (Refer to the general description of configuring sequence.).

If only one IT8661F or IT8661RF chip is implemented, the configuring sequence is not affected by these two (2) bits. Bit 0 is READ only and represents the chip version, as IT8661F if set to "0" and as IT8661RF if set to "1".

6.6.12 PnP Logical Device Enable Register (Index=23h, Default=00h, MB PnP)

The logical devices will not be involved in the ISA PnP protocol sequence except when the enable bits of the PnP logical devices are set.

Bit	Description
7-5	Reserved
4	IR
3	Parallel Port
2	Serial Port 2
1	Serial Port 1
0	FDC

In the ISA PnP mode, the LDNs are dynamic. The default sequence is FDC, Serial Port 1, Serial Port 2, Parallel Port and IR. If one of the bits is not set, the corresponding LDNs of the devices after this current one are subtracted by one. For example: when 0Fh is given to bits[7:0] (PnP logical device enable: FDC, Serial Port 1, 2 & Parallel Port). By LDN mapping, we will get 00h as FDC, 01h as Serial Port 1, 02h as Serial Port 2, and 03h as Parallel Port. When 06h is given to bits[7:0] (only Serial Port 1, 2). By LDN mapping, we will get 00h as Serial Port 1, and 01h as Serial Port 2.

6.6.13 Software Suspend and Input Clock Select (Index=24h, Default=00h, MB PnP)

Bit 0 is the SOFTWARE SUSPEND. When bit 0 is set to "1", the IT8661F and IT8661RF are in the "SOFTWARE SUSPEND" state. All the devices remain inactive until this bit is cleared or the WAKE-UP event occurs. The WAKE-UP event occurs at any transition on signals RI1 (pin 84) and RI2 (pin 86). Bit 1 is for the input clock selection. When this bit is set to "0", the input clock of the IT8661F or IT8661RF is 24MHz. When set to "1", the input clock is 48MHz.

Bit	Description
7-2	Reserved
1	Input Clock Select 1 : 48MHz 0 : 24MHz
0	SOFTWARE SUSPEND 1 : Suspend 0 : Normal

6.6.14 GPIO Function Enable Registers[12:8] (Index=25h, Default=00h, MB PnP)

The bits[4:0] are mapped as the GPIO Function Enable Register[12:8]. The enable bits should be set to "1" to enable the GPIO function, otherwise, the multi-function pins will perform the original functions. Bits[7:5] are reserved. This register can be read from any LDN but can only be written if LDN=05h.

Bit	Description
7-5	Reserved
4	Enable GPIO Function 12 (pin 26)
3	Enable GPIO Function 11 (pin 25)
2	Enable GPIO Function 10 (pin 19)
1	Enable GPIO Function 9 (pin 98)
0	Enable GPIO Function 8 (pin 94)

6.6.15 GPIO Function Pin Enable Register[7:0] (Index=26h, Default=00h, MB PnP)

This register is GPIO Function Enable Register[7:0]. The enable bits should be set to "1" to enable the GPIO function, otherwise, the multi-function pins will perform the original functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	Enable GPIO Function 7 (pin 93)
6	Enable GPIO Function 6 (pin 92)
5	Enable GPIO Function 5 (pin 91)
4	Enable GPIO Function 4 (pin 90)
3	Enable GPIO Function 3 (pin 89)
2	Enable GPIO Function 2 (pin 88)
1	Enable GPIO Function 1 (pin 87)
0	Enable GPIO Function 0 (pin 86)

6.7 FDC Configuration Registers (LDN=00h)

6.7.1 FDC Activate (Index=30h, Default=00h, ISA PnP/MB PnP)

Bit	Description
7-1	Reserved
0	FDC Enable 1: enable 0: disable This is a READ/WRITE register. I/O Range Check must be disabled before it is to be set active.

6.7.2 FDC I/O Range Check (Index=31h, Default=00h, ISA PnP)

This register is used, in the ISA PnP mode, to perform a conflict check on the I/O port range programmed for FDC.

Bit	Description
7-2	Reserved
1	Enable I/O Range Check. If set, then I/O Range Check is enabled. Before set, FDC should be inactive.
0	If set, the IT8661F and IT8661RF are forced to respond with a “55h” to I/O READ of the assigned I/O range of FDC when I/O Range Check is in operation. If cleared, it then sends an “AAh” in response.

6.7.3 FDC Base Address MSB Register (Index=60h, Default=03h, ISA PnP/MB PnP)

Bit	Description
7-4	READ-only, with “0h” for Base Address[15:12]
3-0	Mapped as Base Address[11:8]

6.7.4 FDC Base Address LSB Register (Index=61h, Default=F0h, ISA PnP/MB PnP)

Bit	Description
7-3	READ/WRITE, mapped as Base Address[7:3]
2-0	READ-only as “000b”

6.7.5 FDC Interrupt Level Select (Index=70h, Default=06h, ISA PnP/MB PnP)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for FDC Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.7.6 FDC Interrupt Type (Index=71h, Default=02h, ISA PnP)

This register indicates the type of interrupt used for FDC, and is READ-only as default “02h” (to indicate the traditional interrupt type, edge trigger).

6.7.7 FDC DMA Channel Select (Index=74h, Default=02h, ISA PnP/MB PnP)

Bit	Description
7-3	Reserved with default “00h”
2-0	Select the DMA channel for FDC 7h-5h : not valid 4h : no DMA channel selected 3h : DMA3 2h : DMA2 1h : DMA1 0h : DMA0

6.7.8 FDC Special Configuration Register (Index=F0h, Default=00h, MB PnP)

Bit	Description
7-4	Reserved with default “00h”
3	1 : IRQ sharing 0 : Normal IRQ
2	1 : Swap Floppy Drives A, B 0 : Normal
1	1 : 3-mode 0 : AT mode
0	1 : Software Write Protect 0 : Normal

6.8 Serial Port 1 Configuration Registers (LDN=01h)

6.8.1 Serial Port 1 Activate (Index=30h, Default=00h, ISA PnP/MB PnP)

Bit	Description
7-1	Reserved
0	Serial Port 1 Enable 1: enable 0: disable This is a READ/WRITE register. I/O Range Check must be disabled before it is to be set active.

6.8.2 Serial Port 1 I/O Range Check (Index=31h, Default=00h, ISA PnP)

This register is used, in the ISA PnP mode, to perform a conflict check on the I/O port range programmed for Serial Port 1.

Bit	Description
7-2	Reserved with default “00h”
1	I/O Range Check 1 : enable 0 : disable Serial Port 1 must be inactive before it is to be set.
0	If set, the IT8661F and IT8661RF are forced to respond a “55h” to I/O READ of the assigned I/O range of Serial Port 1 when I/O Range Check is in operation. If cleared, it then sends an “AAh” in response.

6.8.3 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h, ISA PnP/MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.8.4 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h, ISA PnP/MB PnP)

Bit	Description
7-3	READ/WRITE, mapped as Base Address[7:3]
2-0	READ-only as “000b”

6.8.5 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h, ISA PnP/MB PnP)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for Serial Port 1 Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.8.6 Serial Port 1 Interrupt Type (Index=71h, Default=02h, ISA PnP)

This register indicates the type of interrupt used for Serial Port 1, and is READ-only as 02h (to indicate the traditional interrupt type, edge trigger).

6.8.7 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h, MB PnP)

Bit	Description
7-2	Reserved with default “00h”
1	1 : IRQ sharing 0 : normal
0	1 : MIDI support enabled 0 : MIDI support disabled

6.9 Serial Port 2 Configuration Registers (LDN=02h)

6.9.1 Serial Port 2 Activate (Index=30h, Default=00h, ISA PnP/MB PnP)

Bit	Description
7-1	Reserved
0	Serial Port 2 Enable 1: enable 0: disable This is a READ/WRITE register. I/O Range Check must be disabled before it is to be set active.

6.9.2 Serial Port 2 I/O Range Check (Index=31h, Default=00h, ISA PnP)

This register is used, in the ISA PnP mode, to perform a conflict check on the I/O port range programmed for Serial Port 2.

Bit	Description
7-2	Reserved with default “00h”
1	I/O Range Check 1 : enable 0 : disable Before set, Serial Port 2 should be inactive.
0	If set, the IT8661F and IT8661RF are forced to respond a “55h” to I/O READ of the assigned I/O range of Serial Port 2 when I/O Range Check is in operation. If cleared, it then sends an “AAh” in response.

6.9.3 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h, ISA PnP/MB PnP)

Bit	Description
7-4	READ-only with “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.9.4 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h, ISA PnP/MB PnP)

Bit	Description
7-3	READ/WRITE, mapped as Base Address[7:3]
2-0	READ-only as “000b”

6.9.5 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h, ISA PnP/MB PnP)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for Serial Port 2 Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.9.6 Serial Port 2 Interrupt Type (Index=71h, Default=02h, ISA PnP)

This register indicates the type of interrupt used for Serial Port 2, and is READ-only as “02h” (to indicate the traditional interrupt type, edge trigger).

6.9.7 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h, MB PnP)

Bit	Description
7-2	Reserved with default “00h”
1	1 : IRQ sharing 0 : normal
0	1 : MIDI support enabled 0 : MIDI support disabled

6.10 Parallel Port Configuration Registers (LDN=03h)

6.10.1 Parallel Port Activate (Index=30h, Default=00h, ISA PnP/MB PnP)

Bit	Description
7-1	Reserved
0	Parallel Port Enable 1: enable 0: disable This is a READ/WRITE register. I/O Range Check must be disabled before it is to be set active.

6.10.2 Parallel Port I/O Range Check (Index=31h, Default=00h, ISA PnP)

This register is used, in the ISA PnP mode, to perform a conflict check on the I/O port range programmed for Parallel Port.

Bit	Description
7-2	Reserved
1	I/O Range Check 1 : enable 0 : disable Parallel Port must be inactive before it is to be set.
0	If set, the IT8661F and IT8661RF are forced to respond with a “55h” to I/O READ of the assigned I/O range of Parallel Port when I/O Range Check is in operation. If cleared, it then sends an “AAh” in response.

6.10.3 Parallel Port Base Address 1 MSB Register (Index=60h, Default=03h, ISA PnP/MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.10.4 Parallel Port Base Address 1 LSB Register (Index=61h, Default=78h, ISA PnP/MB PnP)

Bit	Description
7-2	READ/WRITE, mapped as Base Address[7:2]
1-0	READ-only as “00b”

6.10.5 Parallel Port Base Address 2 MSB Register (Index=62h, Default=07h, ISA PnP/MB PnP)

This register is used only when the ECP mode is enabled.

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.10.6 Parallel Port Base Address 2 LSB Register (Index=63h, Default=78h, ISA PnP/MB PnP)

This register is used only when the ECP mode is enabled.

Bit	Description
7-2	READ/WRITE, mapped as Base Address[7:2]
1-0	READ-only as “00b”

6.10.7 Parallel Port Interrupt Level Select (Index=70h, Default=07h, ISA PnP/MB PnP)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for Parallel Port Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.10.8 Parallel Port Interrupt Type (Index=71h, Default=02h, ISA PnP)

This register indicates the type of interrupt used for the Parallel Port, and is READ-only as “02h” (to indicate the traditional interrupt type, edge trigger).

6.10.9 Parallel Port DMA Channel Select (Index=74h, Default=03h, ISA PnP/MB PnP)

Bit	Description
7-3	Reserved with default “00h”
2-0	Select the DMA channel for Parallel Port 7h-5h : not valid 4h : no DMA channel selected 3h : DMA3 2h : DMA2 1h : DMA1 0h : DMA0

6.10.10 Parallel Port Special Configuration Register (Index=F0h, Default=03h, MB PnP)

Bit	Description
7-3	Reserved with default “00h”
2	This bit is used to program the IRQ sharing function 1 : IRQ sharing enabled 0 : Normal IRQ output
1-0	Parallel Port mode 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode

If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP specification, the EPP mode cannot be enabled when bit 2 of the Parallel Port Base Address 1 LSB (index 61h) is set to “1”.

6.11 IR Configuration Registers (LDN=04h)

6.11.1 IR Activate (Index=30h, Default=00h, ISA PnP/MB PnP)

Bit	Description
7-1	Reserved
0	IR Enable 1: enable 0: disable This is a READ/WRITE register. I/O Range Check must be disabled before it is to be set active.

6.11.2 IR I/O Range Check (Index=31h, Default=00h, ISA PnP)

This register is used, in the ISA PnP mode, to perform a conflict check on the I/O port range programmed for IR.

Bit	Description
7-2	Reserved
1	Enable I/O Range Check. If set, then I/O Range Check is enabled. Before set, IR should be inactive.
0	If set, the IT8661F and IT8661RF are forced to respond with a “55h” to I/O READ of the assigned I/O range of IR when I/O Range Check is in operation. If cleared, it then sends an “AAh” in response.

6.11.3 IR Base Address 1 MSB Register (Index=60h, Default=02h, ISA PnP/MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	Mapped as Base Address[11:8]

6.11.4 IR Base Address 1 LSB Register (Index=61h, Default=E8h, ISA PnP/MB PnP)

Bit	Description
7-3	READ/WRITE, mapped as Base Address[7:3]
2-0	READ-only as “000b”

6.11.5 IR Base Address 2 MSB Register (Index=62h, Default=03h, ISA PnP/MB PnP) (IT8661RF only)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.11.6 IR Base Address 2 LSB Register (Index=63h, Default=00h, ISA PnP/MB PnP) (IT8661RF only)

Bit	Description
7-3	READ/WRITE, mapped as Base Address[7:3]
2-0	READ-only as “000b”

6.11.7 IR Interrupt Level Select 1 (Index=70h, Default=0Ah, ISA PnP/MB PnP)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for Parallel Port Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.11.8 IR Interrupt Type 1 (Index=71h, Default=02h, ISA PnP)

This register indicates the type of interrupt used for IR, and is READd-only as “02h” (to indicate the traditional interrupt type, edge trigger).

6.11.9 IR Interrupt Level Select 2 (Index=72h, Default=0Bh, ISA PnP/MB PnP) (IT8661RF only)

Bit	Description
7-4	Reserved with default “0h”
3-0	Select the interrupt level for Parallel Port Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.11.10 IR Interrupt Type 2 (Index=73h, Default=02h, ISA PnP) (IT8661RF only)

This register indicates the type of interrupt used for IR, and is READ-only as “02h” (to indicate the traditional interrupt type, edge trigger).

6.11.11 IR DMA Channel Select 1 (Index=74h, Default=01h, ISA PnP/MB PnP) (IT8661RF only)

Bit	Description
7-3	Reserved with default “00h”
2-0	Select the DMA channel for Parallel Port 7h-5h : not valid 4h : no DMA channel selected 3h : DMA3 2h : DMA2 1h : DMA1 0h : DMA0

6.11.12 IR DMA Channel Select 2 (Index=75h, Default=00h, ISA PnP/MB PnP) (IT8661RF only)

Bit	Description
7-3	Reserved with default “00h”
2-0	Select the DMA channel for Parallel Port 7h-5h : not valid 4h : no DMA channel selected 3h : DMA3 2h : DMA2 1h : DMA1 0h : DMA0

6.11.13 IR Special Configuration Register (Index=F0h, Default=00h, MB PnP)

Bit	Description
7-6	Reserved
5	This bit is used to program the IRQ sharing function 1 : IRQ sharing enabled 0 : Normal IRQ output
4	SIR Mode Select 1 : ASKIR 0 : HPSIR (This bit is available for IT8661F only.)
3	1 : Half Duplex for SIR or ASKIR 0 : Full Duplex for SIR or ASKIR
2	1 : Dual DMA Channel One DMA channel is for transmitting and the other one is for receiving. 0 : Single DMA Channel This DMA channel is for both transmitting and receiving. (This bit is available for IT8661RF only.)
1	1 : Dual Interrupt Level One interrupt level is for FIR mode and the other one is for MIR mode. 0 : Single Interrupt Level This interrupt level is for both FIR and MIR modes. (This bit is available for IT8661RF only.)
0	FIR Transceiver Mode Select 1 : 2 Input Transceiver (HP-Like) 0 : 1 Input Transceiver (IBM-Like) (This bit is available for IT8661RF only.)

6.12 GPIO & Alternate Function Configuration Registers (LDN=05h)

6.12.1 CS0 Base Address MSB Register (Index=60h, Default=00h, MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.12.2 CS0 Base Address LSB Register (Index=61h, Default=00h, MB PnP)

Bit	Description
7-0	READ/WRITE, mapped as Base Address[7:0]

6.12.3 CS1 Base Address MSB Register (Index=62h, Default=00h, MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.12.4 CS1 Base Address LSB Register (Index=63h, Default=00h, MB PnP)

Bit	Description
7-0	READ/WRITE, mapped as Base Address[7:0]

6.12.5 CS2 Base Address MSB Register (Index=64h, Default=00h, MB PnP)

Bit	Description
7-4	READ-only as “0h” for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.12.6 CS2 Base Address LSB Register (Index=65h, Default=00h, MB PnP)

Bit	Description
7-0	READ/WRITE, mapped as Base Address[7:0]

6.12.7 Simple I/O Base Address MSB Register (Index=66h, Default=00h, MB PnP)

Bit	Description
7-4	READ-only as "0h" for Base Address[15:12]
3-0	READ/WRITE, mapped as Base Address[11:8]

6.12.8 Simple I/O Base Address LSB Register (Index=67h, Default=00h, MB PnP)

Bit	Description
7-0	READ/WRITE, mapped as Base Address[7:0]

6.12.9 GPIO Interrupt Level Select (Index=70h, Default=00h, MB PnP)

This register is used to program the pin type as either a simple inverting or non-inverting for GPIO [7:0].

Bit	Description
7-4	See Pin Location[note] on page 28.
3-0	Select the interrupt level for GPIO Fh-Ch : not valid Bh : IRQ11 . . 3h : IRQ3 2h : not valid 1h : not valid 0h : no interrupt selected

6.12.10 GPIO[7:0] Pin Polarity Register (Index=F0h, Default=00h, MB PnP)

Bit	Description
7-0	For each bit 1 : inverting 0 : non-inverting

6.12.11 CS0/CS1/CS2 Control Register (Index=F1h/F2h/F3h, Default=00h, MB PnP)

Bit	Description
7-6	Base Address Alignment 00 : single port 01 : 2 ports 10 : 4 ports 11 : 8 ports
5-4	Chip Select Type 00 : Pure Address Decode 01 : Address Decode and IOR command 10 : Address Decode and IOW command 11 : Address Decode and (IOR or IOW command)
3-0	See Location[note] on page 28.

6.12.12 GPIO[7:0] Function Selection Register (Index=F4h, Default=00h, MB PnP)

This register is used to select the function to be either the Simple I/O or the Alternate function.

Bit	Description
7-0	For each bit 1 : Simple I/O 0 : Alternate function

6.12.13 Simple I/O[7:0] Direction Selection Register (Index=F5h, Default=00h, MB PnP)

This register is used to determine the direction of the Simple I/O.

Bit	Description
7-0	For each bit 1 : Input mode 0 : Output mode

6.12.14 Zero Wait State Control & On-Chip High Address Qualification Enable Register (Index=F6h, Default=00h, MB PnP)

Bit	Description
7-6	Reserved
5	This bit is used to program the IRQ sharing function 1 : IRQ sharing enabled 0 : Normal IRQ output
4	This bit is used to enable or disable the GPIO pin to be as high address SA[15:12] input pin for 16-bit address decoding 0 : disable on-chip high address qualification 1 : enable on-chip high address qualification
3-0	See Location[note] of Zero Wait State function on page 28.

6.12.15 Device Zero Wait State Enable Register (Index=F7h, Default=00h, MB PnP)

This register is used to determine which device is enabled in the ZWS function. The bits should be set to "1" to enable the ZWS function.

Bit	Description
7	GPIO (Simple I/O, CS0, CS1, CS2)
6	Reserved
5	Reserved
4	EPP Port (Parallel Port Base Address + 3h~7h)
3	SPP & ECP Port
2	Serial Port 2
1	Serial Port 1
0	FDC

6.12.16 GPIO[12:8] Pin Polarity Register (Index=F8h, Default=00h, MB PnP)

This register is used to program the GPIO[12:8] pin type as polarity inverting or non-inverting for GPIO[12:8].

Bit	Description
7-5	Reserved
4-0	For each bit 1 : inverting 0 : non-inverting

6.12.17 GPIO[12:8] Function Selection Register (Index=F9h, Default=00h, MB PnP)

This register is used to select the function as to be either the Simple I/O or Alternate function.

Bit	Description
7-5	Reserved
4-0	For GPIO[12:8] 1 : Simple I/O 0 : Alternate function

6.12.18 Simple I/O[12:8] Direction Selection Register (Index=FAh, Default=00h, MB PnP)

This register is used to determine the direction of the Simple I/O[12:8].

Bit	Description
7-5	Reserved
4-0	For each bit 1 : Input mode 0 : Output mode

6.12.19 High Address Qualification Inputs 1 & 2 Selection Register (Index=FBh, Default = 00h, MB PnP)

This register is used to program the Pin location of high address inputs 1 and 2 for 16-bit address decoding.

Bit	Description
7-4	See Location[note] of high address input 2 below.
3-0	See Location[note] of high address input 1 below.

6.12.20 High Address Qualification Inputs 3 & 4 Selection Register (Index=FCh, Default = 00h, MB PnP)

This register is used to program the Pin location of high address inputs 3 and 4 for 16-bit address decoding.

Bit	Description
7-4	See Location[note] of high address input 4 below.
3-0	See Location[note] of high address input 3 below.

Note: The Location mapping

Location	Description
0000	None
0010	GPIO 8 (pin 94)
0100	GPIO 9 (pin 98)
0110	GPIO 10 (pin 19)
1000	GPIO 11 (pin 25)
1010	GPIO 12 (pin 26)
0001	GPIO 0 (pin 86)
0011	GPIO 1 (pin 87)
0101	GPIO 2 (pin 88)
0111	GPIO 3 (pin 89)
1001	GPIO 4 (pin 90)
1011	GPIO 5 (pin 91)
1101	GPIO 6 (pin 92)
1111	GPIO 7 (pin 93)
else	Reserved

7. Functional Description

7.1 General Purpose I/O

The IT8661F and IT8661RF provide a set of flexible I/O control and special functions for system designers through a set of General Purpose I/O pins (GPIO). All thirteen (13) GPIO pins are multi-function pins. They will not perform GPIO functions unless the bits of the GPIO function pin enable registers (Index 25h & 26h of Global Configuration Register) are set. GPIO functions include the Simple I/O function and the Alternate function.

The Simple I/O function includes a set of registers, which corresponds to the GPIO pins. All control bits are divided into two (2) registers (Simple I/O 1, GPIO[7:0]; Simple I/O 2, GPIO[12:8]). The accessed I/O ports are programmable and are two consecutive I/O ports (Base Address & Base Address+1). Base Address is programmed on the registers of GPIO Alternate Function (LDN=05h, Index=66h & 67h).

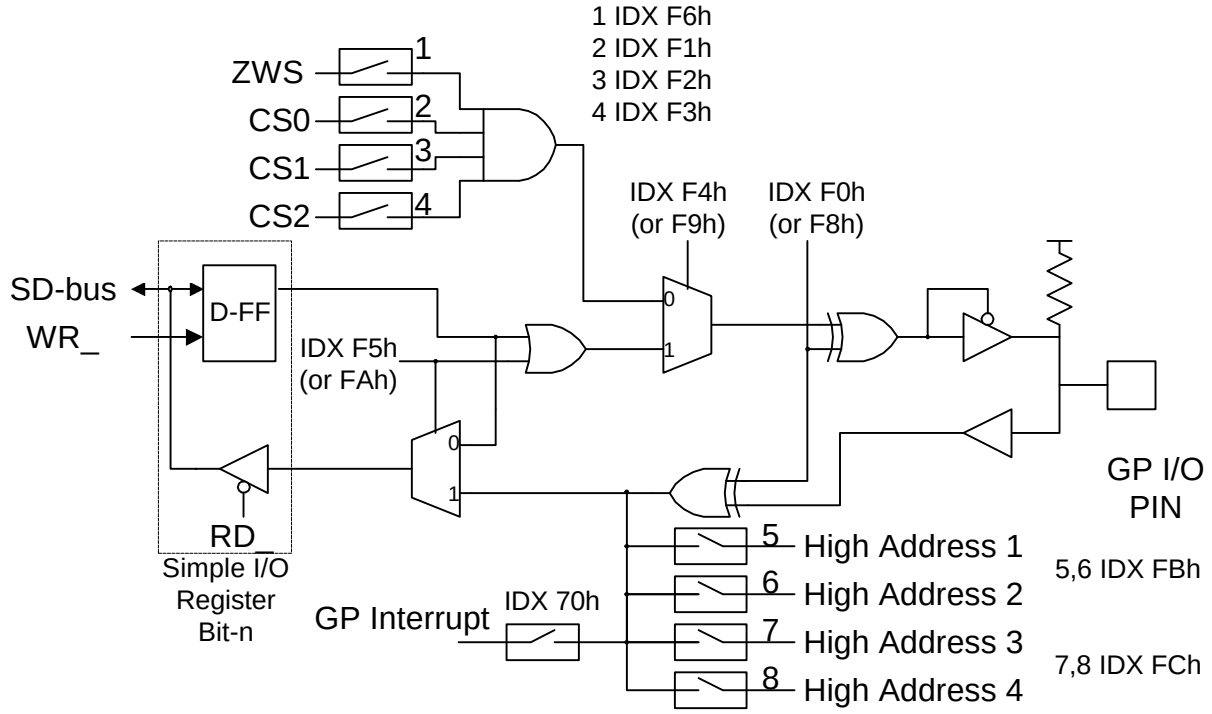
The Alternate Function provides several special functions for use, including three (3) chip select strobes (CS0, CS1, CS2), Zero Wait State, Interrupt level mapping, and On-chip High Address SA[15:12] Qualification. All functions can be programmed to all thirteen (13) GPIO pins. There are three (3) registers that should be programmed to enable an alternate function, Index 26h (or 25h) and F4h (or F9h) or LDN 05h and pin location bits of each Alternate function.

In IT8661F and IT8661RF, there are flexible control register related to each of the three (3) chip select strobes (Index F1h, F2h, F3h, LDN 05h). Each can be programmed as 1 or 2 or 4 or 8 by consecutive I/O port decoding. It can also be programmed to qualify with IOR# and IOW# states. There are four (4) types of qualifying conditions: pure address decided, asserted on address matching and IOR# asserted, asserted on address matching and IOW# asserted, asserted on address matching and IOR# or IOW# asserted.

The Zero Wait State function is used to reduce the cycle time of the ISA bus when the IT8661F and IT8661RF are accessed. The IT8661F and IT8661RF provide a set of enable registers for the logical devices which are activated with Zero Wait State function when they are accessed. By programming this register, users can select the logical devices which are fast enough to set the Zero Wait State of the ISA bus.

The Interrupt level mapping function provides a useful feature for the motherboard designer. Through this mapping, the interrupt level of other on-board devices can be easily changed by software. The programming method is to set the related bits on the registers Index 26h (or 25h), F4h (or F9h) and F5h (or FAh). The pin location mapping, Index 70h must be also programmed correctly.

The on-chip high address SA[15:12] qualification for 16-bit address decoding function provides a useful feature for the system designer to design full 16-bit address decoding without any additional TTL. The programming method is to set the related bits on register index 26h (or 25h), F4h (or F9h) and bit 4 of index F6h to enable this function. Index FBh and FCh are used to determine the pin location of these four (4) input high addresses.



Note: All GPIO pins are internally pulled up 50 KΩ except GPIO10 (pin 19).

Figure 7-1. General Logic of GPIO Function

7.2 FDC Register Description

7.2.1 Digital Output Register (DOR) - (Base Address + 02h)

This register controls drive selection and drive motor. The I/O interface reset may be used at any time to clear DOR's contents.

Table 7-1. Digital Output Register (DOR)

Bit	Symbol	Description
7	-	Reserved
6	-	Reserved
5	MOTB EN	Drive B Motor Enable bit, active high
4	MOTA EN	Drive A Motor Enable bit, active high
3	DMAEN	Disk Interrupt and DMA Enable bit, active high
2	RESET#	FDC Function Reset bit, active low. This reset doesn't affect DSR, CCR and DOR.
1	-	Reserved
0	DVSEL	Drive Selection. When it is low, select drive A. When it is high, select drive B

7.2.2 Main Status Register (MSR) - (Base Address + 04h)

This register indicates the disk controller status. It should be read before each byte is sent to or received from the data register, except when in DMA mode.

Table 7-2. Main Status Register (MSR)

Bit	Symbol	Description
7	RQM	Request for Master When this bit is set high, the host can transfer data.
6	DIO	Data Input/Output bit Indicates the direction of data transfer once a RQM is set. Logic 1 = READ. Logic 0 = WRITE.
5	NDM	Non-DMA Mode Active high. This bit is used with the SPECIFY command.
4	CB	Diskette Control Busy Is set active (high) during the execution of a command, and inactive (low) at the end of the result phase.
3	-	Reserved
2	-	Reserved
1	DBB	Drive B Busy Is set high when drive B is in the SEEK portion of a command.
0	DAB	Drive A Busy It is set high when drive A is in the SEEK portion of a command.

7.2.3 Data Register (FIFO) - (Base Address + 05h)

This 8-bit data register actually consists of several registers in a stack, and only one register is presented to the data bus at a time when storing data commands and parameters, or providing diskette-drive status information.

7.2.4 Digital Input Register (DIR) - (Base + 07h)

Table 7-3. Digital Input Register (DIR)

Bit	Symbol	Description
7	DSKCHG	Diskette Change bit Indicates the inverting value of which is monitored from the input of the Diskette Change pin (DSKCHG#)
6-0		Undefined, high-impedance while being read

7.2.5 Diskette Control Register (DCR) - (Base Address + 07h WRITE)

The transfer rate register is a 2-bit, READ-only register which controls a programmable divider and provides 16/ 8/ 4.8/ 4 MHz clocks for four (4) different data transfer rates. The bits are defined below:

Table 7-4. Diskette Control Register (DCR)

Bit 0	Bit 1	Transfer Rates	Clock Rates	Reduce Write
0	0	500K bps	8 MHz	0
1	0	300K bps	4.8 MHz	1
0	1	250K bps	4 MHz	1
1	1	1M bps	16 MHz	1

7.2.6 Status Register

These 4-byte READ-only registers indicate the status of some determined commands that have been executed during their result phase. Their contents are described in the tables below:

Table 7-5. Status Register 0

Bit	Symbol	Name	Description
7, 6	IC	Interrupt Code	00 - Execution of the command is completed and correct 01 - Execution of the command was begun, but not successfully completed 10 - INVALID command 11 - The execution of the command is not correctly completed, caused by polling
5	SE	Seek End	The FDC executes a SEEK, RELATIVE SEEK or RE-CALIBRATE command.
4	EC	Equipment Check	The TRK00# pin cannot be active after a RE-CALIBRATE command is issued, or when the FDC steps outward beyond track 0 with a relative command.
3	NR	Not Ready	Not Ready
2	H	Head Address	The current head address
1	DSB	Drive B Select	Select drive B
0	DSA	Drive A Select	Select drive A

Table 7-6. Status Register 1

Bit	Symbol	Name	Description
7	EN	End of Cylinder	FDC attempts to access a sector beyond the final sector of the track. If TC is not issued after READ or WRITE DATA commands, it will be set.
6	-	-	Unused, always 0
5	DE	Data Error	A CRC error occurs in the ID field or the data field is detected by FDC.
4	OR	Overrun/ Underrun	Overrun on a READ operation or Underrun on a WRITE operation is caused by an insufficient time interval for the CPU or DMA to service the FDC.
3	-	-	This bit is always "0."
2	ND	No Data	1. FDC cannot find the indicated sector during the READ DATA or READ DELETED DATA commands. 2. While executing a READ ID command, an error occurs upon reading the ID field. 3. While executing a READ TRACK command, the FDC cannot find the starting sector.
1	NW	Not Writeable	Activated when a WRITE or FORMAT Command is being executed on a WRITE-protected diskette.
0	MA	Missing Address Mark	1. The FDC cannot find a data address mark on the specified track or Deleted Data Address mark. 2. The FDC cannot find any ID address on the specified track after two (2) index pulses are detected from the INDEX # pin.

Table 7-7. Status Register 2

Bit	Symbol	Name	Description
7	-	-	Unused, this bit is always "0."
6	CM	Control Mark	When the FDC finds a Delete Data Address mark with a READ DATA or SCAN command, this flag bit is set.
5	DD	Data Error in Data Field	When a CRC error is found in the data field, this flag bit is set.
4	WC	Wrong Cylinder	The track address in the ID field is different from the track address specified in the FDC.
3	SH	Scan Equal Hit	When the condition of "equal" is satisfied with a SCAN command, this flag bit is set.
2	SN	Scan Not Satisfied	When FDC cannot find a sector on the cylinder with a SCAN command, this flag bit is set.
1	BC	Bad Cylinder	The track address FFh is different from the track address in the FDC.
0	MD	Missing Data Address Mark	The Data Address Mark or Deleted Data Address Mark cannot be found by FDC.

Table 7-8. Status Register 3

Bit	Symbol	Name	Description
7	FT	Fault	The status of the Fault signal from the FDD
6	WP	Write Protect	The status of the Write Protected signal from the FDD
5	RDY	Ready	The status of the Ready signal from the FDD
4	TK0	Track 0	The status of the Track 0 signal from the FDD
3	TS	Two Side	The status of the Two Side signal from the FDD
2	HD	Head Address	The status of the Side Select signal to the FDD
1	US1	Unit Select. Indicates the current status of the Unit Select signals to FDD.	
0	US0		

7.2.7 Reset

The IT8661F and IT8661RF implement two (2) types of reset on FDC: software and hardware. Either will perform FDC RESET, releasing the FDC to idle state. Attempting a RESET while writing to the disk will cause corruption of data and CRC.

(1) Hardware Reset (Reset Pin)

With this RESET, all registers of the FDC CORE are cleared (except those programmed by the SPECIFY Command). To exit the RESET state, the DOR bit must be cleared by the host.

(2) Software Reset (DOR reset and DSR reset)

The difference between DOR and DSR is that DSR is self-clearing, while DOR must be cleared by the host in order to exit the RESET state. The DOR reset has higher priority than the DSR RESET.

7.2.8 Controller Phases

There are three (3) controller phases in the FDC: Command phase, Execution phase, and Result phase.

(1) Command Phase

When FDC accepts a command from the host before this phase finishes, a set of command-code bytes and parameter bytes have to be given in the order that the FDC requires. The FDC READ step is enabled only if MSR(7)=1 and MSR(6)=0 (RQM and DIO bit). RQM is set false after each byte-READ cycle, and set true again when a new parameter byte is required, continuing in the READ state while the READ step remains 0.

(2) Execution Phase

This phase can be completed by the SPECIFY command in DMA or NON-DMA modes. By using the CONFIGURE command, FIFO can automatically be enabled and disabled after each RESET.

(3) Result Phase

This phase begins when the IRQx pin is activated. The defined set of result bytes must be read by the Host before this phase can be completed. Before the FDC starts to read data, RQM and DIO must be set high. When the READ step ends, RQM=1, DIO=0, and CB bit is cleared.

7.2.9 Data Transfer Commands Description

All DATA TRANSFER commands utilize the same parameter bytes and return the same result data byte, differentiating between them only in the five (5) bits (0~4) of the first byte. By sending a CONFIGURE Command, the user transparent implied seek can be enabled. During execution of the SEEK, the Drive Busy bit in MSR is active; if the SEEK fails, the Status Register 0 will contain the error code and the current cylinder will be indicated by the symbol C.

Table 7-9. Command Symbol Description

Symbol	Name	Description
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 =0) or Data Register (A_0 =1).
C	Cylinder Number	C stands for the current/selected cylinder (track) number 0 through 76 or the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7 - D_0	Data Bus	8-bit Data Bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During a READ or WRITE operation FDC will stop data transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During READ/WRITE commands, this value determines the number of bytes that VCOs will stay low after two CRC bytes. During the FORMAT command it determines the size of Gap 3.
H	Head Address	H stands for Head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected Head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the Head Unload Time after a READ or WRITE operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT=1 after finishing READ/WRITE operation on side 0, FDC will automatically start searching for sector one on side one.
N	Number	N stands for the number of data bytes written in sector.
NCN	New Cylinder Number	NCN stands for a new cylinder number, which is going to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the sector number, which will be read or written.
R/W	READ/WRITE	R/W stands for either READ (R) or WRITE (W) signal.
SC	Sector	SC indicates the number of sectors per cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives. (F=1 ms, E=2 ms, etc.)

Table 7-9. Command Symbol Description (cont'd)

Symbol	Name	Description
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stands for one (1) of four (4) registers which stores the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$); ST 0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

(1) READ DATA

This mode is set by nine command bytes. Each READ operation is initialized by a READ command and finished by reading the data from FIFO through FDC. The sector address automatically increases by one (1) and the data from the next sector is read and sent through the FIFO.

This continuous function is called a "Multi Sector READ Operation". When a TC or an implied TC is received, the FDC stops sending data, but continues to read data from the current sector. In addition, it checks the CRC bytes until the READ operation is completed to the end of the sector.

The sector size is determined by the N value, from the following formula : sector size = $2^{(7+N\ value)}$ bytes. If the sector size is 128 and the DTL is less, the remaining bytes will be read and checked for CRC error by the FDC. If this occurs in a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128, (N > 00), the DTL should be set to FFh. The MT (multi-track) allows the FDC to read both sides of the diskette.

Both N and MT determine the amount of data, as indicated in table below:

Table 7-10. Effects of MT and N Bits

MT	N	Maximum Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 at side 0 or 1
1	1	256 X 52 = 13312	26 at side 1
0	2	512 X 15 = 7680	15 at side 0 or 1
1	2	512 X 30 = 15360	15 at side 1
0	3	1024 X 8 = 8192	8 at side 0 or 1
1	3	1024 X16 =16384	16 at side 1

Table 7-11. Description of the READ DATA Command

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

(2) READ DELETED DATA

The READ DELETED DATA command is identical to the READ DATA provided in the previous section except for operation on sectors which have a Deleted Data Address Mark at the beginning of a data field.

Table 7-12. Description of the READ DELETED DATA Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information before the command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and the main system.
Result	R				ST0					Status information after command execution
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

(3) READ A TRACK

After receiving a pulse from the INDEX# pin, this READ A TRACK command reads the entire data field from each sector of the track as continuous blocks. If any ID or Data CRC error is found, it continues to read data from the track and indicates the error at the end. Because the MT operation is not allowed with this command, the MT and SK bits should be low during command execution.

This command normally terminates when the number of sectors specified by EOT has not been read. After the second occurrence of the INDEX pulse, provided that any ID Address Mark has been found, the FDC will set the IC code in ST0 to 01, indicating an abnormal termination, then finishes this command.

Table 7-13. Description of the READ A TRACK Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	SK	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system cylinder contents from index hole to EOT.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

(4) WRITE DATA

Each WRITE operation begins with a WRITE DATA command and terminates when data is written into the sector data field, from the host via the FIFO. After, the FDC computes the CRC value and stores it in the CRC field. The sector number in "R" is incremented by one, and the next data operation is performed (Multi Sector WRITE Operation). During this operation, when a terminal count signal or an over/underrun occurs, the remaining data field is filled with 0s. The operation of WRITE DATA command is similar to that of READ DATA command in many aspects, such as transfer capacity, end of the cylinder bit, no data bit, and ID information. The definition of DTL for those cases in N is the same as "no" or 0, etc.

Table 7-14. Description of the WRITE DATA Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

(5) WRITE DELETED DATA

This command is the same as the WRITE DATA command, except a Deleted Data Address Mark is written at the beginning of the data field.

Table 7-15. Description of the WRITE DELETED DATA Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

(6) FORMAT A TRACK

This command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the gaps, address marks, ID fields, and data fields. The gaps and data field values are controlled by the host-specified values programmed into N, SC, GPL, and D. The data field is filled with the data byte specified by D. Four data bytes per sector of the ID field: C, H, R, and N are supplied by the host. The C, R, H, and N values must be renewed for every new sector of a track. Only the R value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps will continue until a new INDEX pulse or the command terminal signal is received.

Table 7-16. Description of the FORMAT A TRACK Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								

Control Commands

A special feature of these commands is that they don't transfer any data. Only three (3) generate interrupts when finished (READ ID, RE-CALIBRATE, and SEEK).

(7) READ ID

This command, used to find the actual recording head position, stores at the same time as it reads the first ID field value into the FDC registers. If this doesn't occur even when the second INDEX pulse is issued, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

Table 7-17. Description of the READ ID Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R				ST0					Status information after command execution
	R				ST1					
	R				ST2					
	R				C					Sector ID information during execution phase
	R				H					
	R				R					
	R				N					

(8) RE-CALIBRATE

This command retracts the READ/WRITE head to the track 0 position, resetting the value of the PCN counter and checking the TK00# status. If TK00# is low the DIR# pin remains low; if TK00# is high, SE and EC bits are set high, and the command is finished. When TK00# remains low for 77 step pulses, the command is terminated by setting SE and EC bits as described previously. Because of this, if the disk can accommodate more than 80 tracks, more than one RE-CALIBRATE command will be needed to retract the head to the physical track 0.

Table 7-18. Description of the RE-CALIBRATE Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0

(9) SEEK

This command controls the READ/WRITE head movement from one track to another. FDC compares PCN's current head position and NCN values after each step pulse to determine the head movement direction, as the following:

PCN < NCN: sets direction signal to 1 and issues step pulses

PCN > NCN: sets direction signal to 0 and issues step pulses

The impulse rate of step pulse is controlled by Stepping Rate Time in the SPECIFY command. The SEEK command will terminate by setting SE to 1 when the comparison result is PCN = NCN.

For the parallel SEEK operation, the FDC returns to Non-Busy State after the command phase (in Busy State), allowing another SEEK or RE-CALIBRATE command to be issued. Since the SEEK command doesn't have a result phase, it is recommended that a SENSE INTERRUPT command be issued after each SEEK command, providing verification of the head position.

Table 7-19. Description of the SEEK Command

PHASE	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

(10) SENSE INTERRUPT STATUS

This command resets the interrupt signal, and can identify the cause of interrupt via IC code and SE bit of ST0, as shown in the table below:

Table 7-20. Interrupt Identification of the SENSE INTERRUPT STATUS Command

Interrupt Identification		
SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of SEEK or RE-CALIBRATE command
1	01	Abnormal termination of SEEK or RE-CALIBRATE command

It may be necessary to generate an interrupt under the following conditions:

- Before any DATA TRANSFER or READ ID command
- After SEEK, RELATIVE SEEK, or RE-CALIBRATE command (no result phase exists)
- When a DATA TRANSFER is required during an execution phase in the non-DMA mode

Table 7-21. Description of the SENSE INTERRUPT STATUS Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end
	R	PCN								of each seek operation

(11) Sense Drive Status

This non-execution phase command provides the drive status information which is saved in ST3 (Status Register 3).

Table 7-22. Description of the SENSE DRIVE STATUS Command

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

(12) SPECIFY

The initial values of the HUT (Head Unload Time), HLT (Head Load Time) and SRT (Step Rate Time) are individually set by this command, as shown in the following table:

Table 7-23. Description of the SPECIFY Command

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

(13) INVALID

If an undefined command is sent to the FDC, then the FDC will terminate the command without interrupt. Bit 6 and bit 7 in the Main Status Register are both high. When the CPU reads Status Register 0 it will find an 80H.

Table 7-24. Description of the INVALID Command

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	invalid codes								INVALID Command Codes (NOOP - FDC goes into stand by state)
Result	R	ST0								STO = 80

7.3 Serial Channel Register Description

The IT8661F and IT8661RF incorporate two (2) enhanced serial channels which perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Individually, they contain a programmable baud rate generator which is capable of dividing the input clock by a number from 1 to 65535; the data rate of each can also be programmed from 115.2K baud to 50 baud. The character options are programmable for one (1) start bit; 1, 1.5 or two (2) stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 7-25. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

7.3.1 Data Register

TBR and RBR each hold from five (5) to eight (8) data bits. If the transmitted data is fewer than eight (8) bits, it aligns to the LSB. Either received or transmitted data is buffered by a shift register, and is latched first by a holding register. The bit 0 of any word is first received and transmitted.

(1) RBR (READ only)

This register receives and holds the entering data. It contains a non-accessible shift register which converts the incoming serial data stream to a parallel 8-bit word.

(2) TBR (WRITE only)

This register holds and transmits the data via a non-accessible shift register. It converts the outgoing parallel data to a serial stream before transmission.

7.3.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR, MCR

(1) IER (READ/WRITE)

IER is used to enable (or disable) four (4) active high interrupts which activate the interrupt outputs, with its lower four (4) bits: IER(0), IER(1), IER(2), and IER(3).

IER(4)~IER(7): These bits are always "0".

IER(3): Set this bit high to enable the Modem Status Interrupt when one of the Modem Status Registers changes its bit state.

IER(2): Set this bit high to enable the Receiver Line Status Interrupt which is caused when Overrun, Parity, Framing or Break occurs.

IER(1): Set this bit high to enable the Transmitter Holding Register Empty Interrupt.

IER(0): Set this bit high to enable the Received Data Available Interrupt (and Time-out Interrupt in the FIFO mode).

(2) IIR (READ only)

This register facilitates the host CPU to determine interrupt priority and its source. The priority of four (4) existing interrupt levels is as follows:

1. Received Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the highest priority pending interrupts to the Host. Any new interrupts will not be acknowledged until the Host access finishes. The contents of the IIR are described in the table below:

Table 7-26. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR READ
0	1	0	0	Second	Received Data Available	Received Data Available	RBR READ or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication		RBR READ
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	IIR READ if THRE is the Interrupt Source or THR WRITE
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, RSLD#	MSR READ

Note: X = Not Defined

IIR(6), IIR(7): Are set when FCR(0) = 1.

IIR(4), IIR(5): Always logic 0.

IIR(3): In non-FIFO mode, this bit is a logic 0. In the FIFO mode this bit is set along with bit 2 when a time-out Interrupt is pending.

IIR(1), IIR(2): Are used to identify the highest priority pending interrupt.

IIR(0): Is used to indicate a pending interrupt in either a hard-wired prioritized or polled environment, with a logic 0 state. When this happens, IIR contents may be used as a pointer to the appropriate interrupt service routine.

(3) FCR (WRITE only)

This register is used to enable, clear the FIFO, and set the RCVR FIFO trigger level.

FCR(6), FCR(7): These bits set the trigger levels for the RCVR FIFO interrupt.

FCR(4), FCR(5): Reserved.

FCR(3): This bit doesn't affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.

FCR(2): This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 by a logic "1".

FCR(1): Setting this self-clearing bit to logic 1 clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).

FCR(0): XMIT and RCVR FIFO are enabled when this bit is set high. XMIT and RCVR FIFO's will be disabled and cleared when this bit is cleared to low. This bit has to be a logic 1 if the other bits of the FCR are written to or they will not be properly programmed. When this register changes to non-FIFO mode, all contents will be cleared.

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches

There are two (2) 8-bit Divisor Latches (DLL and DLM) which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking, with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor range from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

(5) Scratch Pad Register (READ/WRITE)

This 8-bit register does not control the operation of UART in any way. It is intended as a scratch pad register to be used by programmer to temporarily hold general purpose data.

Table 7-27. Baud Rates Using (24MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) LCR (READ/WRITE)

LCR controls the format of the data character and gives the information of the serial line. Its contents are:

LCR(7): Divisor Latch Access Bit
LCR(6): Break Control
LCR(5): Stick Parity Bit
LCR(4): Even Parity Select (EPS)
LCR(3): Parity Enable (PEN)
LCR(2): Stop Bit Select (STB)
LCR(1): Word Length Select Bit 1 (WLS 1)
LCR(0): Word Length Select Bit 0 (WLS 0)

LCR(7): Must be set high to access the Divisor Latches of the baud rate generator

during READ or WRITE operations. It must be set low to access the Data Register (RBR and TBR) or the Interrupt Enable Register.

LCR(6): Forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and will remain until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.

LCR(5): When this bit and LCR(3) are high at the same time, the parity bit is transmitted and then detected by receiver, in opposite state by LCR(4) to force the parity to a known state and to check the parity bit in a known state.

LCR(4): When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.

LCR(3): A parity bit, between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.

LCR(2) specifies the number of stop bits in each serial character, summarized as follows:

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

LCR(0) and LCR(1): Specify the number of bits in each serial character, encoded as the following.

LCR (1)	LCR (0)	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

(7) MCR (READ/WRITE)

Controls the interface with the modem or data set (or device emulating a modem).

Table 7-28. Modem Control Register Bits

MCR Bits	Logic 1	Logic 0
MCR(7) 0		
MCR(6) 0		
MCR(5) 0		
MCR(4) Loop	Loop Enabled	Loop Disabled
MCR(3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR(2) 0		
MCR(1) Request to Send (RTS#)	RTS# Output Low	RTS# Output High
MCR(0) Data Terminal Ready (DTR#)	DTR# Output Low	DTR# Output High

MCR(5)~MCR(7): Are always low.

MCR(4): Provides a loopback feature for a diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and RLSD#) are disconnected, the four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high. The transmitted data is immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.

MCR(3): Is the Output 2 bit and enables the serial port interrupt output by a logic 1.

MCR(2): Controls the Output 1 bit, which does not have an output pin and can only be read or written by the CPU.

MCR(1): Controls the Request to Send (RTS#) which is in an inverse logic state with that of MCR(1).

MCR(0): Controls the Data Terminal Ready (DTR#) which is in an inverse logic state with that of the MCR(0).

7.3.3 Status Register LSR and MSR

(1) LSR (READ/WRITE)

This register provides status indications and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

LSR(7): In 16450 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads LSR, if there are no subsequent errors in the FIFO.

LSR(6): This READ-only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty, otherwise, this bit is "0". It has the same function in the FIFO mode.

LSR(5): Transmitter Holding Register Empty (THRE). This READ-only bit indicates that the TBR is empty and ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty and it is cleared when at least one (1) byte is written to the XMIT FIFO.

LSR(4): Break Interrupt (BI) status bit which indicates that the last character received was a break character, (invalid but entire character), including parity and stop bits. This happens when the received data input is held

in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be produced in the IIR, with the IER(2) previously enabled.

LSR(3): Framing Error (FE) bit, a logic 1, indicates that the stop bit in the received character was not valid. It resets low when the CPU reads the contents of LSR.

LSR(2): Indicates the parity error (PE) with a logic 1 indicating that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever the LSR is read by CPU.

LSR(1): Overrun Error (OE) bit which indicates by a logic 1 that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the LSR is read by the CPU.

LSR(0): Data Ready (DR) bit logic "1", which indicates a character has been received by RBR, and logic "0" indicating all of the data in RBR or RCV FIFO has been read.

Table 7-29. Line Status Register Bits

LSR Bits	Logic 1	Logic 0
LSR(7) PE/FE/BI (FIFO mode)	**Error**	No error
LSR(6) Transmitter Empty(TEMT)	**Empty**	Not empty
LSR(5) Transmitter Holding Register Empty(THRE)	**Empty**	Not empty
LSR(4) Break Interrupt(BI)	**Break**	No break
LSR(3) Framing Error(FE)	**Error**	No error
LSR(2) Parity Error(PE)	**Error**	No error
LSR(1) Overrun Error(OE)	**Error**	No error
LSR(0) Data Ready(DR)	**Ready**	Not ready

(2) MSR (READ/WRITE)

This 8-bit register provides the current state of the control lines from modems or peripheral devices. In addition to this current state information, four (4) of these eight (8) bits MSR(4) - MSR(7) can provide change information when a modem control input changes state. It will be reset to low when the Host reads the MSR.

MSR(7): Receive Line Signal Detect - Indicates the complement status of Receive Line Signal Detect (RLSD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.

MSR(6): Ring Indicator (RI#) - Indicates the complement to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.

MSR(5): Data Set Ready (DSR#) - Indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(5) = 1), MSR(5) is equivalent to DTR# in the MCR.

MSR(4): Clear to Send (CTS#) - Indicates the complement of CTS# input. If the serial channel is in the loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.

MSR(3): Delta Receiver Line Signal Detect (DRLSD) - Indicates that the RLSD# input state has been changed since the last time the Host read it.

MSR(2): Trailing Edge of Ring Indicator (TERI) - Indicates that the RI input state to the serial channel has been changed from a low to high since the last time the Host read it. The change to logic 1 doesn't activate the TERI.

MSR(1): Delta Data Set Ready (DDSR) - A logic "1" indicates that the DSR# input to the serial channel has changed state since the last time it was read by the Host.

MSR(0): Delta Clear to Send (DCTS) - This bit indicates that the CTS# input state to the serial channel has been changed since the last time it was read by the Host.

Table 7-30. Modem Status Register Bits

MSR Bits	Mnemonic	Description
MSR(7)	RLSD#	Receiver Line Signal Detect
MSR(6)	RI#	Ring Indicator
MSR(5)	DSR#	Data Set Ready
MSR(4)	CTS#	Clear To Send
MSR(3)	DRLSD	Delta Receiver Line Signal Detect
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(1)	DDSR	Delta Data Set Ready
MSR(0)	DCTS	Delta Clear to Send

7.3.4 Reset

Reset of IT8661F and IT8661RF should be held to an idle mode reset high for 500ns until initialization causes the following:

1. Initialization of the transmitter and receiver internal clock counters.
2. Resetting all bits of LSR, (except LSR(5) and LSR(6), THRE and TEMT (they are set only by a hardware reset), all bits of MCR and all corresponding discrete lines, memory and logic elements. Before resetting, the IT8661F and IT8661RF remain in the idle mode until programmed

Table 7-31. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5, 6 are high, others are low.
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT0, SOUT1	Reset	High
RTS0#, RTS1#, DTR0#,DTR1#	Reset	High
IRQ of Serial Port	Reset	High Impedance

7.3.5 Programming

Each serial channel of IT8661F and IT8661RF is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though the control register can be written in any order, the IER should be last because it controls the interrupt enables. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

7.3.6 Software Reset

This method allows returning to a completely known state without a SYSTEM RESET. It consists of writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before enabling interrupts to clear out any residual data or status bits which may be invalid for subsequent operations.

7.3.7 Clock Input Operation

The input frequency of the Serial Channel is 24MHz ÷ 13, not exactly 1.8432MHz.

7.3.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When set FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

a. The receive data available interrupt and the IIR, receive data available indication, will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

b. The receiver line status interrupt has higher priority than the received data available interrupt.

c. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO.

RCVR FIFO time-out Interrupt: By enabling RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

a. It will occur only if there is at least one (1) character in the FIFO whenever the period between the most recent received serial character and the most recent Host read from the FIFO is longer than four (4) consecutive character times.

b. The RLCK clock signal input is used to calculate character times.

c. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever any time-out interrupt occurs. The timer will be reset when the Host reads one (1) character from the RCVR FIFO.

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt will occur as follows:

a. The transmitter interrupt will occur when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs: THRE = 1 and there has not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate. Once it is enabled, the THRE indication is delayed one (1) character time minus the last stop bit times.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are zero]

Either one or both XMIT and RCVR can be in this operation mode which the user program will check RCVR and XMIT status via the LSR as described next page:

LSR(7): RCVR FIFO error indication

LSR(6): XMIT FIFO and Shift register empty

LSR(5): The XMIT FIFO empty indication

LSR(1) - LSR(4): Specifies that errors have occurred. Character error status is handled the same way as in the interrupt mode. The IIR is not affected since IER(2)=0.

LSR(0): Will be high whenever the RCVR FIFO contains at least one byte

There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode.

7.4 Parallel Port

The IT8661F and IT8661RF incorporate one multi-mode high performance parallel port.

The IT8661F and IT8661RF support the IBM AT, PS/2 compatible bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Refer to IT8661F and IT8661RF Configuration registers and Hardware Configuration Description for information on the following: enabling/ disabling, changing the base address of the parallel port, and selecting the mode of operation.

Table 7-32. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	76	STB#	WRITE#	nStrobe
2-9	71-68,66-63	PD0 - 7	PD0 - 7	PD0 - 7
10	62	ACK#	INTR	nAck
11	61	BUSY	WAIT#	Busy PeriphAck(2)
12	60	PE	(NU) (1)	PError nAckReverse(2)
13	59	SLCT	(NU) (1)	Select
14	77	AFD#	DSTB#	nAutoFd HostAck(2)
15	75	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	73	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	74	SLIN#	ASTB#	nSelectIn

Notes: 1. NU: Not used
2. Fast mode
3. For more information, please refer to the IEEE 1284 standard

7.4.1 SPP and EPP Modes

Table 7-33. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1H	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2H	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1. The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses when the bit is high.

(2) Status Port (Base Address 1 + 01h)

This is a READ only register. Writing to this register has no effect. The contents of this register are latched during an IOR cycle.

Bit 7 - BUSY# : Inverse of printer BUSY signal, a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.

Bit 6 - ACK#: Printer acknowledge, a logic "0" mean that the printer has received a character and ready to accept another. A logic "1" means that it is still processing the last character.

Bit 5 - PE: Paper end, A logic "1" indicates paper end.

Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.

Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.

Bits 1, 2: Reserved, these bits are always "1" when read.

Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec time out has occurred in EPP operation. A logic "0" means no time out and a logic one (1) means that a time out error has been detected. This bit is cleared by a RESET or writing a logic “1” to it. When IT8661F and IT8661RF are selected to non-EPP mode(SPP or ECP), this bit is always logic "one" (1) when read.

(3) Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.

Bits 6, 7: Reserved, these two (2) bits are always "one" (1) when read.

Bit 5 PDDIR: Data port direction control, this bit determines the direction of the data port. Set this bit "0" to output the data port to PD bus and "1" to input from PD bus.

Bit 4 IRQE: Interrupt request enable, setting this bit "1" enables interrupt requests from the parallel port to the Host. An interrupt request is generated by a "zero" (0) to "one" (1) transition of the ACK# signal.

Bit 3 SLIN: Inverse of SLIN# pin, setting this bit to "1" selects the printer.

Bit 2 INIT: Initiate printer, setting this bit to "0" initializes the printer.

Bit 1 AFD: Inverse of the AFD# pin, setting this bit to "1" causes the printer to automatically feed after each line is printed.

Bit 0 STB: Inverse of the STB# pin. This pin controls the data strobe signal to printer.

(4) EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR causes an EPP ADDRESS READ cycle.

(5) EPP Data Port 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW causes an EPP DATA WRITE cycle. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR causes an EPP DATA READ cycle.

7.4.2 EPP Mode Operation

When the parallel port of IT8661F or IT8661RF is selected to be in EPP mode, the SPP mode is also available, if no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY high (EPP READ/WRITE cycle) to WAIT# being

de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle is aborted and a logic "1" will be read in the status port register Bit 0. The Host must write 0 to bits 0, 1, 3 of the control port register, before any EPP READ/WRITE cycle (EPP spec.) The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

(1) EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip drives IOCHRDY low and asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. Peripheral de-asserts WAIT, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus and releases IOCHRDY, allowing the Host to complete the I/O WRITE cycle.
4. Peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives PD bus to tristate for peripheral to drive.
2. The chip drives IOCHRDY low and asserts ASTB# after IOR becomes active.
3. Peripheral drives PD bus valid and de-asserts WAIT, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7 and releases IOCHRDY, allowing the Host to complete the I/O READ cycle.
4. Peripheral drives PD bus to tristate and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip drives IOCHRDY low and asserts WRITE# (STB#) and DSTB(AFD#) after IOW becomes active.
3. Peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to PD bus and releases IOCHRDY, allowing the Host to complete the I/O WRITE cycle.
4. Peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(4) EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tristate for peripheral to drive.
2. The chip drives IOCHRDY low and asserts DSTB# after IOR becomes active.
3. Peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7 and releases IOCHRDY allowing the host to complete the I/O READ cycle.
4. Peripheral tristates PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

7.4.3 ECP Mode Operation

This mode is both software and hardware compatible with that of the existing parallel ports, allowing ECP to be used as a standard LPT port when ECP is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or ECP in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how

many times a byte is repeated. The IT8661F and IT8661RF do not support hardware compression. For a detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 7-34. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 7-35. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	R	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions

Table 7-36. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description on pages 62-64 for a detailed description of mode selection.

(3) ECP Pin Descriptions

Table 7-37. ECP Pin Descriptions

Pin	Name	Type	Description
76	nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device
71-68, 66-63	PD0~PD7	I/O	Address or data or RLE data
62	nACK (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
61	Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (hand-shaking with nStrobe). In the reverse direction, this signal is used to determine whether command or data information is present on PD0~PD7.
60	PError (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, permitting the host to drive the PD bus.
59	Select	I	Printer On-Line indication
77	nAutoFd (HostAck)	O	In the reverse direction, it is used for handshaking between the nACK and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether command or data information is present on PD0 ~ PD7.
75	nFault (nPeriphRequest)	I	In the forward direction(only), the peripheral is permitted (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to host, which has ultimate control over the transfer direction.
73	nInit (nReverseRequest)	O	The host may drive this signal low to place PD bus in the reverse direction. In ECP mode, the peripheral is permitted to drive the PD bus when nInit is low and nSelect is high
74	nSelectIn (1284 Active)	O	Always inactive (high) in ECP mode

(4) Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a WRITE operation, the contents of the data bus are latched by the Data Register at the rising edge of the IOW# input. The contents are then sent without being inverted to PD0~ PD7. In a READ operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data byte written to this port is placed in the FIFO and tagged as an ECP Address/RLE. Then the hardware automatically sends this data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)

Bits 0, 1 and 2 of this register are not implemented. They remain at high in a READ operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.

dsr(6): This bit is the state of the nAck input.

dsr(5): This bit is the state of the PError input.

dsr(4): This bit is the state of the Select input.

dsr(3): This bit is the state of the nFault input.

dsr(2)~dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bits 6 and 7 of this register have no function. They are set high during the READ operation, and cannot be written. Contents in bits 0~5 are initialized to zero when the RESET pin is active.

dcr(7)~dcr(6): These two bits are always high.

dcr(5): Except in modes 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high, in input operation. This bit will be forced to low in mode 000.

dcr(4): Setting this bit high enables interrupt request from peripheral to host due to a rising edge of the nAck input.

dcr(3): It is inverted and output to SelectIn.

dcr(2): It is output to nInit without inversion.

dcr(1): It is inverted and output to nAutoFd.

dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshake to the peripheral according to standard parallel port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can get these bytes by making READ operations or DMA transfers from this FIFO.

(10) Test FIFO Mode (tFifo) (Base 2+00h, Mode 100)

The Host may operate READ/WRITE or DMA transfers to this FIFO in any direction. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a READ from an empty tFifo causes the last data byte to be returned.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This READ-only register indicates to the system that interrupts are ISA-Pulses. This is an 8 bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is READ-only.

cnfgB(7): Logic zero read indicates that the chip does not support hardware RLE compression.

cnfgB(6): Returns the value on the ISA IRQ line to warn of possible conflicts.

cnfgB(5)~cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.

cnfgB(2)~cnfg(0): A value 000 read indicates that the DMA channel is jumpered 8-bit DMA.

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

ECP function control register.

ecr(7)~ecr(5): These bits are used for READ/WRITE and Mode selection.

Table 7-38. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	Standard Parallel Port Mode. The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	PS/2 Parallel Port Mode. It is similar to the SPP mode, except that the dcr(5) is READ/WRITE. When dcr(5) is 1, the PD bus is tristate. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port data FIFO Mode. This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to the FIFO. Then the FIFO data is sent to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	ECP Parallel Port Mode. In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically sent to the peripheral under ECP protocol. In the reverse direction, bytes are sent to the ecpDFifo from ECP port.
100, 101	Reserved, not defined
110	Test mode. In this mode, the FIFO may be read from or written to, but it cannot be sent to peripheral.
111	Configuration mode. In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode

1: Disables the interrupt generated on the asserting edge of the nFault input.

0: Enables the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from 1 to 0 in the low level nFault.

ecr(3): dmaEn, READ/WRITE

1: Enables DMA. DMA starts when serviceIntr (ecr(2)) is 0.

0: Disables DMA unconditionally.

ecr(2) : serviceIntr, READ/WRITE

1: Disables DMA and all service interrupts

0: Enables the service interrupts. This bit will be set to one (1) by hardware when one (1) of the three (3) service interrupts has occurred.

Writing one (1) to this bit will not generate an interrupt.

Case 1: dmaEn=1

During DMA, this bit is set to 1 (a service interrupt generated) when terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0

This bit is set to 1 (a service interrupt generated) whenever there are writeIntrThreshold or more bytes space free in the FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

ecr(1): full, read-only 1: The FIFO is full and cannot accept another byte.

0: The FIFO has at least 1 free data byte space.

ecr(0): empty, READ only

1: The FIFO is empty.

0: The FIFO contains at least 1 data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks which happen before data is transferred, are software controlled. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between FIFO and the ECP port.

From mode 000 or 001, any other mode may be immediately switched to from another mode. To change direction, the mode must first be set to 001.

In extended forward mode, FIFO must be clear and all the signals must be de-asserted before returning to mode 000 or 001. In ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Usually, unneeded data is accumulated during ECP reverse handshaking, when mode changes during a data transfer. In such conditions, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

(15) Software Operation (ECP)

Before ECP operation can begin, it is first necessary for the Host to switch the mode to 000 in order to negotiate with the parallel port. During this process, the Host determines whether peripheral supports ECP protocol.

After this negotiation, mode is set to 011 (ECP). To enable the drivers, direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, address/RLE transfers are byte-wide. ECP address/RLE bytes may be automatically sent by writing the ecpAFifo. Similarly, data PWords may be automatically sent via ecpDFifo.

To change directions, the Host switches mode to 001. It then negotiates either the forward or reverse channel, sets direction to 1 or 0, and finally switches mode to 001. If the direction is set to 1, the hardware performs handshaking for each ECP data byte read, then tries to fill the FIFO. At this time, PWords may be read from the expDFifo while it retains data. It is also possible to perform ECP transfers by handshaking with individual bytes under program control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

Standard PC DMA protocol is followed. As in the programmed I/O case, software sets THE direction and state. Next, the desired count and memory address are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents in the FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from the FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting dREQ for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing a transfer, the host DMA controller is disabled, serviceIntr is then set either to 1, and dmaEn is next set to 0. If Either the contents in FIFO are empty or full, the DMA will start again. This is first done by enabling the host DMA controller, then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reaches the peripheral device.

(17) Interrupts

It is necessary to generate an interrupt when any of the following states are reached.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in FIFO is greater than or equal to writeIntrThreshold.

2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of full PWords in the FIFO is greater than or equal to readIntrThreshold.

3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.

4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

5. ackIntEn = 1. In current implementations using existing parallel ports, the interrupt generated may be either edge or level type, making it "ISA-friendly".

(18) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is zero (0) and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

Any PC ISA implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on the ISA is maintained in the interface. Although the ISA bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or near the permitted peak bandwidth of 500KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

7.5 FIR Controller

The FIR controller of IT8661RF is fully IrDA1.1 compliant. It supports the serial infrared link at 288Kbits, 576Kbits, 1.152Mbits and 4Mbits. The three lower speeds comply with Synchronous Data Link Control (SDLC) protocol, a packet with start/stop flags delimiting a data packet encoded by 'zero-insertion'. The 4Mbit protocol uses an optical preamble and post-amble to delimit the 4 Pulse Position Modulated (4 PPM) packet data.

7.5.1 FIR Transmit Operation

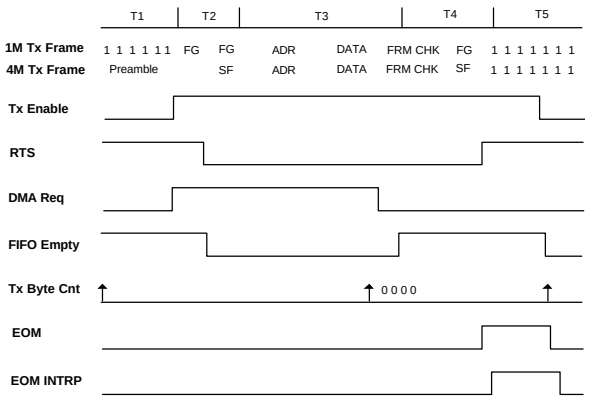


Figure 7-2. Time Waveform for FIR Transmit Operation

T1: Setup phase:

(1) Set up Tx Control Registers for Transmitting options.

(2) Load the byte count to the Transmit Byte Count Register.

(3) Set up the host DMA controller and the Tx packet.

(4) Set RTS and Transmit Enable bits.

T2: Startup phase:

(1) RTS is active. If no carrier is detected, then the Transmitter begins to transmit.

(2) (2) DMA request is activated if DMA is enabled. The Tx FIFO is being filled with transmitted data. If DMA is not enabled, WRITE Tx FIFO command can be used.

(3) If the Num Start Flag/Preamble bit is '0', the transmitter starts sending flags (1M) or Preambles (4M) until the Tx FIFO is half filled (8 bytes). If the Num Start Flag/Preamble bit is '1', the transmitter waits until the Tx FIFO is half filled, then sends two starting flags (1M mode) or preambles and one Start Flag (4M mode).

T3: Data Send Phase:

(1) The transmitter starts sending data stored in the FIFO.

(2) DMA Req stops. The transmitter sends out the remaining data in the FIFO.

(3) CRC generator inverts the CRC and sends it out.

(4) Send Closing Flag, set EOM latch, and activate Interrupt.

T4: End of Transmission

(1) The byte Counter counts down to 0.

(2) DMA Req stops. The transmitter sends out the remaining data in the FIFO.

(3) CRC generator inverts the CRC and sends it out.

(4) Closing Flag is sent. EOM latch is set, and Interrupt is activated.

T5: Idle Phase:

(1) The transmitter continues sending '1's or Flags (1M)/Preambles (4M) depending on the Idle line setting option.

(2) The host reads the Tx Status Register to check for transmission completion status.

(3) Reset EOM, Transmit Enable and RTS bits.

(4) End of transmission.

7.5.2 FIR Receive Operation

Receiving logic facilities:

(1) Receive control circuitry.

(2) Receive Byte Count Register to keep track of received bytes.

(3) Receive FIFO, 16 x 11 bits 8-bit data 3-bit status: Frame Error, Abort and End Of Frame.

(4) Receive Ring Frame Counter to keep track of the Rx byte number in the host Rx buffer.

(5) Receive Ring Frame Pointer which points to the last byte of the last received packet in the host Rx buffer.

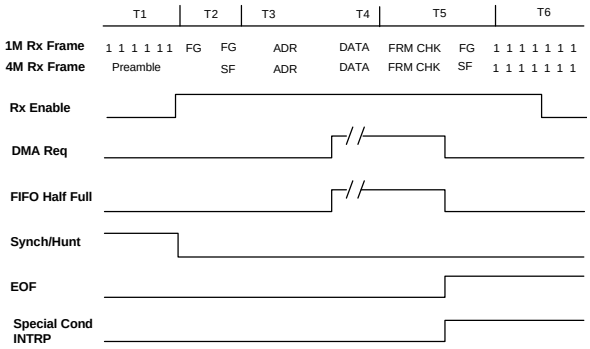


Figure 7-3. Time Waveform for FIR Receive Operation

T1: Startup phase:

(1) Set up Receive Control Registers for receiving options.

(2) Set Receive Enable bit.

(3) FIR mode logic detects Carrier, receive clock starts running. If consecutive '1's are received, the receive clock may not be synchronized with the incoming data.

T2: Flag(s)/Preambles Detection:

(1) When the Starting flag is detected, all counters in the receiver are initialized. Characters can be recognized from this point on.

(2) '0' deletion starts for 1M-bit mode only.

T3: Address Matching:

(1) The first non-flag byte after the starting flag is the address. Depending on the address mode option, the frame can be rejected or start receiving. If the frame is rejected, the receiver will look for the next starting flag and another address match.

T4: Data Receiving:

(1) When a data byte is received, the data and the three (3) status bits are stored in the Rx FIFO.

(2) If DMA is enabled, DMA request is activated when the FIFO threshold level is reached. DMA request continues until all data stored in the FIFO has been transferred to the host receive buffer. However, the four (4) status bits in the FIFO will not be transferred to the host.

(3) If DMA is not used, the READ Rx FIFO I/O command can be used. Read the status bits first, then read the data byte. If EOF or Abort is set to '1', the data byte just read is the last byte of the packet. If the FIFO is still not empty, the next entry is the beginning of another packet.

(4) Receive byte counter and the Receive Ring Frame counter increases accordingly.

T5: Closing Flag:

(1) End of Frame bit will be set, when the closing flag is detected.

(2) CRC pattern is checked. Frame error is set if CRC is wrong.

T6: Post Frame phase:

(1) DAM request continues until all the received data in the FIFO has been transferred. Two (2) more bytes in the following format will be stored in Rx FIFO and transmitted to the host receive buffer:

First byte:	7-0 - Byte count 7 to 0
Second byte:	7 - Abort
	6 - Frame Error
	5 - Overrun
	0 - Byte Count 1

(2) DMA de-activates.

(3) The Receive Ring Frame Pointer is updated pointing to the 2nd byte above, which has been successfully stored in the host Rx buffer.

(4) If DMA is not used, the last two bytes will not be stored in the FIFO. Status bit EOF will be set at the last Frame Check byte received.

(5) Repeat steps T2 through T6 if receiving continuous frame is required.

7.5.3 FIR Controller Registers Description

Table 7-39. FIR Controller Registers Summary

Bank	Address	READ	WRITE
0	Base + 0h	Master Control Register	Master Control Register
0	Base + 1h	Master Status Register	Miscellaneous Control Register
0	Base + 2h	Rx FIFO Register	Tx FIFO Register
0	Base + 3h	Tx Control 1 Register	Tx Control 1 Register
0	Base + 4h	Tx Control 2 Register	Tx Control 2 Register
0	Base + 5h	Tx Status Register	
0	Base + 6h	Rx Control Register	Rx Control Register
0	Base + 7h	Rx Status Register	Reset Command Register
1	Base + 0h	Master Control Register	Master Control Register
1	Base + 1h	Address Register	Address Register
1	Base + 2h	Rx Byte Count Low Register	
1	Base + 3h	Rx Byte Count High Register	
1	Base + 4h	Rx Ring Frame Pointer Low Register	
1	Base + 5h	Rx Ring Frame Pointer High Register	
1	Base + 6h	Tx Byte Count Low Register	Tx Byte Count Low Register
1	Base + 7h	Tx Byte Count High Register	Tx Byte Count High Register
2	Base + 0h	Master Control Register	Master Control Register
2	Base + 1h	Infrared Configuration 1 Register	Infrared Configuration 1 Register
2	Base + 2h	Infrared Transceiver Control Register	Infrared Transceiver Control Register
2	Base + 3h	Infrared Configuration 2 Register	Infrared Configuration 2 Register
2	Base + 4h	Timer Register	Timer Register
2	Base + 5h	Infrared Configuration 3 Register	Infrared Configuration 3 Register
2	Base + 6h	Reserved	
2	Base + 7h	Reserved	

(1) Master Control Register (Bank=0,1,2h, Base Address+0h, READ/WRITE)

Bit 7 Interrupt Enable

Setting this bit to '1' enables all FIR Controller interrupts.

Bit 6 Tx Enable

Setting this bit to '1' enables the transmitter logic in the FIR Controller. No packets are transmitted until the transmitter has been enabled

Bit 5 Rx Enable

Setting this bit to '1' enables the receiver logic in the FIR Controller. No packets are received until the receiver has been enabled.

Bits 4-0 Bank Select

b4	b3	b2	b1	b0	Bank #
0	0	0	0	0	Bank 0
0	0	0	0	1	Bank 1
0	0	0	1	0	Bank 2

(2) Master Status Register (Bank=0h, Base Address+1h, READ-only)

Bit 7 Reserved

Bit 6 Timer Interrupt

When set to '1', indicates a timer interrupt is pending.

Bit 5 Tx Interrupt

When set to '1', indicates a transmitter interrupt is pending.

Bit 4 Rx Interrupt

When set to '1', indicates a receiver interrupt is pending. The following conditions clear the Rx interrupt condition.

* Reading the Rx Ring Frame Counter Low Register
* Issuing a Reset Rx Special Condition Interrupt command
* Clearing the Rx Enable bit
* Hardware Reset
* Software Reset

Bits 3-1 Interrupt identification

These three (3) bits correspond to interrupt identification ID2-ID0 which provide an alternate method for identifying the interrupt source by indicating the interrupt type and priority level as shown in following table:

Interrupt Type	ID2	ID1	ID0	Priority
Rx Special Condition * FIFO Overrun * Frame Error * EOF * Rx Abort * Sync/Hunt	1	0	0	Highest
Rx Data Available	1	0	1	Second
Tx Buffer Empty	1	1	0	Third
Tx Special Condition * FIFO Underrun * EOM * Early EOM	1	1	1	Fourth

Bit 0 Reserved

(3) Miscellaneous Control Register (Bank=0h, Base Address+1h, WRITE-only)

Bits 7-6 DMA Channel Select

Specify single or dual DMA channel usage.

b7	b6	DMA Channel Select
0	0	No DMA
0	1	Channel 1 for Receive
1	0	Channel 1 for Transmit
1	1	Channel 1 for Receive/ Channel 2 for Transmit

Bit 5 Controller Loopback

When set to '1', the FIR controller's transmit data output signal is internally looped back to its receive data input. This allows for diagnostic testing of the FIR controller transmit and receive data paths.

Bit 4 4Mbit Loopback

When set to '1', the 4Mbit modem transmits data output signal is internally looped back to its receive data input. This allows for

diagnostic testing of the modem transmit and receive data paths.

Bits 3-0 Reserved

(4) Rx FIFO Register (Bank=0h, Base Address+2h, READ-only)

Bits 7-0 Receive Data

Used to read receive packet data from Rx FIFO

(5) Tx FIFO Register (Bank=0h, Base Address+2h, WRITE-only)

Bits 7-0 Transmit Data

Used to write transmit packet data to Tx FIFO.

(6) Tx Control 1 Register (Bank=0h, Base Address+3h, READ/WRITE)

Bit 7 Request To Send (RTS)

Setting this bit to '1' activates the Request To Send signal to the modem.

Note: The Tx Enable bit (bit 6 of Master Control Register) must be set, and Tx FIFO must contain transmit data prior to activating RTS. Setting this bit to '0' de-activates the Request To Send signal to the modem.

Bit 6 Enables Tx FIFO Ready Interrupt

Setting this bit to '1' enables Tx FIFO Ready interrupts.

Setting this bit to '0' disables Tx FIFO Ready interrupts.

Bit 5 Enables Tx FIFO Underrun/EOM Interrupt

Setting this bit to '1' enables FIFO underrun and EOM interrupts.

Bit 4 Tx FIFO Level

Setting this bit to '1' sets the Tx FIFO threshold to half-empty level.

Setting this bit to '0' sets the Tx FIFO threshold to not full level.

Bit 3 Auto Reset RTS

Setting this bit to '1' enables automatic deactivation of the modem Request To Send line at the end of transmission.

For back-to-back transmission, it is desirable that the Request To Send signal remains active for the entire duration in which packets are transmitted. It is therefore recommended that Auto Reset RTS be disabled while running back-to-back transmissions.

Bit 2 Auto Reset EOM

Setting this bit to '1' causes the EOM bit to automatically clear when the Tx Status Register is read.

Setting this bit to '0' causes the EOM bit to remain set after the Tx Status Register has been read. Only a Reset FIFO Underrun/EOM Latch command or a hardware reset can clear it.

Bit 1 Tx Idle

Setting this bit to '1' causes the TXD output line to remain in the inactive state when the transmitter is idle.

Setting this bit to '0' causes the transmitter to transmit continuous flags (1Mbit mode) or continuous preambles (4Mbit mode) when the transmitter is idle.

Bit 0 Underrun Abort

When a FIFO underrun occurs, the software has two options before transmission is terminated. One option is to send an abort sequence to the receiving end. The other option is to transmit a CRC and an ending/stop flag following the transmission of the last data byte in Tx FIFO.

Setting this bit to '1' causes the transmitter to transmit an abort sequence when underrun occurs.

Setting this bit to '0' causes the transmitter to transmit a CRC and an ending/stop flag immediately following the transmission of the last data byte in Tx FIFO before the underrun condition occurs.

(7) Tx Control 2 Register (Bank=0h, Base Address+4h, READ/WRITE)

Bit 7 Send Break

Setting this bit to '1' causes the transmitter to transmit zeros.

Bit 6 Enables TX CRC

Setting this bit to '1' enables automatic CRC generation of all outgoing packets. The CRC is automatically generated by the transmitter logic and transmitted after the data field, but before the ending flag.

Setting this bit to '0' disables CRC generation. This allows transmission of packets already containing a valid CRC.

Bits 5-4 SIR Interaction Pulse (SIP) Control

Commands the 4Mbit modem to send a SIR Interaction Pulse based on the bit setting. A '01' bit setting instructs the 4Mbit modem to transmit a SIP at the end of current packet. A '10' bit setting instructs the 4Mbit modem to transmit a SIP immediately, regardless of the modem's current activity. Note: SIP control bits are self-clearing.

Bit 3 Num Start Flag/Preamble

Specifies the number of starting flags or preambles to transmit for a given packet.

Setting this bit to '1' causes only two starting flags or a single preamble to be transmitted per packet.

Setting this bit to '0' causes several starting flags or preambles to be transmitted.

Bits 2-0 Early EOM Interrupt Level

b2	b1	b0	Early EOM Interrupt Level
0	0	0	Interrupt by EOM Only
0	0	1	Tx Byte Count = 16
0	1	0	Tx Byte Count = 32
0	1	1	Tx Byte Count = 64
1	0	0	Tx Byte Count = 128
1	0	1	Tx Byte Count = 256
1	1	0	Tx Byte Count = 512
1	1	1	Tx Byte Count = 1024

(8) Tx Status Register (Bank=0h, Base Address+5h, READ-only)

Bits 7-4 Reserved

Bit 3 FIFO Underrun

When set to '1', indicates Tx FIFO ran out of data before the transmitter could finish transmitting all the data (i.e. Tx FIFO is empty, and the Tx Byte Count value is greater than zero). This bit must be reset by an explicit FIFO UNDERRUN/EOM LATCH command.

Bit 2 End of Message (EOM)

When set to '1', indicates transmission completed successfully. The EOM interrupt occurs immediately after the CRC and ending flag have been transmitted. If bit 2 of Tx Control 1 Register (Auto Reset EOM) is enabled, the EOM bit will automatically clear when Tx Status is read. The EOM bit can also cleared by a RESET FIFO UNDERRUN LATCH command from the Reset Command Register.

Bit 1 Tx FIFO Ready

When set to '1', indicates Tx FIFO is ready for more data transfers. when the bit 6 of Tx Control 1 Register is set, an interrupt is generated whenever this condition becomes true. Alternately, this bit may be polled when the interrupt is disabled. When Tx FIFO is full, this bit is set to '0'.

Bit 0 Early EOM

When set to '1', indicates the Tx Byte Count has reached the count level set by the Early EOM Interrupt Level bits. This bit is cleared by reading Tx Status.

(9) Rx Control Register (Bank=0h, Base Address+6h, READ/WRITE)

Bit 7 Rx FIFO Level

Setting this bit to '1' sets the Rx FIFO threshold to half-full (more than 8 bytes of Receive data are still remaining in FIFO).

Setting this bit to '0' sets the Rx FIFO threshold to not empty (more than 1 byte of Receive data remaining in FIFO).

Bit 6 Enables Rx CRC

Setting this bit to '1' enables automatic CRC checking of all incoming packets.

Setting this bit to '0' disables CRC checking. Disabling this bit results in no CRC errors being reported.

Bits 5-4 Rx Address Mode

Specifies the type of address filtering to apply for determining which receive frames to accept.

b5	b4	Rx Address Mode
0	0	All packets accepted
0	1	Address must match Frame Address Register(FAR)
1	0	Address (high nibble) must match FAR
1	1	Reserved

Note: Packets with a universal address 0x7F are always accepted

Bit 3 Enables Sync/Hunt Change interrupt

Setting this bit to '1' enables Sync/Hunt Change interrupts.

Bit 2 Reserved

Bit 1 Enables Rx FIFO ready Interrupt

Setting this bit to '1' enables Rx FIFO Ready interrupts.

Setting this bit to '0' disables Rx FIFO Ready interrupts.

Bit 0 Enables Rx Special Condition Interrupt

Setting this bit to '1' enables the following special condition interrupts:

* Overrun
* Frame Error
* End of Frame (EOF)
* Rx Abort

Setting this bit to '0' disables the above special condition interrupts:

(10) Rx Status Register (Bank=0h, Base Address+7h, READ-only)

Bit 7 Rx Abort

When set to '1', indicates abort sequence detected in the receive data stream of current packet.

In 1Mbit mode, the abort sequence is characterized by seven (7) or more consecutive 1's in the data stream.

In 4Mbit mode, the abort sequence is represented by two (2) or more illegal symbols "0000" after a valid start flag but before a complete stop flag; or an illegal symbol, which is not part of a valid stop flag field, received any time after a valid flag.

Bit 6 Frame Error

When set to '1', indicates a CRC or alignment error was detected in the incoming data stream. This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 5 FIFO Overrun Interrupt

When set to '1', indicates the host system was not fast enough removing the data out of Rx FIFO before it overflowed with received data.

Bit 4 End of Frame (EOF)

When set to '1', indicates an ending/stop flag or abort sequence was detected in the incoming data stream.

This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 3 Rx Data Available

When set to '1', indicates Rx FIFO is not empty. When set to '0', indicates Rx FIFO is empty.

When this bit is set, it does not cause an interrupt; rather it is used to unload the FIFO by polling.

Note: Rx FIFO Level (bit 7 of Rx Control Register) has no effect on the Rx Data Available bit.

Bit 2 Sync/Hunt Change

When set to '1', indicates a transition or status change occurred on the internal Sync/Hunt signal. The following conditions cause the Sync/Hunt signal to change states:

* When ENTER HUNT MODE command is issued

* Valid SDLC start or stop flag is detected

* Valid preamble or stop flag is detected (4Mbit mode)

If bit 3 of Rx Control Register (Enables Sync/Hunt Change Interrupt bit) is enabled, the setting of Sync/Hunt Change bit causes an interrupt to the host system. Reading the Rx Status Register after the interrupt has occurred clears the Sync/Hunt Change bit. If bit 3 of Rx Control Register is disabled, reading Rx Status register will directly provide the status of the Sync/Hunt signal and will not clear the Sync/Hunt Change bit.

Bits 1-0 Reserved

(11) RESET Command Register (Bank=0h, Base Address+7h, WRITE-only)

Bits 7-4 RESET Command

Used to send a reset signal to the appropriate hardware in order to clear a particular status condition, a counter, or general reset.

b7	b6	b5	b4	RESET Command
0	0	0	1	Enter Hunt Mode
0	0	1	0	Reset Rx FIFO Pointer
0	0	1	1	Reset Rx Special Condition Interrupt
0	1	0	0	Reset Rx Ring Frame Pointer
0	1	0	1	Reset FIFO Underrun/EOM Latch
0	1	1	0	Reset Tx FIFO Pointer
0	1	1	1	Hardware Reset

Note: These bits are self-clearing (i.e. a programmer does not need to reset the Reset Command bit value to "0000")

Bits 3-0 Reserved

(12) Frame Address Register (Bank=1h, Base Address+1h, READ/WRITE)

Bits 7-1 Rx Frame Address, A7-A1

Specifies the address value that must be contained in the address field of incoming frames.

Bit 0 is always '0'.

b7	b6	b5	b4	b3	b2	b1	b0
A7	A6	A5	A4	A3	A2	A1	0

(13) Rx Byte Count Low Register (Bank=1h, Base Address+2h, READ-only)

Bits 7-0 Rx Byte Count, D7-D0

Provides a running count (low-order value) of the number of bytes of data being received. It is useful when receiving back-to-back packets.

b7	b6	b5	b4	b3	b2	b1	b0
D7	D6	D5	D4	D3	D2	D1	D0

(14) Rx Byte Count High Register (Bank=1h, Base Address+3h, READ-only)

Bits 7-5 Reserved

Bits 4-0 Rx Byte Count, D12-D8

Provides a running count (high-order value) of the number of bytes of data being received. It is useful when receiving back-to-back packets.

b4	b3	b2	b1	b0
D12	D11	D10	D9	D8

(15) Rx Ring Frame Pointer Low Register (Bank=1h, Base Address+4h, READ-only)

Bits 7-0 Ring Frame Pointer (RFP), D7-D0

Used in back-to-back packet reception to provide the end-of-packet pointer value.

b7	b6	b5	b4	b3	b2	b1	b0
D7	D6	D5	D4	D3	D2	D1	D0

(16) Rx Ring Frame Pointer High Register (Bank=1h, Base Address+5h, READ-only)

Bits 7-0 Ring Frame Pointer (RFP), D15-D8

Used in back-to-back packet reception to provide the end-of-packet pointer value.

b7	b6	b5	b4	b3	b2	b1	b0
D15	D14	D13	D12	D11	D10	D9	D8

The RFP value is initially set to '0000h'. Thus, software should not use the RFP value for any computation prior to receiving the first packet.

(17) Tx Byte Count Low Register (Bank=1h, Base Address+6h, READ/WRITE)

Bits 7-0 Tx Byte Count, D7-D0

Provides a running count (low-order value) of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the low-order byte length of the data packet. When the counter reaches zero (0), the transmitter ceases to make DMA requests. Transmission continues until Tx FIFO is depleted.

b7	b6	b5	b4	b3	b2	b1	b0
D7	D6	D5	D4	D3	D2	D1	D0

(18) Tx Byte Count High Register (Bank=1h, Base Address+7h, READ/WRITE)

Bits 7-5 Reserved

Bits 4-0 Tx Byte Count, D12-D8

Specifies the high-order byte length of the data packet to be transmitted. Refer Tx Byte Count Register.

b4	b3	b2	b1	b0
D12	D11	D10	D9	D8

(19) Infrared Configuration 1 Register (Bank=2h, Base Address+1h, READ/WRITE)

Bits 7-4 Infrared Speed

Specifies the data rate under 1Mbit FIR modulation.

b7	b6	b5	b4	Infrared Speed
0	0	0	0	1.152 Mbps
0	0	0	1	0.576 Mbps
0	0	1	0	0.288 Mbps

Bits 3-0 Infrared Modulation

Specifies the modulation mode of infrared communication.

b3	b2	b1	b0	Infrared Modulation
0	0	0	0	HP-SIR
0	0	0	1	Sharp ASK
0	0	1	0	1.152 Mbps IrDA
0	0	1	1	Reserved
0	1	0	0	4 Mbps IrDA

(20) Infrared Transceiver Control Register (Bank=2h, Base Address+2h, READ/WRITE)

Bits 7-6 Reserved

Bit 5 High/Low Data Frequency

When an HP-like transceiver is selected in the configuration register, high or low infrared data frequency is determined by this bit.

Setting this bit to '1' causes the low frequency to be asserted on IRRXL pin.

Setting this bit to '0' causes the high frequency to be asserted on IRRXH pin.

When an IBM-like transceiver is selected in the configuration register, this bit will be invalidated.

Bit 4 Mode Select

When an IBM-like transceiver is selected in the configuration register, mode select function will be present on the IRRXH pin.

Setting this bit to '1' causes the external IRRXH pin to be high.

Setting this bit to '0' causes the external IRRXH pin to be low.

When an HP-like transceiver is selected in the configuration register, this bit will be invalidated.

Bit 3 Echo On

Setting this bit to '1' sets the optical loopback feature. This bit is set to '0' on power-up.

Bits 2-0 Reserved

(21) Infrared Configuration 2 Register (Bank=2h, Base Address+3h, READ/WRITE)

Bits 7,3,2 ACEN, CCTRL1, CCTRL0

These bits control the 4M pulse auto-chopping mechanism. This feature handles transceivers which deliver single pulses that exceed the 165ns maximum supported by the 4M demodulator. When autochop is enabled, the circuit measures a typical pulse width during a frame's preamble sequence and adjusts the chopping level accordingly. The error threshold can be adjusted by using the chop control bits (CCTRL0 and CCTRL1). The recommended setting for 4M mode is ACEN=1 CCTRL1=CCTRL0=0. These bits are reset to 0 on power-up. If this feature is used, the software must set these bits accordingly when entering 4M mode and reset them when leaving 4M mode. Chopping operation with the autochop enable bit reset is provided for diagnostic tests of the transceiver and is not recommended for normal operation where pulse widths can vary significantly.

The setting and their effects are as follows:

Autochop Enable / CCTRL1 / CCTRL0	Effect
000	Chopping circuit is disabled.
001	Extend the single pulse width tolerance to 187ns. Back-to-back pulses must be greater than 209ns.
010	Extend the single pulse width tolerance to 229ns. Back-to-back pulses must be greater than 249ns.
011	Extend the single pulse width tolerance to 208ns. Back-to-back pulses must be greater than 229ns.
100	Autochop enabled with maximum tolerance for error. Back-to-back pulses must be 62ns longer than a single pulse sample.
101	Autochop enabled with less tolerance for error. Back-to-back pulses must be 42ns longer than a single pulse sample.
110	Autochop enabled with zero tolerance for error. Back-to-back pulses must be 42ns longer than a single pulse sample.
111	Autochop enabled with zero tolerance for error. Back-to-back pulses must be longer than a single pulse sample. Digital transceiver with Rx signal in synchronous with 48MHz clock

Bits 6-4 Reserved

Bit 1 Disables SIR interrupt

Setting this bit to '1' causes SIR interrupt request to be masked.

Bit 0 Disables FIR Interrupt

Setting this bit to '1' causes FIR interrupt request to be masked.

(22) Timer Register (Bank=2h, Base Address+4h, READ/WRITE)

Bits 7-0 Timer value, D7-D0

Specifies the initialization value for the down counter. The counter has a period of 128µs. When the counter reaches zero (0), an interrupt is generated.

b7	b6	b5	b4	b3	b2	b1	b0
D7	D6	D5	D4	D3	D2	D1	D0

(23) Infrared Configuration 3 Register (Bank=2h, Base Address+5h, READ/WRITE)

Bit 7 Enables Sharp CD Interrupt

Setting this bit to '1', enables Sharp Carrier Detect interrupts.

Bit 6 Sharp Carrier Detect

When set to '1', this READ-only status bit indicates a 500KHz Sharp ASK carrier has been detected. To clear the interrupt, software must WRITE a '1' to this bit.

Bits 5-2 Reserved

Bit 1 Enable Timer Interrupt

Setting this bit to '1' enables Timer Interrupt.

Bit 0 Timer Interrupt

When set to '1', indicates a timer interrupt is pending. To clear the interrupt, software must WRITE a '1' to this bit. This bit is self-clearing.

8. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage (V_{CC}) .....-0.5V to V_{CC}+0.3V

Input Voltage (V_I).....-0.5V to 7.0V

Output Voltage (V_O)..... -0.5V to V_{CC}+0.3V

Storage Temperature (T_{STG})..... -65°C to 150°C

Power Dissipation..... 300mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
General Output Buffer Tri-state Leakage						
I_{OZ}	3-state Leakage	-20		20	µA	
I/O12 Type Buffer						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 12 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -6 mA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Leakage		10		µA	V_{IN} = 0
I_{IH}	Input High Leakage			-10	µA	V_{IN} = VCC
I/O24 Type Buffer						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -12 mA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Leakage		10		µA	V_{IN} = 0
I_{IH}	Input High Leakage			-10	µA	V_{IN} = VCC
O48 Type Buffer						
V_{OL}	Output Low Voltage			0.5	V	I_{OL} = 48mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -12 mA
O24 Type Buffer						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -12 mA

DC Electrical Characteristics (cont'd)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
O12 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 12mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -12 mA
OD24 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
OP12 Type Buffer						
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -12 mA
IS Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.0			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
OCLK Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 12mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -12 mA
ICLK Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.0			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC

9. AC Characteristics (VCC = 5.0V ± 5%, Ta = 0°C to + 70°C)

9.1 READ Cycle Timing

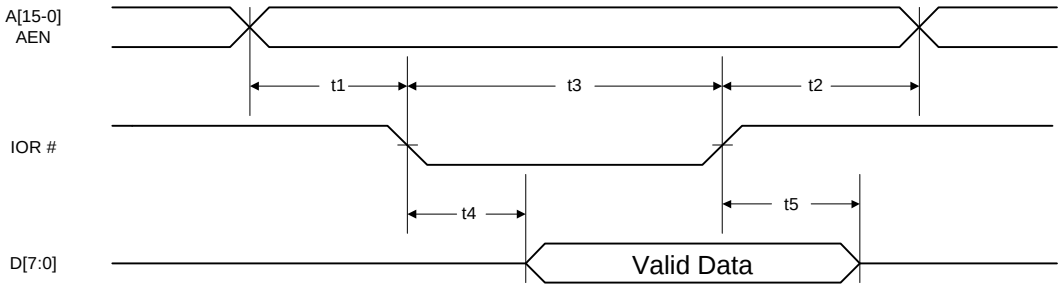


Table 9-1. READ Cycle Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Address setup to IOR# ↓	10			ns
t2	Address hold from IOR# ↑	10			ns
t3	IOR# pulse width	100			ns
t4	IOR# ↓ to Data valid	25		65	ns
t5	Output floating delay from IOR# ↑	25		50	ns

9.2 WRITE Cycle Timing

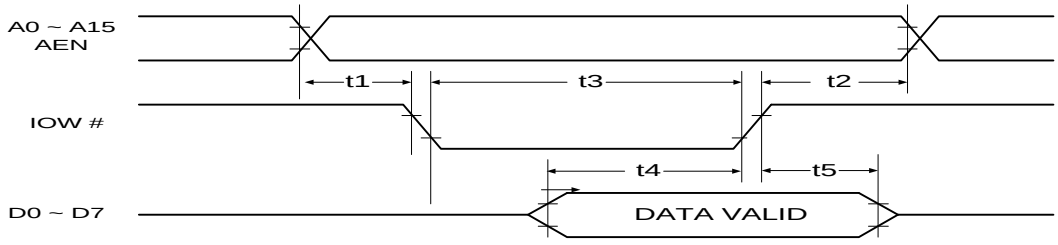


Table 9-2. WRITE Cycle Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Address setup to IOW# ↓	10			ns
t2	Address hold from IOW# ↑↑	10			ns
t3	IOW# pulse width	100			ns
t4	Data setup to IOW# ↑	25			ns
t5	Data hold from IOW# ↑	15			ns

9.3 FDC Timing

9.3.1 DMA Operation Timing

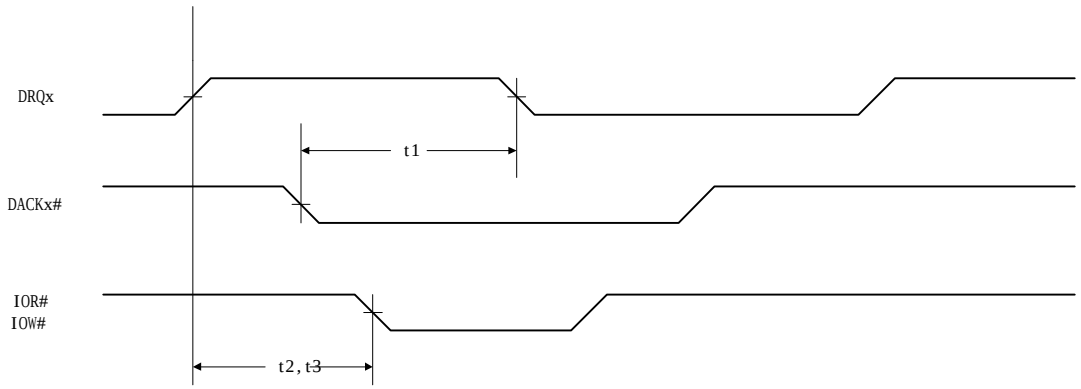


Table 9-3. DMA Operation Timing of FDC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	DACKx ↓ to DRQx ↓			100	ns
t2	DRQx ↑ to IOR# ↓	0			ns
t3	DRQx ↑ to IOW# ↓	0			ns

***** The DMA Channel is selected by the configuration register (0X74).

9.3.2 Terminal Count, Index

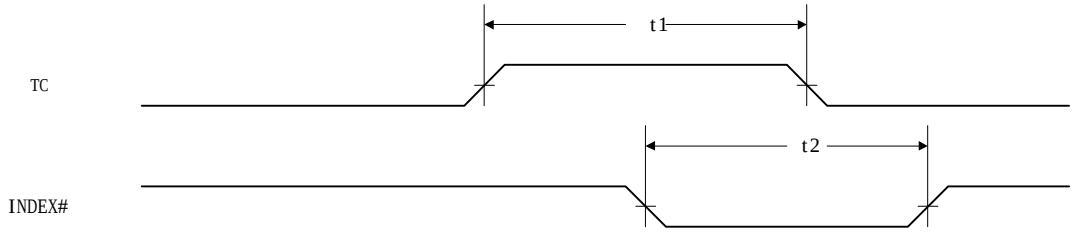


Table 9-4. Terminal Count, Index of FDC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Terminal count width	80			ns
t2	INDEX# pulse width	100			ns

9.3.3 FDD WRITE/READ Operation Timing

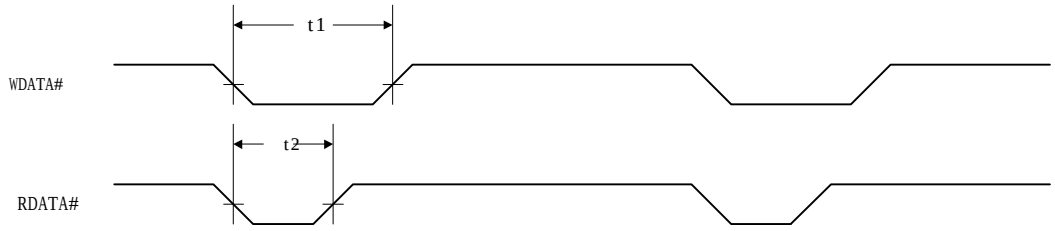


Table 9-5. FDD WRITE/READ Operation Timing of FDC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	WRITE data width (low)		396/248/ 252		ns
t2	READ data width (low)		248/396/ 748		ns

Note: In the typical column of above table, each item includes values for 500/300/250 bps transfer rates respectively.

9.3.4 SEEK Operation Timing

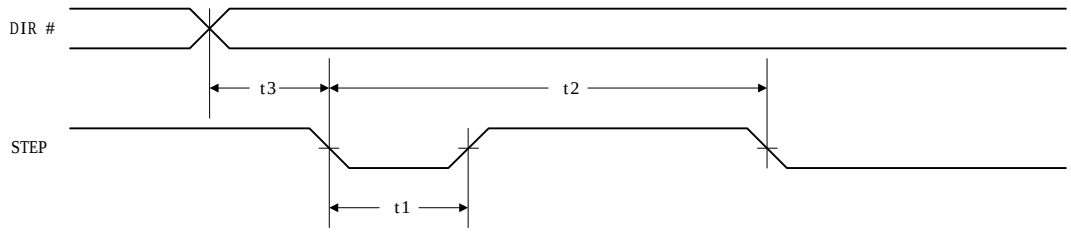


Table 9-6. SEEK Operation Timing of FDC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	STEP# active time	6			us
t2	STEP# cycle time	6.104			ms
t3	DIR# setup to STEP# ↓	1		2	us

9.4 Serial Port Timing

9.4.1 Transmitter

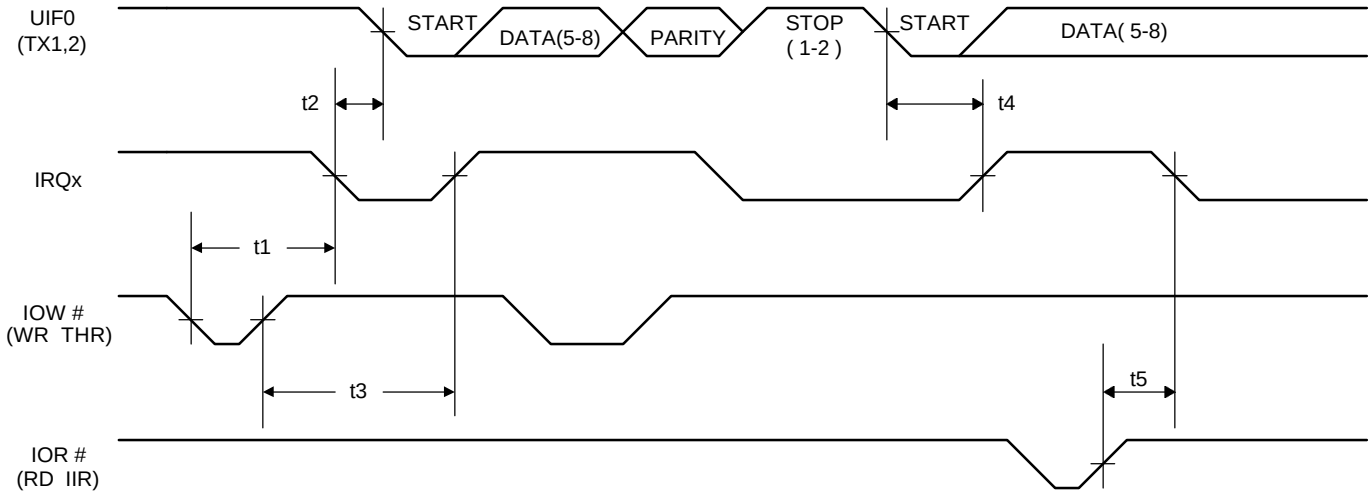


Table 9-7. Transmitter of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay from falling edge of IOW# (WR THR) to reset interrupt			80	ns
t2	Delay from initial interrupt reset to transmit start (SOUT)	8		24	Baud cycle
t3	Delay from initial write to IRQx active	8		24	baud cycle
t4	Delay from stop (SOUT) to IRQx ↑(THRE)	8		24	baud cycle
t5	Delay from IOR# ↑ (RD IIR) to reset IRQx (THRE)			100	ns

9.4.2 Modem

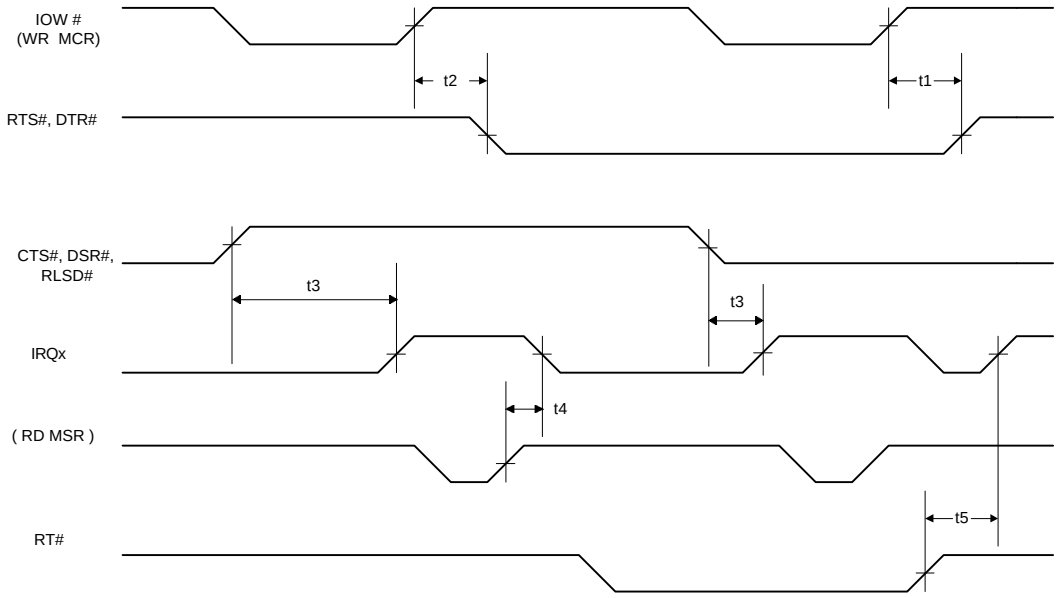


Table 9-8. Modem of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay from IOW# ↑ (WR MCR) to output (RTS# or DTR#) high			40	ns
t2	Delay from IOW# ↑ (WR MCR) to output (RTS# or DTR#) low			40	ns
t3	Delay to set interrupt IRQx from MODEM input (CTS#, RLSD#, DSR#)			40	ns
t4	Delay to reset interrupt IRQx from IOR# ↑ (RD MSR)			80	ns
t5	Delay to set interrupt IRQx from MODEM input (RI#)			40	ns

9.4.3 Receiver

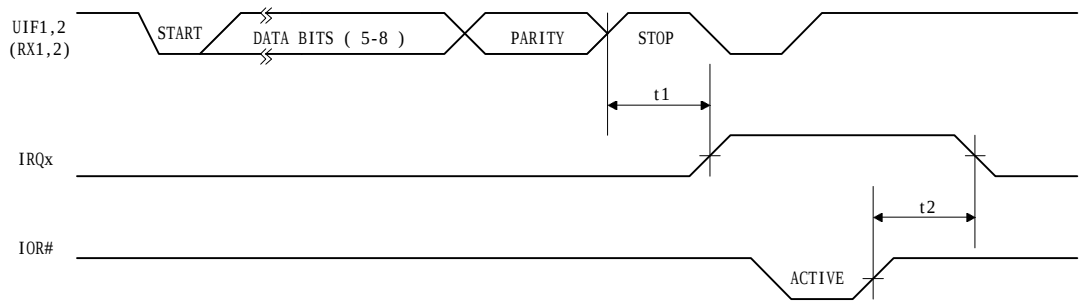


Table 9-9. Receiver of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay from stop (SIN) to set IRQx		8		clk_{ACE}
t2	Delay from IOR# ↑ (RD RBR/RD LSR) to reset interrupt IRQx		55		ns

Note: ^{clk}ACE stands for ACE actual input clock, i.e. 24/13=1.846 MHz internal clock.

9.4.4 IrDA Receive Timing

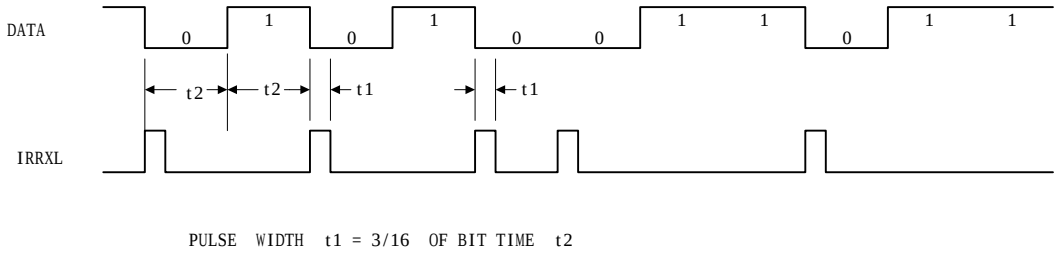
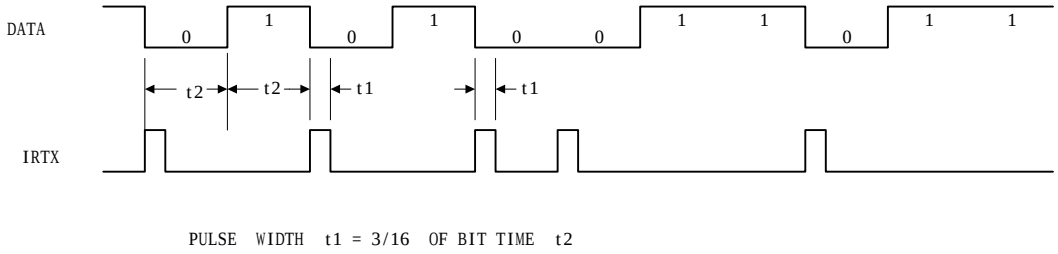


Table 9-10. IrDA Receive Timing of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Pulse Width at 115 kbaud	1.41	1.6	2.71	us
t1	Pulse Width at 57.6 kbaud	2.82	3.22	3.69	us
t1	Pulse Width at 38.4 kbaud	4.23	4.8	5.53	us
t1	Pulse Width at 19.2 kbaud	7.05	9.7	11.07	us
t1	Pulse Width at 9.6 kbaud	14.1	19.5	22.13	us
t1	Pulse Width at 4.8 kbaud	28.2	39	44.27	us
t1	Pulse Width at 2.4 kbaud	56.4	78	88.5	us
t2	Bit Time at 115 kbaud		8.68		us
t2	Bit Time at 57.6 kbaud		17.4		us
t2	Bit Time at 38.4 kbaud		26		us
t2	Bit Time at 19.2 kbaud		52		ms
t2	Bit Time at 9.6 kbaud		104		ms
t2	Bit Time at 4.8 kbaud		208		ms
t2	Bit Time at 2.4 kbaud		416		ms

Note: IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.

9.4.5 IrDA Transmit Timing



PULSE WIDTH t1 = 3/16 OF BIT TIME t2

Table 9-11. IrDA Transmit Timing of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Pulse Width at 115 kbaud	1.41	1.6	2.71	ms
t1	Pulse Width at 57.6 kbaud	2.82	3.22	3.69	ms
t1	Pulse Width at 38.4 kbaud	4.23	4.8	5.53	ms
t1	Pulse Width at 19.2 kbaud	7.05	9.7	11.07	ms
t1	Pulse Width at 9.6 kbaud	14.1	19.5	22.13	ms
t1	Pulse Width at 4.8 kbaud	28.2	39	44.27	ms
t1	Pulse Width at 2.4 kbaud	56.4	78	88.5	ms
t2	Bit Time at 115 kbaud		8.68		ms
t2	Bit Time at 57.6 kbaud		17.4		ms
t2	Bit Time at 38.4 kbaud		26		ms
t2	Bit Time at 19.2 kbaud		52		ms
t2	Bit Time at 9.6 kbaud		104		ms
t2	Bit Time at 4.8 kbaud		208		ms
t2	Bit Time at 2.4 kbaud		416		ms

Note: Criteria for Receive Pulse Detection - A received pulse is considered detected if the pulse width is 1.4 ms minimum.

9.4.6 ASKIR Receive Timing

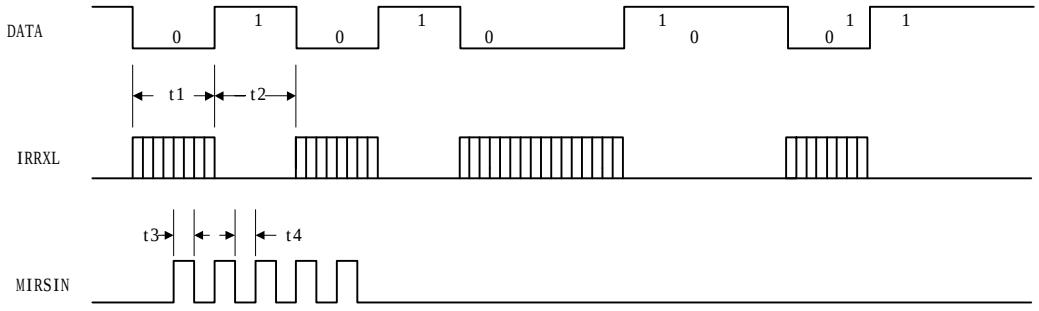


Table 9-12. ASKIR Receive Timing of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Modulated Input Bit Time				us
t2	Off Bit Time				us
t3	Modulated Input "high"	0.8	1	1.2	us
t4	Modulated Input "low"	0.8	1	1.2	us

Note: MIRSIN is the modulated input.

9.4.7 ASKIR Transmit Timing

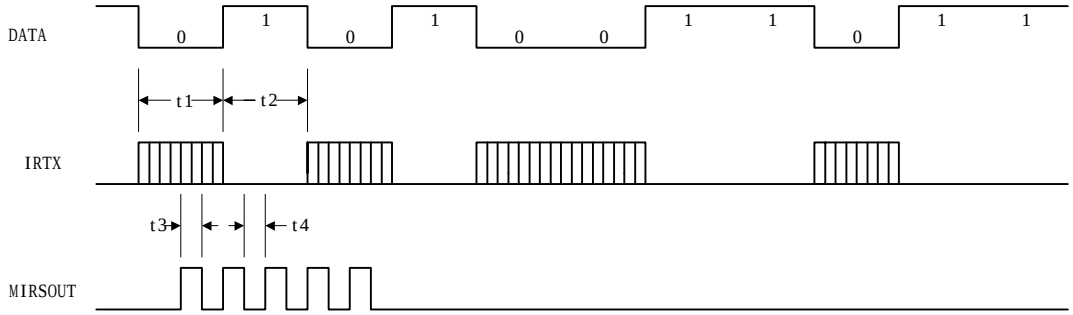


Table 9-13. ASKIR Transmit Timing of Serial Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Modulated Output Bit Time				ms
t2	Off Bit Time				ms
t3	Modulated Output "high"	0.8	1	1.2	ms
t4	Modulated Output "low"	0.8	1	1.2	ms

Note: MIRSOUT is the modulated output.

9.5 Parallel Port Timing

9.5.1 Control Signal Delay Time

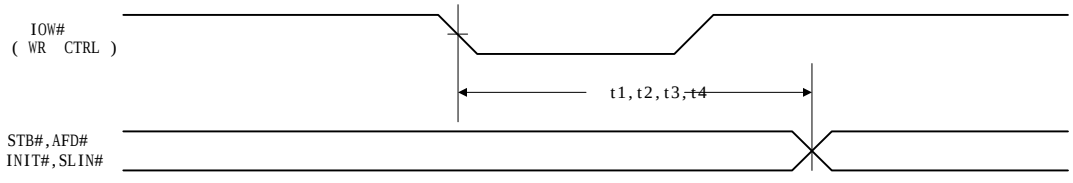


Table 9-14. Control Signal Delay Time of Parallel Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay from IOW# ↓ (WR CTRL PORT) to STB# valid	52			ns
t2	Delay from IOW# ↓ (WR CTRL PORT) to AFD# valid	52			ns
t3	Delay from IOW# ↓ (WR CTRL PORT) to INIT# valid	52			ns
t4	Delay from IOW# ↓ (WR CTRL PORT) to SLIN# valid	52			ns

9.5.2 Interrupt Request Timing

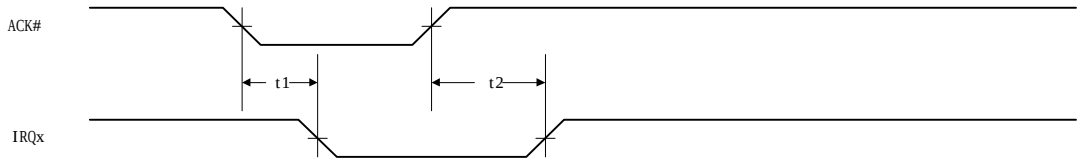


Table 9-15. Interrupt Request Timing of Parallel Port Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	Delay from ACK# ↓ to IRQx ↓			32	ns
t2	Delay from ACK# ↑ to IRQx ↑			16	ns

9.6 EPP Address or DATA WRITE Cycle

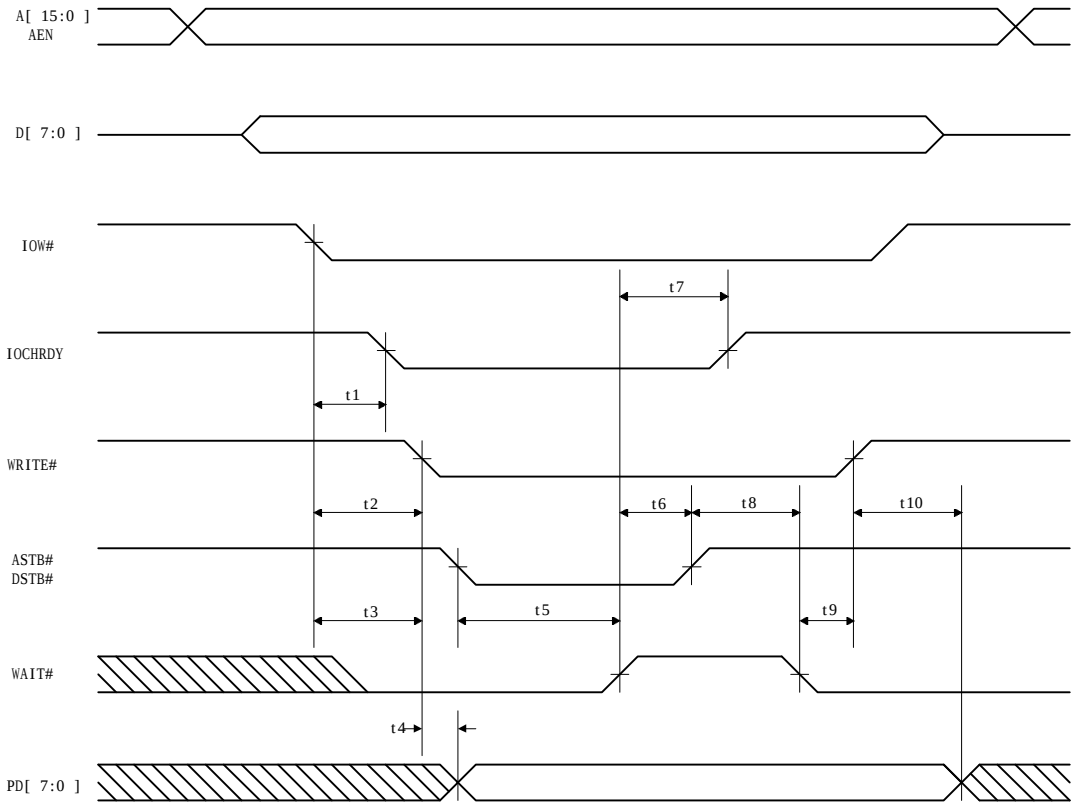


Table 9-16. EPP Address or DATA WRITE Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	IOW# asserted to IOCHRDY asserted	10		70	ns
t2	IOW# asserted to WRITE# asserted	10		70	ns
t3	IOW# asserted to ASTB# or DSTB# asserted	10		70	ns
t4	WRITE# asserted to PD[7:0] valid			70	ns
t5	ASTB# or DSTB# asserted to WAIT# deasserted	0		10	us
t6	WAIT# deasserted to ASTB# or DSTB# deasserted	65		135	ns
t7	WAIT# deasserted to IOCHRDY asserted	65		135	ns
t8	ASTB# or DSTB# deasserted to WAIT# asserted	0			ns
t9	WAIT# asserted to WRITE# deasserted	65			ns
t10	PD[7:0] invalid after WRITE# deasserted	0			ns

9.7 EPP Address or DATA READ Cycle

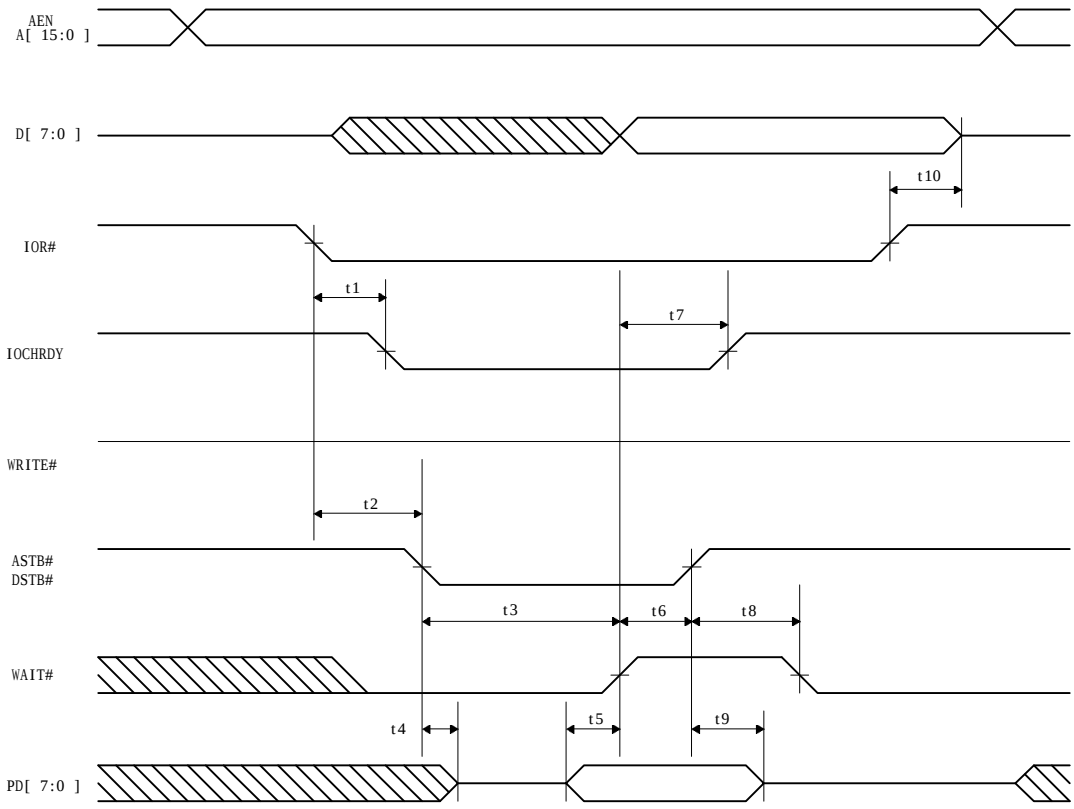


Table 9-17. EPP Address or DATA READ Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	IOR# asserted to IOCHRDY asserted	10		70	ns
t2	IOR# asserted to ASTB# or DSTB# asserted	10		70	ns
t3	ASTB# or DSTB# asserted to WAIT# deasserted			10	us
t4	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			ns
t5	PD[7:0] to WAIT# deasserted	0			ns
t6	WAIT# deasserted to ASTB# or DSTB# deasserted	65		135	ns
t7	WAIT# deasserted to IOCHRDY deasserted	65		135	ns
t8	ASTB# or DSTB# deasserted to WAIT# deasserted	0			ns
t9	PD[7:0] invalid after ASTB# or DSTB# deasserted	20			ns
t10	D[7:0] invalid after IOR# deasserted	0		25	ns

9.8 ECP Parallel Port Forward Timing Diagram

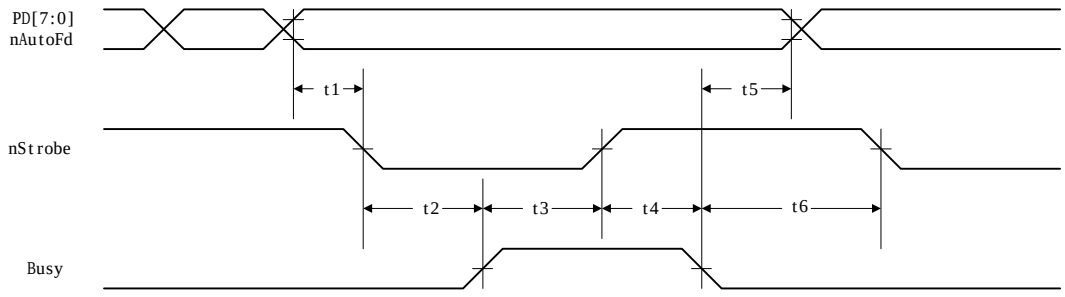


Table 9-18. ECP Parallel Port Forward Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	PD[7:0] & nAutoFd valid to nStrobe asserted	0			ns
t2	nStrobe asserted to busy asserted	0			ns
t3	Busy asserted to nStrobe deasserted (see note)	80		180	ns
t4	nStrobe deasserted to busy deasserted	0			ns
t5	Busy deasserted to PD[7:0] & nAutoFd changed (see note)	80		180	ns
t6	Busy deasserted to nStrobe asserted (see note)	80		180	ns

Note: Maximum value only applies if there is data in the FIFO waiting to be written out.

9.9 ECP Parallel Port Backward Timing Diagram

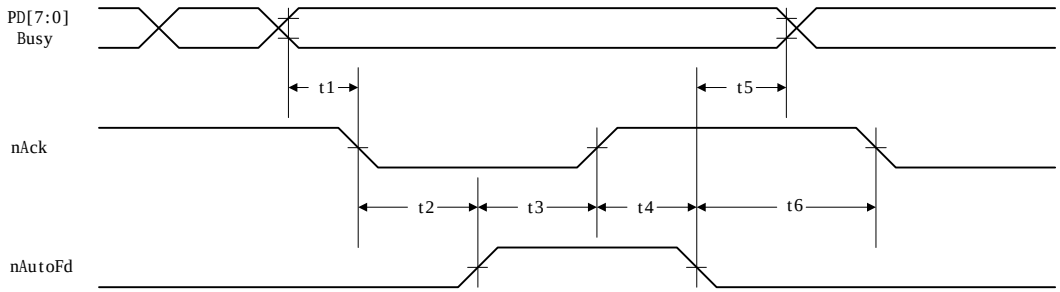


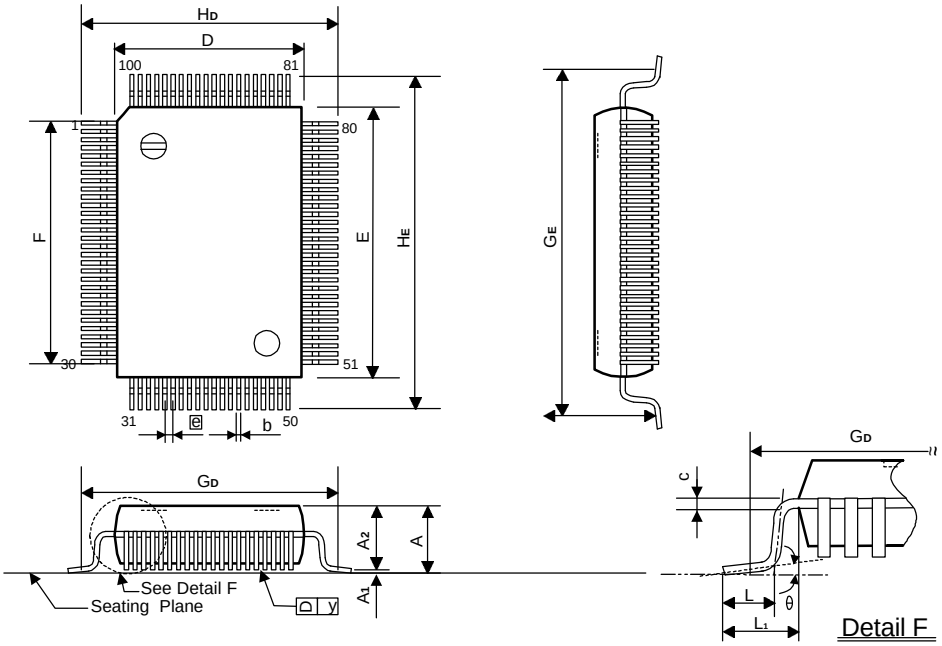
Table 9-19. ECP Parallel Port Backward Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	PD[7:0] & busy valid to nAck asserted	0			ns
t2	nAck asserted to nAutoFd asserted (see note)	80		210	ns
t3	nAutoFd asserted to nAck deasserted	0			ns
t4	nAck deasserted to nAutoFd deasserted (see note)	80		170	ns
t5	nAutoFd deasserted to PD[7:0] & busy changed	90			ns
t6	nAutoFd deasserted to nAck asserted	0			ns

Note: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nAUTOFD low.

10. Package Information

QFP 100L Outline Dimensions unit: inches/mm



Symbol	Dimension in inches	Dimension in mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112 ± 0.005	2.85 ± 0.13
b	0.012 +0.004 −0.002	0.31 +0.10 −0.05
c	0.006 +0.004 −0.002	0.15 +0.10 −0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.787 ± 0.005	20.00 ± 0.13
e	0.026 ± 0.006	0.65 ± 0.15
F	0.742 NOM.	18.85 NOM.
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740 ± 0.012	18.80 ± 0.31
H_E	0.976 ± 0.012	24.79 ± 0.31
L	0.047 ± 0.008	1.19 ± 0.20
L_1	0.095 ± 0.008	2.41 ± 0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:

1. Dimensions D&E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

11. Ordering Information

Part No.	Supports	Package
IT8661F	MIR	100L QFP
IT8661RF	MIR or FIR	100L QFP