INTEGRATED TECHNOLOGY EXPRESS, INC.

# IT8101E and IT8101F

***Windows® CE Intelligent Peripheral Controller***

## Preliminary Specification V0.3

INTEGRATED TECHNOLOGY EXPRESS, INC.



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# Revision History V0.2 – V0.3

**Note: Words in bold lettering in the revisions below indicate the changes. The revisions will also be marked in bold lettering for easy reference.**

| Section | Revision | Page No. |
|---|---|---|
| 1 | • Changed the feature descriptions of **1.3** and **1.4**. | 1 |
| 3 | • Deleted the block **Miniature Interface** from **Figure 3-1**. | 3 |
| 4 | • Changed the description of **Table 4-3**. | 10 |
| | • Changed the description of **Table 4-11**. | 16 |
| 5 | • Added **max.** to the Resolution column of **Table 5-1. LCD Mode** | 19 |
| | • Changed the **bits 6, 3-1** of BITBLTOMDE | 58 |
| 6 | • Deleted " Physical Area 5 and 2 (MCC) " from **Table 6-1. PC Card Controller Register** | 65 |
| | • Deleted Section **6.5.11 Miniature Card Interface Status Register (MCCISR), 6.5.12 Miniature Card General Control Register (MCCGCR), 6.5.13 Miniature Card Status Change Register (MCCSCR),** and **6.5.14 Miniature Card Status Change Interrupt Enable Register (MCCSCIER).** | 79 |
| | • Deleted section **6.6 Miniature Card $I^2C$ Host Controller** | 84 |
| 7 | • Changed **Figure 7-1. AFE Interface Block Diagram** | 81 |
| | • Changed **Table 7-2. Registers of AFE Interface**<br>• Changed the title of section **7.2.1** Control Register (CTR) to **AFE Control Register (ACTR)**, and all CTR were replaced by **ACTR**. | 82 |
| | • Changed the title of section **7.2.2** Status Register (STR) to **AFE Status Register (ASTR),** and all STR were replaced by **ASTR**. Also changed the description of bits 14, 3 and 2. | 84 |
| | • Changed the title of section **7.2.3** Transmit Data Register (TXDR) to **AFE Transmit Data Register (ATXDR),** and all TXDR were replaced by **ATXDR**.<br>• Changed the title of section **7.2.4** Receive Data Register (RXDR) to **AFE Receive Data Register (ARXDR),** and all RXDR were replaced by **ARXDR.** | 86 |
| | • Changed the title of section **7.2.5** Transmit Data Buffers (TXDB0,1) to **AFE Transmit Data Buffers (ATXDB0,1),** and all TXDB0 and 1 were replaced by **ATXDB0 and 1**.<br>• Changed the title of section **7.2.6** Transmit Shift Register (TSFTR) to **AFE Transmit Shift Register (ATSFTR),** and all TSFTR were replaced by **ATSFTR.**<br>• Changed the title of section **7.2.7** Receive Data Buffers (RXDB0,1) to **AFE Receive Data Buffers (ARXDB0,1),** and all RXDB0 and 1 were replaced by **ARXDB0 and 1.**<br>• Changed the title of section **7.2.8** Receive Shift Register (RSFTR) to **AFE Receive Shift Register (ARSFTR),** and all RSFTR were replaced by **ARSFTR.** | 87 |
| | • Added a paragraph **The procedure required to …..in Figures 7.4/7.5**. | 91 |
| | • Added a sentence **Receiving data requires….and SCLK**. to section **7.7.2**. | 92 |

## Revision History V0.2 – V0.3 (cont'd)

| Section | Revision | Page No. |
|---|---|---|
| 8 | • Changed **Table 8-1. The List of I/O Port Pin Function Configurations**. | 93 |
| 9 | • Deleted **LCDC, Miniature card and I2C** form section 9.1 Overview.<br>• Deleted **LCDC, Miniature and I2C** form F**igure 9-1. Block Diagram of the Interrupt Controller.** | 98 |
| | • Changed the R/W column of Interrupt Request register to **R**.<br>• Deleted **LCD Controller (LCDC) and $I^2C$** form the list of section **9.2.1**. | 100 |
| | • Deleted **LCDC, Miniature card and $I^2C$** from the description of section **9.3**.<br>• Changed bits **15, 8 and 7** of section **9.3** to reserved, and all R/O were changed to **R**. | 100 |
| | • Deleted **LCDC, Miniature card and I2C** from the description of section **9.4**.<br>• Changed bits **15, 8 and 7** of section **9.3** to **reserved**. | 101 |
| 10 | • Added **Access Size: 16 bits** to **Address: H'10000000**, and changed the descriptions of bits 15-9. | 103 |
| | • Added **Access Size: 16 bits** to **Address: H'10000002.** Changed the bit name of bit 10 from "SF_decode" to "-." Changed the descriptions of bits 13-8, 6,4, 1-0. | 104 |
| | • Added **Access Size: 16 bits** to **Address: H'10000004**, and changed the description of bit 4. | 106 |
| 11 | • Deleted as **MODE=00/10** from descriptions of **11.1.3 Pin Configuration**. | 110 |
| | • Changed the tile of section **11.2.8** TIMR: Timer Interrupt Mask Register to TIMR: Timer Interrupt **Enable** Register.<br>• Changed the name of bits 1: TMU1M and 0: TMU0M to **TMU1E** and **TMU0E.** | 115 |
| | • Changed the **ID[15:0]** of **Figure 11-3**. | 117 |
| 12 | • Replaced **Figure 12-1 Functional Block Diagram of FIR** with a new one. | 120 |
| | • Added 2 lines to the end of **Table 12-1. Summary of FIR Controller Registers**. | 122 |
| | • Added register name list table to every section in **12.2.3 Register Description** | 123 |
| | • Added a new section (**25) FIR Configuration register** to the end of 12.2.3 Register Description. | 138 |
| 13 | • Added a register table in section **(4) Divisor Latches** | 144 |
| | • MCR were all replaced by **UMCR** in Table 13-4. **Modem Control Register Bits**. | 146 |
| | • Added section **13.9 Caution** to the end of this chapter. | 151 |
| 15 | • Changed the MIn. and Max value of **Table 15-1, 15-2, 15-3, 15-4, 15-5 and 15-6** | 153 |
| | • Replaced Table 15-8, 15-9 and 15-10 with new tables. | 156 |
| | • Added Table 15-11, 15-12 and 15-13. | 157 |
| | • In Figure 15-18, changed tCAS to **tCAS1** and **tCAS2**<br>• In Figure 15-19, changed tCSB to **tCSR** | 167 |
| | • Replaced Figure **15-22** with a new one. | 169 |

# CONTENTS

# TABLES

**Page**



# FIGURES

**Page**

## 1. Features

### 1.1 CPU Interface

- Supports Hitachi SH7709 CPU Interface
- 3.3 V

### 1.2 LCD Controller

- Color/Monochrome STN-LCD direct interface
  - 64, 16, 4, 2 gray scales
  - 256/256K and 64K colors
- Supports CRT interface (VESA VGA)
- Display resolution 640 x 240 for LCD, 640 x 480 for CRT
- Supports CRT and LCD simultaneous display
- Ten (10) types of BitBLT hardware acceleration
- Solid line drawing based upon Bresenham Parameter
- Rectangular solid color fill function
- Supports 256KX16 bit EDO-DRAM
- 4/8 bit display interface
- Supports STANDBY Mode

### 1.3 PCMCIA Controller

- PCMCIA PC card standard v2.1 compliant
- Miniature card spec. v1.1 compliant
- Supports PCMCIA memory and IO card at area 6
- Supports PCMCIA memory card at area 5.

### 1.4 AFE Interface

- Supports SGS-THOMSON STL7550 interface
- Supports STANDBY Mode

### 1.5 GPIO Function

- GPIO pins can be programmable Input, Output or Interrupt input pins.
- Internal pull-up resistor ON/OFF control
- Interrupt events can be independently generated or masked on each I/O pin.
- Power down control by software (input gated and output floating)

### 1.6 Interrupt

- Only one external interrupt output pin is used for SH7709 External interrupt input.
- The priority order of interrupt request lines is determined by software.
- Module interrupts can be masked on/off.

### 1.7 Power Management

- Supports STANDBY Mode for each module.
- AFE, LCD, UART clock input can be stopped.
- IrDA clock input can be gated.
- The CPU input signals can be gated.

### 1.8 Timer

- 2-channel 16-bit timer with prescale (1, 1/4, 1/8, 1/16)
- Supports STANDBY Mode

### 1.9 IrDA

- Supports HP SIR or ASKIR infrared interface
- Supports MIR and FIR
- Provides DMA channel mode for FIR

### 1.10 UART

- Standard 16550 compatible

### 1.11 Package

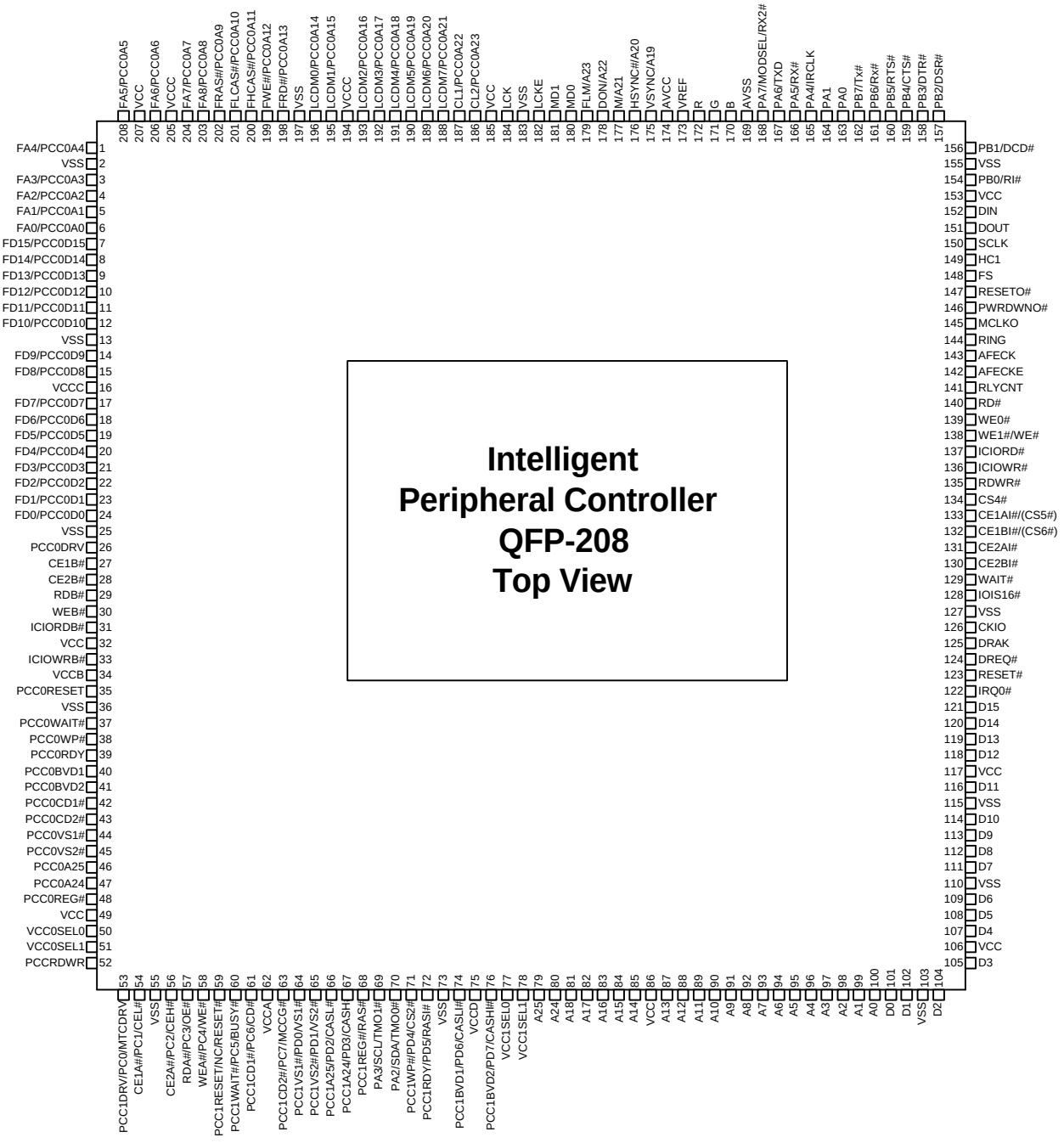
- IT8101E: 208-pin LQFP
- IT8101F: 208-pin PQFP

## 2. General Description

This Controller LSI, directly connected to SH7709, integrates a color LCD controller, a PCMCIA controller, an analog front end (AFE) interface, an I/O port, a timer, the UART, etc. This chip architecture features two-chip solution for PDA/HPC with a color LCD.

# 3. Pin Configuration and Block Diagram

## 3.1 Pin Configuration




AVCC*1 for analog group (170-173)
AVSS*1 for analog group (170-173)
VSS*13 GND (for other I/O cell)

VCCA*1 for PCC (54, 56-60, 66-**68**)
VCCB*1 for PCC (27-31, 33, 35, 37-41, 46-48)
VCCC*3 for address / data buffer of PCC0 or LCDC (1, 3-12, 14, 15, 17-24, 186-193, 195, 196, 198-204, 206, 208)
VCCD*1 for pins 71, 72, 74 and 76
VCC*8 3.3V (for other I/O cell)

### 3.2 Block Diagram

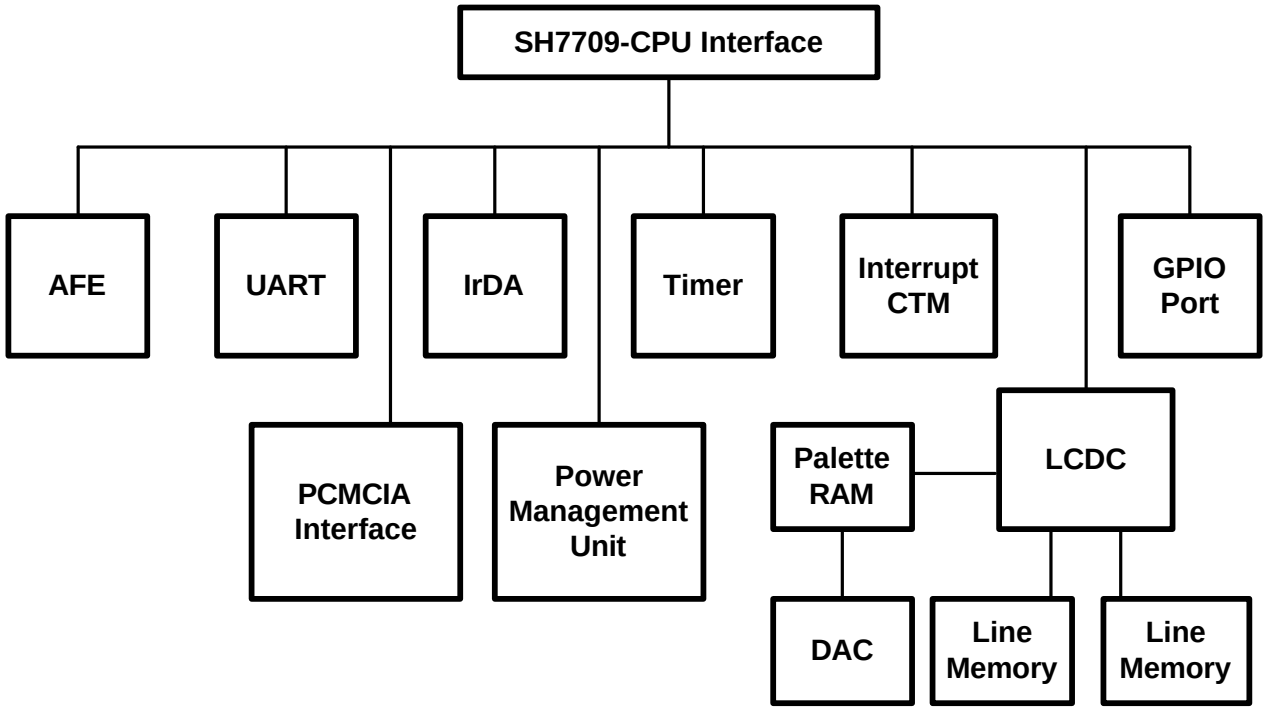



**Figure 3-1. IT8101E and IT8101F Block Diagram**

### 3.3 Physical Address Space Map

This LSI is directly connected to SH7709 on Area 4 (Fig3-2). SH7709 can access the internal registers on the Intelligent Peripheral Controller. Frame memory is accessed on Area 4.

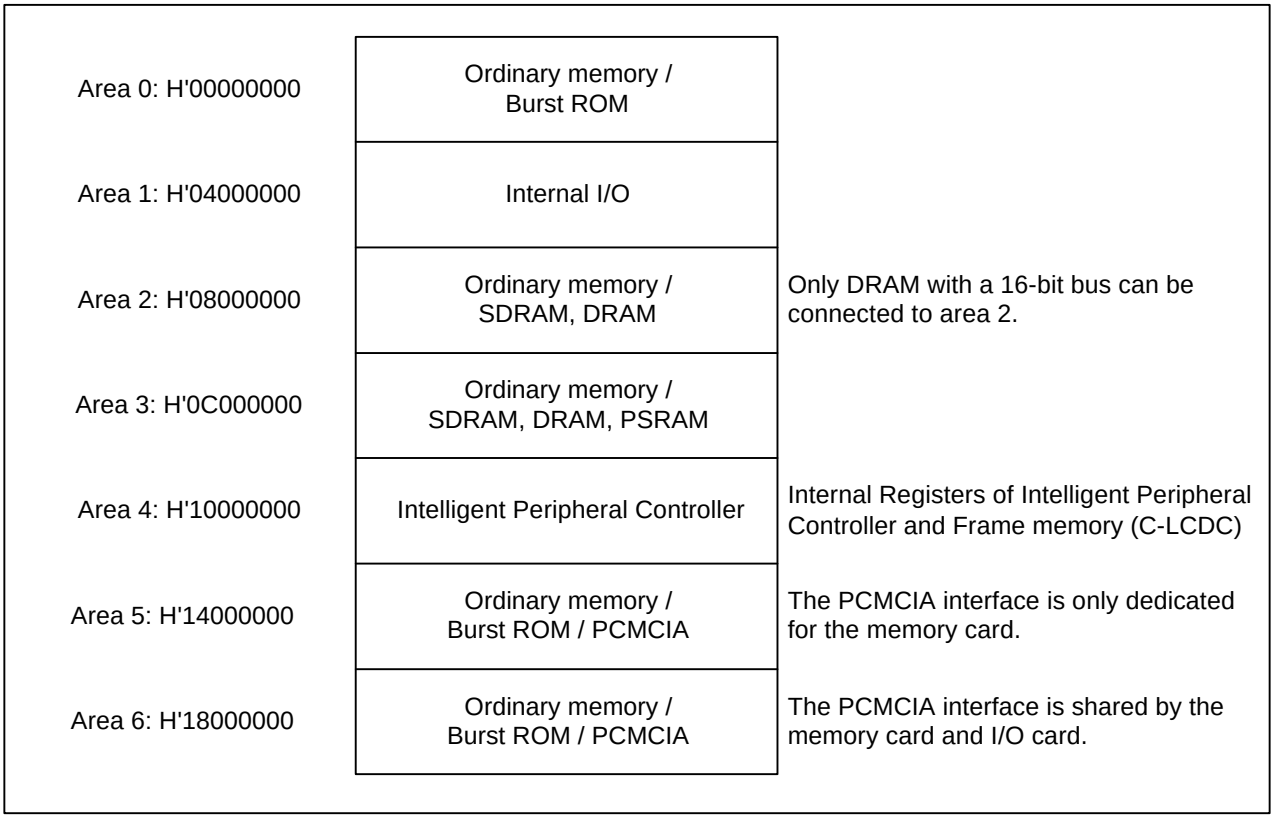



**Figure 3-2. IT8101 and IT8101F Physical Address Space Map**

### 3.4 SH7709 CPU Interface Access Timing

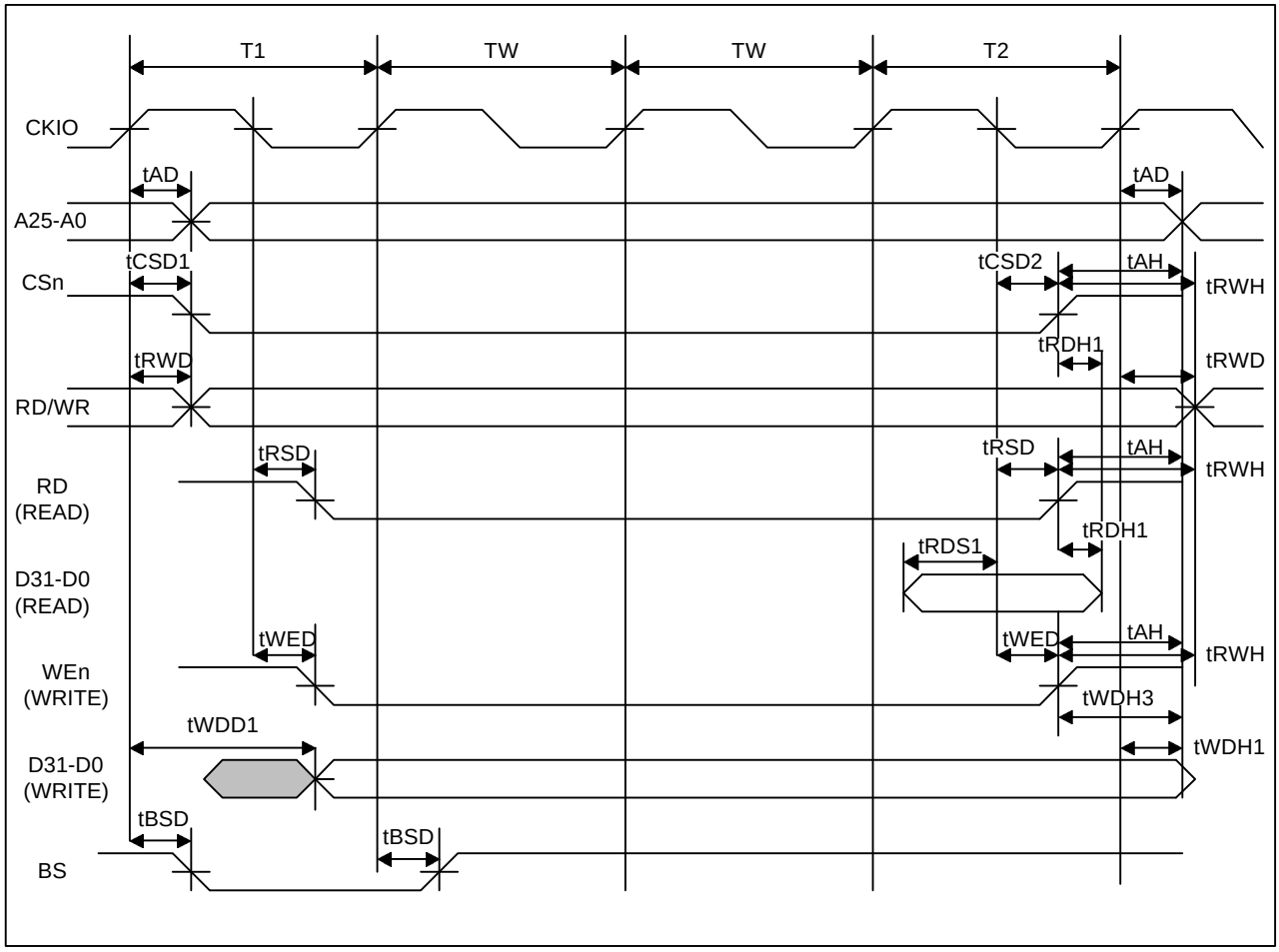



**Figure 3-3. Basic Bus Cycle**

## 4. IT8101E and IT8101F Pin Descriptions

The Intelligent Peripheral Controller comes in two packages: 208-pin LQFP (Low Profile Quad Flat Package) for IT8101E and 208 PQFP (Plastic Quad Flat Package) for IT8101F. The controller comprises three (3) categories: 179 signal balls, fifteen (15) power balls and fourteen (14) ground balls.

**Table 4-1. Signal Names (by pin numbers in alphabetical order )**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | FA4/PCC0A4 | 22 | FD2/PCC0D2 | 43 | PCC0CD2# | 64 | PCC1VS1#/PD0/ VS1# |
| 2 | VSS | 23 | FD1/PCC0D1 | 44 | PCC0VS1# | 65 | PCC1VS2#/PD1/ VS2# |
| 3 | FA3/PCC0A3 | 24 | FD0/PCC0D0 | 45 | PCC0VS2# | 66 | PCC1A25/PD2/ CASL# |
| 4 | FA2/PCC0A2 | 25 | VSS | 46 | PCC0A25 | 67 | PCC1A24/PD3/ CASH# |
| 5 | FA1/PCC0A1 | 26 | PCC0DRV | 47 | PCC0A24 | 68 | PCC1REG#/RAS# |
| 6 | FA0/PCC0A0 | 27 | CE1B# | 48 | PCC0REG# | 69 | PA3/SCL/TMO1# |
| 7 | FD15/PCC0D15 | 28 | CE2B# | 49 | VCC | 70 | PA2/SDA/TMO0# |
| 8 | FD14/PCC0D14 | 29 | RDB# | 50 | VCC0SEL0 | 71 | PCC1WP#/PD4/ CS2# |
| 9 | FD13/PCC0D13 | 30 | WEB# | 51 | VCC0SEL1 | 72 | PCC1RDY/PD5/ RASI# |
| 10 | FD12/PCC0D12 | 31 | ICIORDB# | 52 | PCCRDWR | 73 | VSS |
| 11 | FD11/PCC0D11 | 32 | VCC | 53 | PCC1DRV/PC0/ MTCDRV | 74 | PCC1BVD1/PD6/ CASLI# |
| 12 | FD10/PCC0D10 | 33 | ICIOWRB# | 54 | CE1A#/PC1/CEL# | 75 | VCCD |
| 13 | VSS | 34 | VCCB | 55 | VSS | 76 | PCC1BVD2/PD7/ CASHI# |
| 14 | FD9/PCC0D9 | 35 | PCC0RESET | 56 | CE2A#/PC2/CEH# | 77 | VCC1SEL0 |
| 15 | FD8/PCC0D8 | 36 | VSS | 57 | RDA#/PC3/OE# | 78 | VCC1SEL1 |
| 16 | VCCC | 37 | PCC0WAIT# | 58 | WEA#/PC4/WE# | 79 | A25 |
| 17 | FD7/PCC0D7 | 38 | PCC0WP# | 59 | PCC1RESET/NC/ RESET# | 80 | A24 |
| 18 | FD6/PCC0D6 | 39 | PCC0RDY | 60 | PCC1WAIT#/PC5/ BUSY# | 81 | A18 |
| 19 | FD5/PCC0D5 | 40 | PCC0BVD1 | 61 | PCC1CD1#/PC6/ CD# | 82 | A17 |
| 20 | FD4/PCC0D4 | 41 | PCC0BVD2 | 62 | VCCA | 83 | A16 |
| 21 | FD3/PCC0D3 | 42 | PCC0CD1# | 63 | PCC1CD2#/PC7/ MCCG# | 84 | A15 |

**Table 4-1. Signal Names (by pin numbers in alphabetical order ) [cont'd]**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 85 | A14 | 116 | D11 | 147 | RESETO# | 178 | DON/A22 |
| 86 | VCC | 117 | VCC | 148 | FS | 179 | FLM/A23 |
| 87 | A13 | 118 | D12 | 149 | HC1 | 180 | MD0 |
| 88 | A12 | 119 | D13 | 150 | SCLK | 181 | MD1 |
| 89 | A11 | 120 | D14 | 151 | DOUT | 182 | LCKE |
| 90 | A10 | 121 | D15 | 152 | DIN | 183 | VSS |
| 91 | A9 | 122 | IRQ0# | 153 | VCC | 184 | LCK |
| 92 | A8 | 123 | RESET# | 154 | PB0/RI# | 185 | VCC |
| 93 | A7 | 124 | DREQ# | 155 | VSS | 186 | CL2/PCC0A23 |
| 94 | A6 | 125 | DRAK | 156 | PB1/DCD# | 187 | CL1/PCC0A22 |
| 95 | A5 | 126 | CKIO | 157 | PB2/DSR# | 188 | LCDM7/PCC0A21 |
| 96 | A4 | 127 | VSS | 158 | PB3/DTR# | 189 | LCDM6/PCC0A20 |
| 97 | A3 | 128 | IOIS16# | 159 | PB4/CTS# | 190 | LCDM5/PCC0A19 |
| 98 | A2 | 129 | WAIT# | 160 | PB5/RTS# | 191 | LCDM4/PCC0A18 |
| 99 | A1 | 130 | CE2BI# | 161 | PB6/Rx# | 192 | LCDM3/PCC0A17 |
| 100 | A0 | 131 | CE2AI# | 162 | PB7/Tx# | 193 | LCDM2/PCC0A16 |
| 101 | D0 | 132 | CE1BI#/(CS6#) | 163 | PA0 | 194 | VCCC |
| 102 | D1 | 133 | CE1AI#/(CS5#) | 164 | PA1 | 195 | LCDM1/PCC0A15 |
| 103 | VSS | 134 | CS4# | 165 | PA4/IRCLK | 196 | LCDM0/PCC0A14 |
| 104 | D2 | 135 | RDWR# | 166 | PA5/RX# | 197 | VSS |
| 105 | D3 | 136 | ICIOWR# | 167 | PA6/TXD | 198 | FRD#/PCC0A13 |
| 106 | VCC | 137 | ICIORD# | 168 | PA7/MODSEL/ RX2# | 199 | FWE#/PCC0A12 |
| 107 | D4 | 138 | WE1#/WE# | 169 | AVSS | 200 | FHCAS#/ PCC0A11 |
| 108 | D5 | 139 | WE0# | 170 | B | 201 | FLCAS#/ PCC0A10 |
| 109 | D6 | 140 | RD# | 171 | G | 202 | FRAS#/PCC0A9 |
| 110 | VSS | 141 | RLYCNT | 172 | R | 203 | FA8/PCC0A8 |
| 111 | D7 | 142 | AFECKE | 173 | VREF | 204 | FA7/PCC0A7 |
| 112 | D8 | 143 | AFECK | 174 | AVCC | 205 | VCCC |
| 113 | D9 | 144 | RING | 175 | VSYNC/A19 | 206 | FA6/PCC0A6 |
| 114 | D10 | 145 | MCLKO | 176 | HSYNC#/A20 | 207 | VCC |
| 115 | VSS | 146 | PWRDWNO# | 177 | M/A21 | 208 | FA5/PCC0A5 |

**Table 4-2. Signal Names (by symbols in alphabetical order)**

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|---|---|---|---|---|---|---|---|
| A0 | 100 | CE2AI# | 131 | FA3/PCC0A3 | 3 | HSYNC#/A20 | 176 |
| A1 | 99 | CE2B# | 28 | FA4/PCC0A4 | 1 | ICIORD# | 137 |
| A2 | 98 | CE2BI# | 130 | FA5/PCC0A5 | 208 | ICIORDB# | 31 |
| A3 | 97 | CL1/PCC0A22 | 187 | FA6/PCC0A6 | 206 | ICIOWR# | 136 |
| A4 | 96 | CL2/PCC0A23 | 186 | FA7/PCC0A7 | 204 | ICIOWRB# | 33 |
| A5 | 95 | CKIO | 126 | FA8/PCC0A8 | 203 | IOIS16# | 128 |
| A6 | 94 | CS4# | 134 | FD0/PCC0D0 | 24 | IRQ0# | 122 |
| A7 | 93 | D0 | 101 | FD1/PCC0D1 | 23 | LCDM0/PC0A14 | 196 |
| A8 | 92 | D1 | 102 | FD2/PCC0D2 | 22 | LCDM1/PC0A15 | 195 |
| A9 | 91 | D2 | 104 | FD3/PCC0D3 | 21 | LCDM2/PC0A16 | 193 |
| A10 | 90 | D3 | 105 | FD4/PCC0D4 | 20 | LCDM3/PC0A17 | 192 |
| A11 | 89 | D4 | 107 | FD5/PCC0D5 | 19 | LCDM4/PC0A18 | 191 |
| A12 | 88 | D5 | 108 | FD6/PCC0D6 | 18 | LCDM5/PC0A19 | 190 |
| A13 | 87 | D6 | 109 | FD7/PCC0D7 | 17 | LCDM6/PC0A20 | 189 |
| A14 | 85 | D7 | 111 | FD8/PCC0D8 | 15 | LCDM7/PC0A21 | 188 |
| A15 | 84 | D8 | 112 | FD9/PCC0D9 | 14 | LCK | 184 |
| A16 | 83 | D9 | 113 | FD10/PCC0D10 | 12 | LCKE | 182 |
| A17 | 82 | D10 | 114 | FD11/PCC0D11 | 11 | M/A21 | 177 |
| A18 | 81 | D11 | 116 | FD12/PCC0D12 | 10 | MCLKO | 145 |
| A24 | 80 | D12 | 118 | FD13/PCC0D13 | 9 | MD0 | 180 |
| A25 | 79 | D13 | 119 | FD14/PCC0D14 | 8 | MD1 | 181 |
| AFECK | 143 | D14 | 120 | FD15/PCC0D15 | 7 | PA0 | 163 |
| AFECKE | 142 | D15 | 121 | FHCAS#/ PCC0A11 | 200 | PA1 | 164 |
| AVCC | 174 | DIN | 152 | FLCAS#/ PCC0A10 | 201 | PA2/SDA/ TMO0# | 70 |
| AVSS | 169 | DOUT | 151 | FLM/A23 | 179 | PA3/SCL/TMO1# | 69 |
| B | 170 | DRAK | 125 | FRAS#/PCC0A9 | 202 | PA4/IRCLK | 165 |
| CE1A#/PC1/CEL# | 54 | DREQ# | 124 | FRD#/PCC0A13 | 198 | PA5/RX# | 166 |
| CE1AI#/(CS5#) | 133 | DON/A22 | 178 | FS | 148 | PA6/TXD | 167 |
| CE1B# | 27 | FA0/PCC0A0 | 6 | FWE#/PCC0A12 | 199 | PA7/MODSEL/ RX2# | 168 |
| CE1BI#/(CS6#) | 132 | FA1/PCC0A1 | 5 | G | 171 | PB0/RI# | 154 |
| CE2A#/PC2/ CEH# | 56 | FA2/PCC0A2 | 4 | HCI | 149 | PB1/DCD# | 156 |

**Table 4-2. Signal Names (by symbols in alphabetical order) [cont'd]**

| Signal | Pin | Signal | Pin | Signal | Pin |
|---|---|---|---|---|---|
| PB2/DSR# | 157 | PCC1BVD1/PD6 /CASLI# | 74 | RLYCNT | 141 |
| PB3/DTR# | 158 | PCC1BVD2/PD7 /CASHI# | 76 | SCLK | 150 |
| PB4/CTS# | 159 | PCC1CD1#/PC6 /CD# | 61 | VCC0SEL0 | 50 |
| PB5/RTS# | 160 | PCC1CD2/PC7/ MCCG# | 63 | VCC0SEL1 | 51 |
| PB6/Rx# | 161 | PCC1DRV/PC0/ MTCDRV | 53 | VCC1SEL0 | 77 |
| PB7/Tx# | 162 | PCC1RDY/PD5/ RASI# | 72 | VCC1SEL1 | 78 |
| PCC0A24 | 47 | PCC1RESET/ NC/RESET# | 59 | VCCA | 62 |
| PCC0A25 | 46 | PCC1REG#/ RAS# | 68 | VCCB | 34 |
| PCC0BVD1 | 40 | PCC1WAIT#/ PC5/BUSY# | 60 | VCCD | 75 |
| PCC0BVD2 | 41 | PCC1WP#/PD4/ CS2# | 71 | VREF | 173 |
| PCC0CD1# | 42 | PCC1VS1#/PD0 /VS1# | 64 | VSYNC/A19 | 175 |
| PCC0CD2# | 43 | PCC1VS2#/PD1 /VS2# | 65 | WE0# | 139 |
| PCC0DRV | 26 | PCCRDWR | 52 | WE1#/WE# | 138 |
| PCC0RDY | 39 | PWRDWNO# | 146 | WAIT# | 129 |
| PCC0REG# | 48 | R | 172 | WEB# | 30 |
| PCC0RESET | 35 | RD# | 140 | WEA#/PC4/WE # | 58 |
| PCC0VS1# | 44 | RDA#/PC3/OE# | 57 | VCC | 32, 49, 86, 106, 117, 153, 185, 207 |
| PCC0VS2# | 45 | RDB# | 29 | VCCC | 16, 194, 205 |
| PCC0WAIT# | 37 | RDWR# | 135 | VSS | 2, 13, 25, 36, 55, 73, 103, 110, 115, 127, 155, 183, 197 |
| PCC0WP# | 38 | RESET# | 123 | | |
| PCC1A24/PD3/ CASH# | 67 | RESETO# | 147 | | |
| PCC1A25/PD2/ CASL# | 66 | RING | 144 | | |

**Table 4-3. Pin Descriptions of Mode Select**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **Mode Select** | | | |
| 181-180 | MD1-MD0 | I | System Configuration Mode select (MD1, MD0)<br>00 - PCMCIA card 0 with the external address/data buffer<br>PCMCIA card 1 with the external address/data buffer<br>Port A[7:4] / IrDA<br>Port A[3:2] / Timer 1, 0<br>Port A[1:0]<br>Port B / UART<br>AFE Interface<br>LCDC with CRT<br>10 - PCMCIA card 0 with the external address/data buffer<br>Port A[7:4]/ IrDA<br>Port A[3:2] / Timer 1, 0<br>Port A[1:0]<br>Port B / UART<br>Port C<br>Port D<br>AFE Interface<br>LCDC with CRT |

**Table 4-4. Pin Descriptions of SH7709 Interface**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **SH7709 Interface** | | | |
| 79 | A25 | I | Address bus |
| 80 | A24 | I | Address bus |
| 81-85, 87-100 | A18-A0 | I | Address bus |
| 121-118, 116, 114-111, 109-107, 105, 104, 102, 101 | D15-D0 | IO | Data bus |
| 134 | CS4# | I | Chip select 4 |
| 126 | CKIO | I | System clock |
| 133 | CE1AI#/ (CS5#) | I | Chip enable 1 for PCMCIA card 1 |
| 132 | CE1BI#/ (CS6#) | I | Chip enable 1 for PCMCIA card 0 |
| 131 | CE2AI# | I | Chip enable 2 for PCMCIA card 1 |
| 130 | CE2BI# | I | Chip enable 2 for PCMCIA card 0 |
| 139 | WE0# | I | D7-D0 write strobe signal |
| 138 | WE1#/WE# | I | D15-D8 write strobe signal, or PCMCIA write strobe signal |
| 135 | RDWR# | I | Data bus direction indicator signal |
| 140 | RD# | I | Strobe signal indicating the read cycle |
| 128 | IOIS16# | O | Write protect I/O is 16 bits for PC card 0. |
| 136 | ICIOWR# | I | PCMCIA card 0 I/O write |
| 137 | ICIORD# | I | PCMCIA card 0 I/O read |
| 123 | RESET# | I | RESET request |
| 129 | WAIT# | O | Wait state request signal |
| 124 | DREQ# | O | DMA request signal |
| 125 | DRAK | I | DMA request acknowledge |
| 122 | IRQ0# | O | Interrupt request output to SH7709 from the Intelligent Peripheral Controller |

**Table 4-5. Pin Descriptions of Port B, Port A and I/O Port A**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **Port B (multifunction with UART)** | | | |
| 162 | PB7/Tx# | IO/O | Multifunction pin: Port B bit 7 for GPIO / Data output for UART |
| 161 | PB6/Rx# | IO/I | Multifunction pin: Port B bit 6 for GPIO / Data input for UART |
| 160 | PB5/RTS# | IO/O | Multifunction pin: Port B bit 5 for GPIO / Request to Send Output for UART |
| 159 | PB4/CTS# | IO/I | Multifunction pin: Port B bit 4 for GPIO / Clear to Send Input for UART |
| 158 | PB3/DTR# | IO/O | Multifunction pin: Port B bit 3 for GPIO / Data Terminal Ready Output for UART |
| 157 | PB2/DSR# | IO/I | Multifunction pin: Port B bit 2 for GPIO / Data Set Ready for UART |
| 156 | PB1/DCD# | IO/I | Multifunction pin: Port B bit 1 for GPIO / Receive Line Signal Detect for UART |
| 154 | PB0/RI# | IO/I | Multifunction pin: Port B bit 0 for GPIO / Ring Indicator for UART |
| **Port A (multifunction with IrDA)** | | | |
| 168 | PA7 /MODSEL /RX2# | IO/O /I | Multifunction pin: Port A bit 7 for GPIO. For IrDA, Low frequency infrared / High frequency infrared select/Low frequency infrared data stream in |
| 167 | PA6/TXD | IO/O | Multifunction pin: Port A bit 6 for GPIO / Infrared data stream output for IrDA |
| 166 | PA5/RX# | IO/I | Multifunction pin: Port A bit 5 for GPIO / High frequency infrared data stream input for IrDA |
| 165 | PA4/IRCLK | IO/I | Multifunction pin: Port A bit 4 for GPIO / Clock for IrDA |
| **I/O Port A** | | | |
| 164 | PA1 | IO | Port A bit 1 for GPIO |
| 163 | PA0 | IO | Port A bit 0 for GPIO |

**Table 4-6. Pin Descriptions of AFE Interface**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **AFE Interface** | | | |
| 141 | RLYCNT | O | This signal is used for RLY Control and Dial Pulse Output Pin. |
| 142 | AFECKE | I/O | Crystal Oscillator Output Pin for AFE clock |
| 143 | AFECK | I | Crystal Oscillator input Pin for AFE clock |
| 144 | RING | I | Ringing Signal Input Pin |
| 145 | MCLKO | O | Master Clock to AFE module |
| 146 | PWRDWNO # | O | AFE Control 2 Output Pin (CNT2). This signal outputs to control AFE module. |
| 147 | RESETO# | O | AFE Control 1 Output Pin (CNT1). This signal outputs to control AFE module. |
| 148 | FS | I | Frame Sync Signal Input Pin. This signal comes form AFE module FS. |
| 149 | HC1 | O | This output signal is used for Hardware Control Signal 1 (STLC7546). |
| 150 | SCLK | I | Shift Clock Input Pin. This signal comes from AFE module SCLK. |
| 151 | DOUT | I | Serial Receive Data Input Pin (RxD). This signal comes from AFE module DOUT. |
| 152 | DIN | O | Serial Transmit Data Output Pin (TxD). This signal outputs to control AFE module DI. |

**Table 4-7. Pin Descriptions of LCD Interface**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **LCD Interface** | | | |
| 184 | LCK | I | Crystal Oscillator input pin for LCD clock |
| 182 | LCKE | I/O | Crystal Oscillator output pin for LCD clock |
| 188-193, 195, 196 | LCDM7-0 /PC0A21-14 | O/O | Multifunction pin: Output data bus for LCD module / Address bus for PCMCIA card 0 |
| 187 | CL1 /PCC0A22 | O/O | Multifunction pin: Display data latch clock for LCD module / Address bus for PCMCIA card 0 |

**Table 4-7. Pin Descriptions of LCD Interface (cont'd)**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **LCD Interface** | | | |
| 186 | CL2 /PCC0A23 | O/O | Multifunction pin: Display data shift clock for LCD module / Address bus for PCMCIA card 0 |
| 179 | FLM/A23 | O/I | Multifunction pin: First line marker for LCD module / Address 23 from the CPU |
| 178 | DON/A22 | O/I | Multifunction pin: Display ON/OFF control for LCD module / Address 22 from the CPU |
| 177 | M/A21 | O/I | Multifunction pin: Converts liquid crystal drive output to AC for LCD module / Address 21 from the CPU |

**Table 4-8. Pin Descriptions of Frame Memory (DRAM) Interface**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **Frame Memory (DRAM) Interface** | | | |
| 203, 204, 206, 208, 1, 3-6 | FA8-0 /PCC0A8-0 | O/O | Multifunction pin : Frame memory address bus / PCMCIA card 0 address bus |
| 202 | FRAS# /PCC0A9 | O/O | Multifunction pin : Row Address Strobe for Frame Memory / PCMCIA card 0 address bus |
| 201 | FLCAS# /PCC0A10 | O/O | Multifunction pin : Low Byte Column Address Strobe for Frame Memory / PCMCIA card 0 address bus |
| 200 | FHCAS# /PCC0A11 | O/O | Multifunction pin : High Byte Column Address Strobe for Frame Memory / PCMCIA card 0 address bus |
| 199 | FWE# /PCC0A12 | O/O | Multifunction pin : Frame Memory Write Strobe / PCMCIA card 0 address bus |
| 198 | FRD# /PCC0A13 | O/O | Multifunction pin : Frame Memory Read Strobe / PCMCIA card 0 address bus |
| 7-12, 14, 15, 17-24 | FD15-0 /PCC0D15-0 | IO/IO | Multifunction pin : Frame Memory Data Bus / PCMCIA card 0 data bus / PCMCIA Card 0 Data Bus |

**Table 4-9. Pin Descriptions of CRT Interface**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **CRT Interface** | | | |
| 172 | R | O | DAC Analog Red signal output for CRT Display |
| 171 | G | O | DAC Analog Green signal output for CRT Display |
| 170 | B | O | DAC Analog Blue signal output for CRT Display |
| 173 | VREF | I | Reference Voltage |
| 176 | HSYNC#/A20 | O/I | Multifunction Pin : Horizontal Synchronization signal for CRT Display / Address 20 from the CPU |
| 175 | VSYNC/A19 | O/I | Multifunction Pin : Vertical Synchronization signal for CRT Display / Address 19 from the CPU |

**Table 4-10. Pin Descriptions of PCMCIA Card 0**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **PCMCIA 0 (Memory and I/O)** | | | |
| 52 | PCCRDWR | O | Control PCMCIA card 0, PCMCIA card 1 and Miniature card data bus direction |
| 26 | PCC0DRV | O | PCMCIA card 0 external address buffer control signal |
| 27 | CE1B# | O | PCMCIA card 0 low byte enable |
| 28 | CE2B# | O | PCMCIA card 0 high byte enable |
| 29 | RDB# | O | PCMCIA card 0 Read enable |
| 30 | WEB# | O | PCMCIA card 0 Write enable |
| 31 | ICIORDB# | O | PCMCIA card 0 I/O Read enable |
| 33 | ICIOWRB# | O | PCMCIA card 0 I/O Write enable |
| 35 | PCC0RESET | O | PCMCIA card 0 reset |
| 37 | PCC0WAIT# | I | PCMCIA card 0 memory or I/O insert wait state |
| 38 | PCC0WP# | I | Reflects the states of the Write Protect switch on PCC0 memory cards. For I/O cards, PCC0WP# is used for the card, which is 16-bit Port (IOIS16# ) function. |

**Table 4-10. Pin Descriptions of PCMCIA Card 0 (cont'd)**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **PCMCIA card 0 (Memory and I/O)** | | | |
| 39 | PCC0RDY | I | Driven low by memory PC cards to indicate that the memory card circuits are busy. For I/O card, PCC0RDY is used as an interrupt request. |
| 40 | PCC0BVD1 | I | The signal indicates the condition of the battery on the PCC0 memory card. Both PCC0BVD1 and PCC0BVD2 are high level when the battery is in good condition. When PCC0BVD1 is low, the PC card battery is no longer serviceable and data are lost. For I/O cards, PCC0BVD1 is used for card status change ( STSCHG ) function. |
| 41 | PCC0BVD2 | I | The signal indicates the condition of the battery on the PCC0 memory card. Both PCC0BVD1 and PCC0BVD2 are high level when the battery is in good condition. When PCC0BVD2 is low while PCC0BVD1 is high level, the PC card battery is in a warning condition. For I/O cards, PCC0BVD2 provides the SPKR function. |
| 42 | PCC0CD1# | I | Provided for the detection of PCMCIA card 0 insertion |
| 43 | PCC0CD2# | I | Provided for the detection of PCMCIA card 0 insertion |
| 44 | PCC0VS1# | I | PCMCIA card 0 Voltage sense |
| 45 | PCC0VS2# | I | PCMCIA card 0 Voltage sense |
| 46 | PCC0A25 | O | PCMCIA card 0 Address 25 |
| 48 | PCC0REG# | O | PCMCIA card 0 attribute memory select |
| 47 | PCC0A24 | O | PCMCIA card 0 Address 25 |
| 51 | VCC0SEL1 | O | PCMCIA card 0 VCC power control |
| 50 | VCC0SEL0 | O | PCMCIA card 0 VCC power control |

**Table 4-11. Pin Descriptions of PCMCIA Card 1**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **PCMCIA 1 (Memory)** | | | |
| 53 | PCC1DRV /PC0 | O/IO | Multifunction Pin: PCMCIA card 1 external address buffer control signal /Port C bit 0 for GPIO |
| 54 | CE1A#/PC1 | O/IO | Multifunction Pin: PCMCIA card 1 low byte enable /Port C bit 1 for GPIO |
| 56 | CE2A#/PC2 | O/IO | Multifunction Pin: PCMCIA card 1 high byte enable /Port C bit 2 for GPIO |
| 57 | RDA#/PC3 | O/IO | Multifunction Pin: PCMCIA card 1 READ enable /Port C bit 3 for GPIO |

**Table 4-11. Pin Descriptions of PCMCIA Card 1 (cont'd)**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 58 | WEA#/PC4 | O/IO | Multifunction Pin: PCMCIA card 1 Write enable /Port C bit 4 for GPIO |
| 59 | PCC1RESET /NC | O/IO | Multifunction Pin: PCMCIA card 1 reset /NC |
| 60 | PCC1WAIT# /PC5 | I/IO | Multifunction Pin: PCMCIA 1 memory or I/O card insert wait state /Port C bit 5 for GPIO |
| 71 | PCC1WP# /PD4 | I/IO | Multifunction Pin: Reflects the states of the Write Protect switch on PCMCIA 1 memory cards /Port D bit 4 for GPIO |
| 72 | PCC1RDY /PD5 | I/IO | Multifunction Pin: Driven low by memory PC cards to indicate that the memory card circuits are busy /Port D bit 5 for GPIO |
| 74 | PCC1BVD1 /PD6 | I/IO | Multifunction Pin: The signal indicates the condition of the battery on the PCMCIA 1 memory card. Both PCC1BVD1 and PCC1BVD2 are in high level when the battery is in good condition. When PCC1BVD1 is low, the PC card battery is no longer serviceable and data are lost. /Port D bit 6 for GPIO |
| 76 | PCC1BVD2 /PD7 | I/IO | Multifunction Pin: The signal indicates the condition of the battery on the PCMCIA 1 memory card. Both PCC1BVD1 and PCC1BVD2 are in high level when the battery is in good condition. When PCC1BVD2 is low while PCC1BVD1 is in high level, the PC card battery is in a warning condition. /Port D bit 7 for GPIO |
| 61 | PCC1CD1# /PC6 | I/IO | Multifunction Pin: Provided for PCMCIA card 1 insertion detection. /Port C bit 6 for GPIO |
| 63 | PCC1CD2# /PC7 | I/IO | Multifunction Pin: Provided for the detection of PCMCIA card 1 insertion. /Port C bit 7 for GPIO |
| 64 | PCC1VS1# /PD0 | I/IO | Multifunction Pin: PCMCIA card 1 Voltage sense / Port D bit 0 for GPIO |
| 65 | PCC1VS2# /PD1 | I/IO | Multifunction Pin: PCMCIA card 1 Voltage sense / Port D bit 1 for GPIO |
| 66 | PCC1A25 /PD2 | O/IO | Multifunction Pin: PCMCIA card 1 Address 25 /Port D bit 2 for GPIO |

**Table 4-11. Pin Descriptions of PCMCIA Card 1 (cont'd)**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 68 | PCC1REG# | O | Multifunction Pin: PCMCIA card 1 attribute memory select. |
| 67 | PCC1A24 /PD3 | O/IO | Multifunction Pin: PCMCIA card 1 Address 24 /Port D bit 3 for GPIO |
| 78 | VCC1SEL1 | O | PCMCIA card 1 VCC power control |
| 77 | VCC1SEL0 | O | PCMCIA card 1 VCC power control |

**Table 4-12. Pin Descriptions of I/O Port**

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| **I/O Port (Multifunction with Miniature)** | | | |
| 69 | PA3/SCL /TMO1# | IO/O/ O | Multifunction Pin: Port A bit 3 for GPIO / Serial Clock Line for $I^2C$ bus interface /Timer 1 output signal for triggering A/D converter. It is enabled by bit 3 ETMO1 in timer 1 control register TCR1 as MODE =00/10. |
| 70 | PA2/SDA /TMO0# | IO/IO /O | Multifunction Pin: Port A bit 2 for GPIO / Serial Data Line for $I^2C$ bus interface / Timer 0 output signal used to trigger A/D converter. It is enabled by bit 3 ETMO0 in timer 0 control register TCR0 as MODE =00/10. |
| 2, 13, 25, 36, 55, 73, 103, 110, 115, 127, 155, 183, 197 | VSS | I | Ground for other I/O cell |
| 32, 49, 86, 106, 117, 153, 185, 207 | VCC | I | 3.3 Volt power for other I/O cell |
| 16, 194, 205 | VCCC | I | 0 / 3.3 / 5V power for address /data buffer of PCC0 or LCDC (1, 3-12, 14, 15, 17-24, 186-193, 195, 196, 198-204, 206, 208) |
| 34 | VCCB | I | 0 / 3.3 / 5V for PCC (27-31, 33, 35, 37-41, 46-48) |
| 62 | VCCA | I | 0 / 3.3 / 5V for PCC (54, 56-60, 66-70) |
| 75 | VCCD | I | 0 / 3.3 / 5V for pins 71, 72, 74 and 76 |
| 169 | AVSS | I | Ground for analog group (170-173) |
| 174 | AVCC | I | Power for analog group (170-173) |

# 5. Color LCD Controller

## 5.1 Overview

The Intelligent Peripheral Controller contains a color LCD controller (LCDC). The LCDC serves to control EDO-DRAM, which acts as the display memory. The LCDC is equipped with an I/F, which can directly drive Color or Monochrome STN-LCDs in the LCD Mode, or CRT monitors in the CRT Mode. Several graphical functions are accelerated by hardware to reduce the workload of the CPU, thereby enhancing the performance.

### 5.1.1 Features

- Color/Monochrome STN-LCD direct interface
- 64, 16, 4, 2 gray scales
- Supports 256/256K and 64K colors
- Supports CRT interface (VESA VGA)
- Supports display resolution of 640x240 (max.) for LCD, and 640x480 for CRT
- Supports CRT and LCD simultaneous display
- Ten (10) types of BitBLT Hardware Acceleration
- Solid-line drawing based upon Bresenham Parameter
- Rectangular solid color fill function
- Supports 256X16 bit EDO-DRAM

### 5.1.2 Display Capabilities

**(1) LCD Mode**

**Table 5-1. LCD Mode**

| No. | Display Type | Display I/F | Colors/Gray Scales | Resolution | Duty |
|---|---|---|---|---|---|
| 1 | Color STN-LCD | 8 bits | 256/256K colors | **Max.**640x240 | 1/240 |
| 2 | Color STN-LCD | 8 bits | 64K colors | **Max.**640x240 | 1/240 |
| 3 | Monochrome STN-LCD | 4/8 bits | 64 gray scales | **Max.**640x240 | 1/240 |
| 4 | Monochrome STN-LCD | 4/8 bits | 16 gray scales | **Max.**640x240 | 1/240 |
| 5 | Monochrome STN-LCD | 4/8 bits | 4 gray scales | **Max.**640x240 | 1/240 |
| 6 | Monochrome STN-LCD | 4/8 bits | 2 gray scales | **Max.**640x240 | 1/240 |

Note: LCD Mode only supports Single -Panel and Single Drive STN-LCD.

Mode one (1): A total of 256 combinations out of 256K colors can be displayed simultaneously. The combinations are defined by the palette registers. In Mode one (1), therefore, palette registers must be properly programmed before the display function is initiated. In this mode, 8-bits/pixel data is used to define the address of each palette register.

Mode two (2): A total of 64K colors can be displayed simultaneously. In this mode, one (1) pixel data, which consists of 16 bits. are used to display colors. The 16-bits/pixel data is comprised of five (5) bits for Red, six (6) for Green and five (5) for Blue.

Modes 3, 4, 5, 6: In Modes 3, 4, 5, 6, LCDC displays monochrome data. In Mode three (3), 6-bits/pixel data are used to describe the gray scales, 4-bit/pixel data for Mode 4, 2-bit/pixel for Mode 5, and 1bit/pixel data for Mode 6.

**(2) CRT Mode**

**Table 5-2. CRT Mode**

| No. | Display Type | Display I/F | Colors/Gray Scales | Resolution | Duty |
|---|---|---|---|---|---|
| 1 | VESA VGA | Analog R, G, B | 256/256K colors | 640x480 | 72Hz |

**(3) Simultaneous Mode**

This mode is capable of simultaneously displaying both CRT and LCD. CRT Mode is VESA VGA with 256 color combinations and the resolution is 640x480. LCD Mode is color STN-LCD with 256 color combinations, and the resolution is 640x240.

### 5.1.3 Hardware Acceleration

**(1) BitBLT Function**

This device supports screen-to-screen bit block transfer function with nine (9) ternary raster-operations and one (1) quaternary raster-operation required by Windows CE™ API. The table below defines the supported raster operations.

**Table 5-3. Definition of Supported Raster-Operation**

| No. | Value | Code | Meaning | Operation |
|---|---|---|---|---|
| 1 | SRCAND | 88h | Combine the source and destination bits using the bitwise AND operator. | Ternary |
| 2 | SRCCOPY | CCh | Copy source bits to the destination rectangle. | Ternary |
| 3 | SRCINVERT | 66h | Combine the source and destination bits using the bitwise exclusive OR operator. | Ternary |
| 4 | SRCPAINT | EEh | Combine the source and destination bits using the bitwise OR operator. | Ternary |
| 5 | PATCOPY | F0h | Copy the brush bits to the destination rectangle. | Ternary |
| 6 | PATINVERT | 5Ah | Combine the pattern and destination bits using the bitwise exclusive OR operator. | Ternary |
| 7 | DSTINVERT | 55h | Copy the inverse of the destination bits. | Ternary |
| 8 | BLACKNESS | 00h | Set all destination bits to black. | Ternary |
| 9 | WHITENESS | FFh | Set all destination bits to white. | Ternary |
| 10 | MASKED SRCCOPY | CCAAh | Copy source bits to the destination rectangle, depending on the data of mask bits. | Quaternary |

The table below shows how the destination dots are changed by each operation.

**Table 5-4. Results of BitBLT Raster-Operation**

| | OPERATION | OPERANDS | | DESTINATION |
|---|---|---|---|---|
| 1 | SRCAND | (SRC) | (DST) | (DST) |
| 2 | SRCCOPY | (SRC) | | (DST) |
| 3 | SRCINVERT | (SRC) | (DST) | (DST) |
| 4 | SRCPAINT | (SRC) | (DST) | (DST) |
| 5 | PATCOPY | (PAT) | | (DST) |
| 6 | PATINVERT | (PAT) | (DST) | (DST) |
| 7 | DSTINVERT | | (DST) | (DST) |
| 8 | BLACKNESS | | | (DST) |
| 9 | WHITENESS | | | (DST) |
| 10 | MASKEDDSTCPY | (SRC) | (MASK) | (DST) |

*SRC – Source Block. DST – Destination Block. PAT – Pattern Block. MASK – Mask Block.

**Note**: 1) **BitBLT functions are available only in LCD Mode one (1) and Mode two (2).**
2) PAT Block size must be 8x8 dots.
3) MASK Block and SRC Block's width and height are the same as that of DST Block.
4) MASK Block data is 1 bit/pixel (1: MASK, 0: Through) and must be word (16 bits) aligned.

Refer to BitBLT Registers Section for more details.

**(2) Solid Line drawing based upon Bresenham Parameter**

**(3) Rectangular Solid Color Fills**

### 5.1.4 System BUS I/F

#### (1) SRAM I/F

LCDC's registers are allocated in lower 32Mbyte on Area 4 of SH7709. Display memory is allocated in upper 32 Mbyte of Area 4 of SH7709. In order to control the LCDC, the CPU accesses the LCDC registers and display memory via SRAM I/F since SRAM I/F is located in Area 4's memory space.

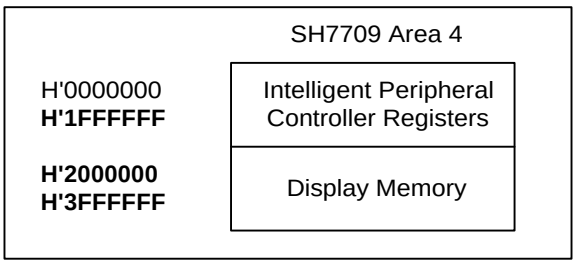



**Figure 5-1. LCDC Register & Display Memory Allocation**

#### (2) Wait Signal

The Intelligent Peripheral Controller issues a wait signal to inform the CPU that LCDC is in a busy state when the CPU requires READ/WRITE access during some process. LCDC enters into a busy state when the following two conditions occur:

(1) When it needs to perform more than 32 cycles while reading the display data.
(2) When the acceleration function is in action, and the duration of the busy state is determined by the number of cycles that the acceleration commands need to perform.

#### (3) Acceleration Flag

The device provides a flag bit to indicate that the acceleration function is in action. This flag bit is located in the common registers of the accelerator. As shown in the flow chart below, the flag bit value must be 0 to enter the idle state before the CPU can access the Display Memory.

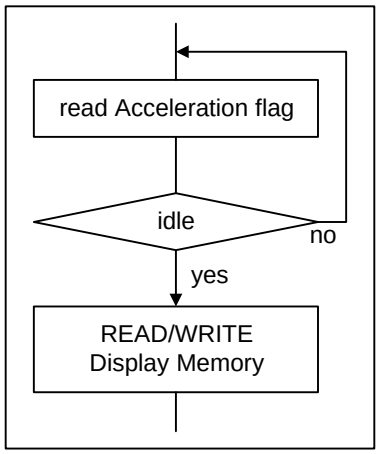



**Figure 5-2. Flow Chart for CPU Access Display Memory**

### 5.1.5 Display Memory I/F

**(1) DRAM I/F**

EDO-DRAM supports
4Mbits (512Kbytes) 256Kx16bits speed version 60 ns.

**(2) DRAM Refresh**

CAS-before-RAS refresh
Self refresh

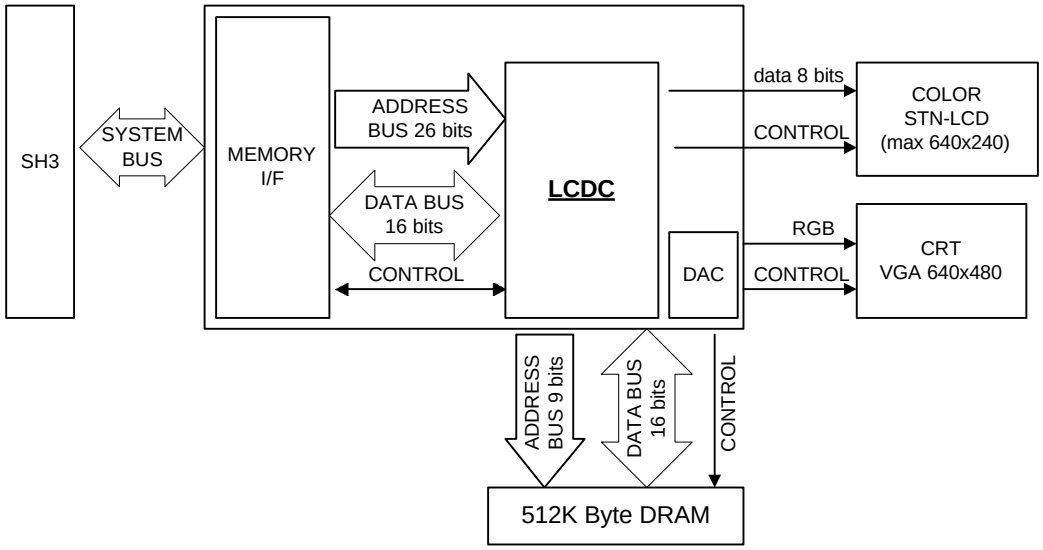



**Figure 5-3. LCD System Block Diagram**

## 5.2 LCD Controller Control Register

### 5.2.1 Base Address Register

LCDCBAR, a 16-bit register, provides the display area start address bit [25:12] of the display memory, indicating the display start address step is 4K Byte.

**Address: 10001000h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD[13:0] | BAD [13:0] | BAD [13:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD [13:0] | BAD [13:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 13 | Reserved | 0000hex |
| 12 ~ 0 | Display area start address bit [25:12] | |

### 5.2.2 Line Address Offset Register

LCDCLOR, a 16-bit register, provides the line increment address.

**Address: 10001002h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | LO [10:0] | LO [10:0] | LO [10:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LO [10:0] | LO [10:0] | LO [10:0] | LO [10:0] | LO [10:0] | LO [10:0] | LO [10:0] | LO [10:0] |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 11 | Reserved | 0280hex |
| 10 ~ 0 | Line increment address | |

### 5.2.3 LCDC Control Register

LCDCCR, a 16-bit register, is used to control the LCD Controller. All the bits on this register are initialized to define the initial value at RESET.

**Address: 10001004h**

| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | STBACK | Reserved | STREQ |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 |
| **R/W** | - | - | - | - | - | **R** | R | R/W |

| **Bit** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | **MOFF** | REFSEL | EPON | SPON | Reserved | DSPSEL [2:0] | DSPSEL [2:0] | DSPSEL [2:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **R/W** | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |

| **Bit** | **Description** | **Default** |
|---|---|---|
| 15 ~ 11 | - | 0001hex |
| 10 | STBACK (Standby Back), this bit indicates the LCDC is in the STANDBY state or in the default state.<br>1:Indicates STANDBY state. The VRAM access from the CPU is forbidden.<br>0: Indicates default state | |
| 9 | Reserved | |
| 8 | STREQ (Standby Request), when this bit is set to 1, LCDC begins the standby sequence. When this bit is set to 0, LCDC begins the standby back sequence when this bit is set to 0.<br>1: Requires STANDBY state<br>0: Requires default state | |
| 7 | **MOFF (Memory Off), when this bit is set to 1, write enable signal for frame memory (FWE#) is forced to Low level. This bit is used to save power consumption when power supply to frame Memory is shut down at standby mode. Other pins (FA, FD, FRAS#, FLCAS#, FHCAS#, FRD#) are forced to low level at standby mode automatically.**<br>**0: Default**<br>**1: Force FWE# signal to low level** | |
| 6 | REFSEL (Refresh Select), when this bit is set to 0, LCDC will self-refresh the display memory at standby sequence.<br>1: Selfrefresh off<br>0: Selfrefresh on | |

**LCDC Control Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 5 | EPON (End Power On), this bit shows that LCDC has completed the power- on sequence.<br>1: End Power-on sequence<br>0: Default | |
| 4 | SPON (Start Power On), when this bit is set to 1, LCDC initiates the power-on sequence.<br>1: Start Power-on sequence<br>0: Default | |
| 3 | Reserved | |
| 2 ~ 0 | ESPSEL [2:0] (Display select)<br>100: LCD & CRT on<br>010: CRT on<br>001: LCD on | |

**Examples of the LCDC Register Settings:**

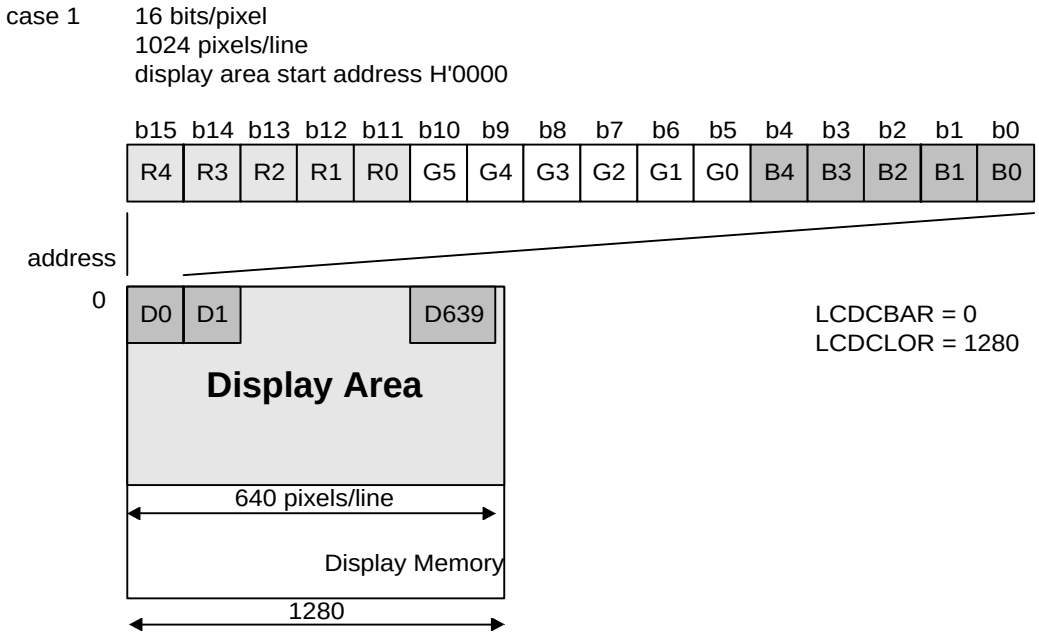



**Figure 5-4. 64K Colors Example**

case 2 8 bits/pixel
1024 pixels/line
display area start address H'0000

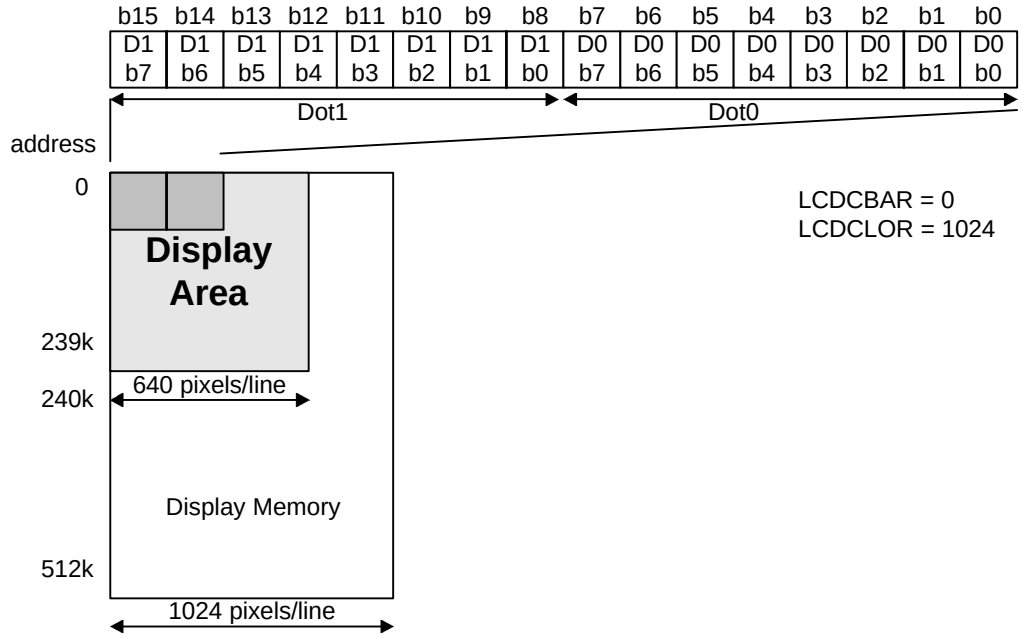



**Figure 5-5. 256/256K Colors Example**

case 3 6 bits/pixel
1024 pixels/line
display area start address H'0000

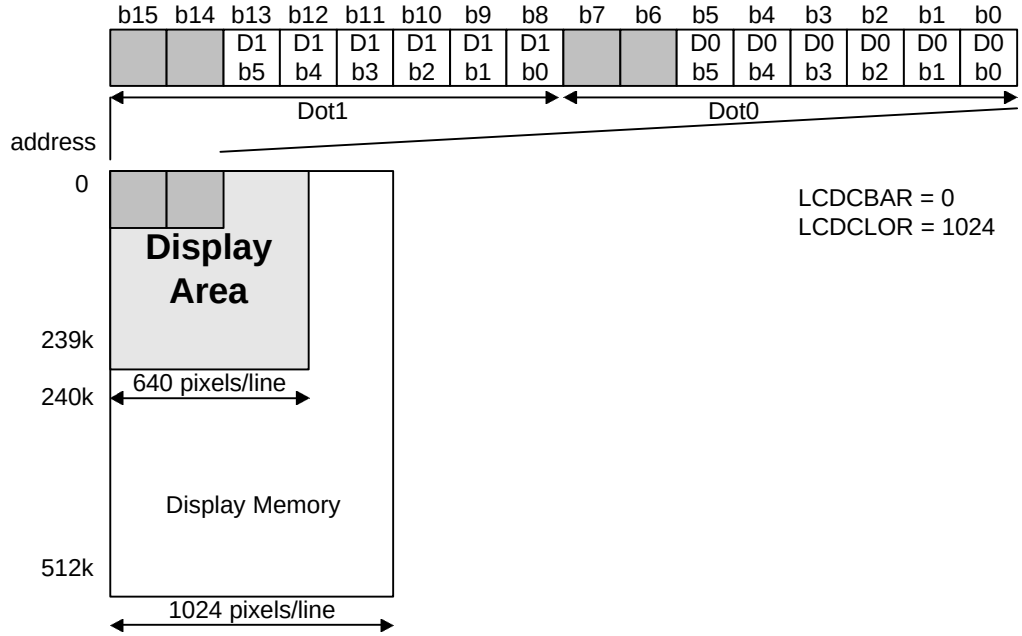



**Figure 5-6. 64 Gray Scales Example**

case 4 4 bits/pixel
1024 pixels/line
display area start address H'0000

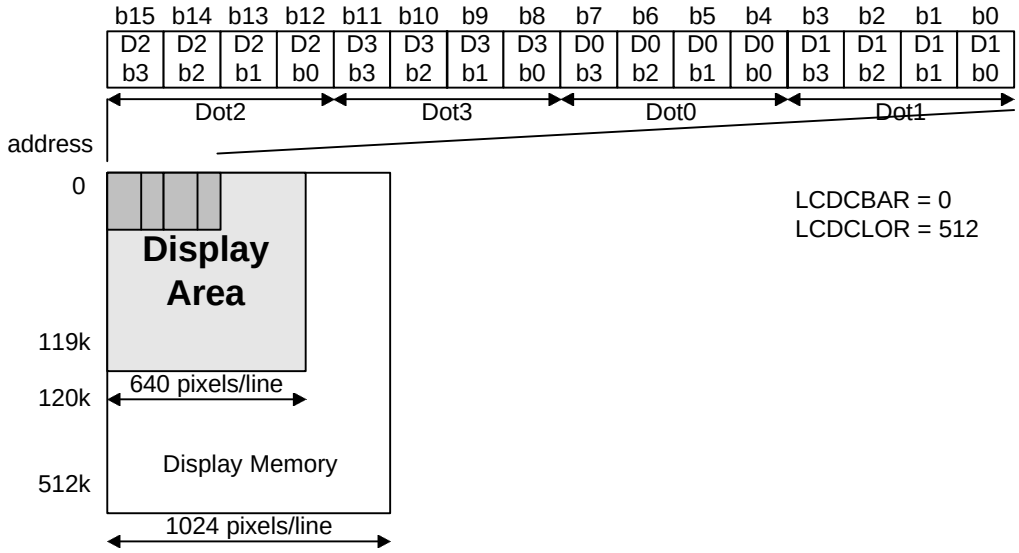



**Figure 5-7. 16 Gray Scales Example**

case 5 2 bits/pixel
1024 pixels/line
display area start address H'0000

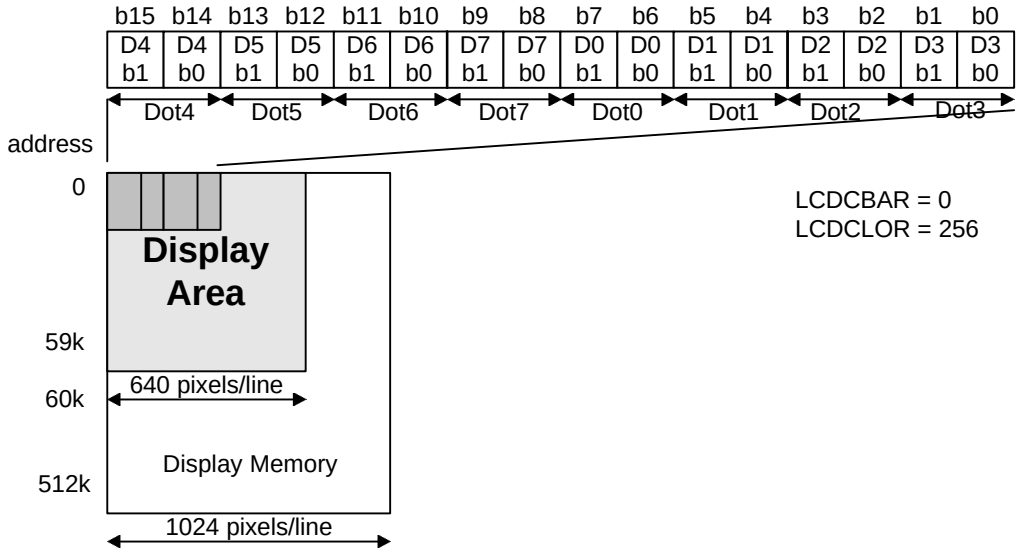



**Figure 5-8. 4 Gray Scales Example**

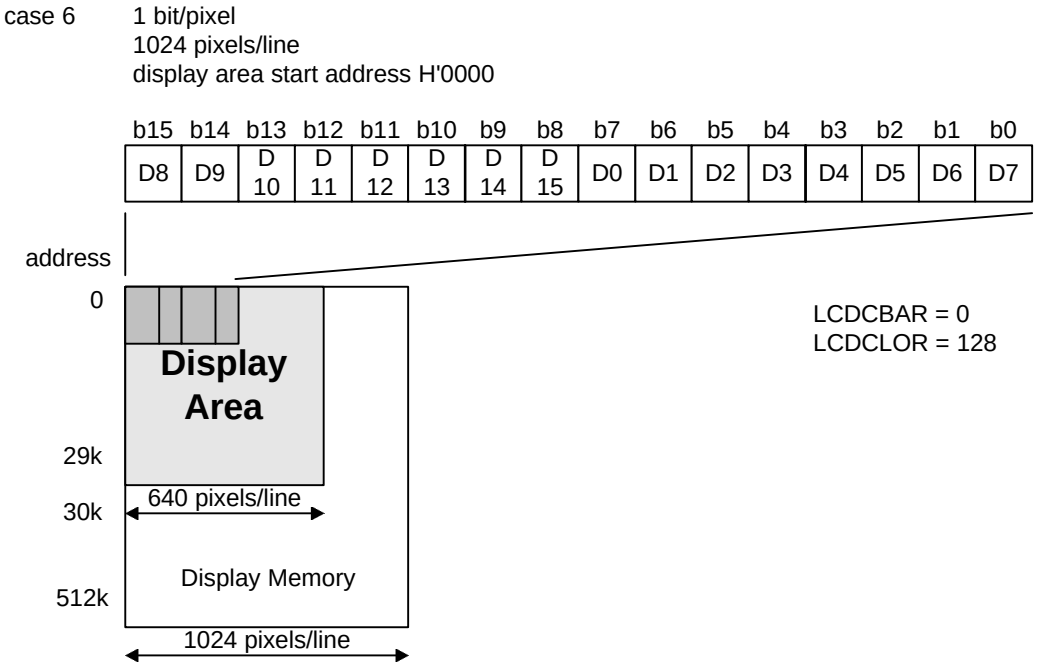



**Figure 5-9. 2 Gray Scales Example**

The diagram below shows the way to access the LCDCCR register:

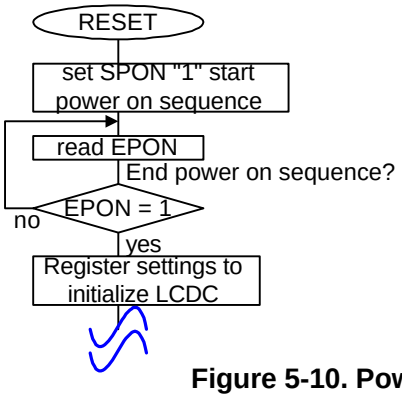



**Figure 5-10. Power-On RESET Sequence**

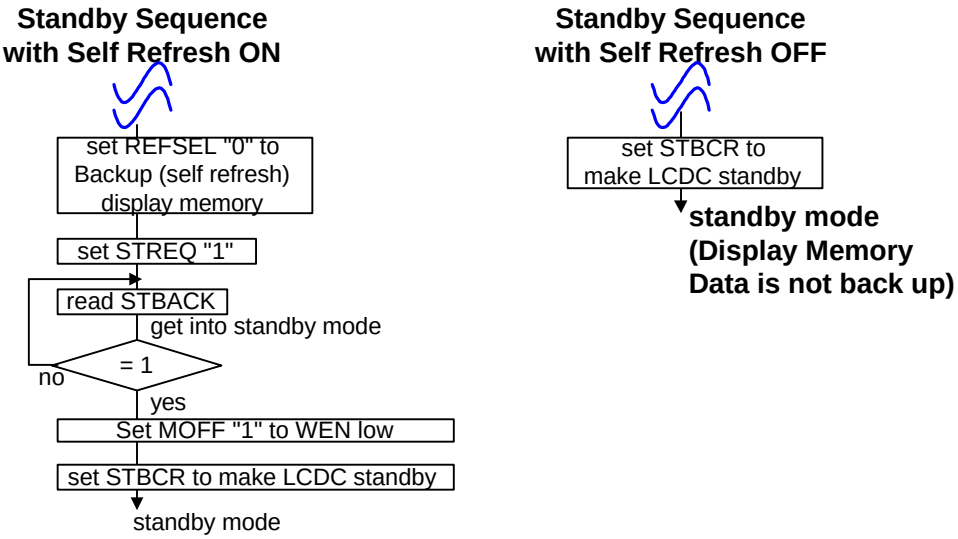



**Figure 5-11. Standby Sequence**

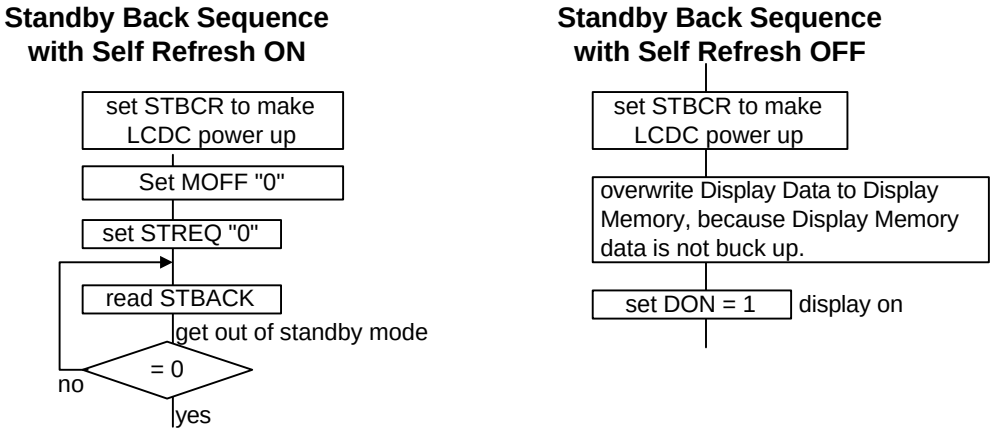



**Figure 5-12. Standby Back Sequence**

### 5.3 LCD Register

#### 5.3.1 LCD Display Register

LDR1, a 16-bit register, is used to control the LCD.

**Address: 10001010h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | - | **DINV** |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | - | - | **R/W** |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | - | DON |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **R/W** | - | - | - | - | - | - | - | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 9 | Reserved | 0000hex |
| 8 | **DINV (Display Invert), when this bit is set to 1, monochrome LCD display data is inverted in gray scale.** | |
| 7 ~ 1 | Reserved | |
| 0 | DON (Display On), controls the output pin DON<br>1: LCD on<br>0: LCD off | |

#### 5.3.2 LCD Display Register 2

LDR2, a 16-bit register, is used to control the LCD.

**Address: 10001012h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | Reserved | Reserved | Reserved |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | CC1 | CC2 | Reserved | Reserved | Reserved | LM [2:0] | LM [2:0] | LM [2:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**LCD Display Register 2 (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Reserved | 0002hex |
| 7 | CC1 (Clock Control 1), controls CL1<br>**1: No output at retrace period**<br>0: Vertical retrace period CL1 output | |
| 6 | CC2 (Clock Control 2), controls CL2<br>**1: No output at retrace period**<br>0: Retrace period CL2 output | |
| 5 ~ 3 | Reserved | |
| 2 ~ 0 | LM[2:0] (LCD Module), set LCD display data output interface<br>110: Reserved<br>101: Reserved<br>100: Color, one screen, and output of R, G, B bits<br>011: Reserved<br>010: Reserved<br>001: Monochrome, one screen, 8-bit output/multi-fraction, 8-bit output.<br>000: Monochrome, one screen, 4-bit output/multi-fraction, 4-bit output. | |

### 5.3.3 LCD Number of Characters in Horizontal Register

LDNCHR, a 16-bit register, is used to define the number of horizontal character.

**Address: 10001014h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | NHD[7:0] | NHD[7:0] | NHD[7:0] | NHD[7:0] | NHD[7:0] | NHD[7:0] | NHD[7:0] | NHD[7:0] |
| **Initial Value** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | NHT[7:0] | NHT[7:0] | NHT[7:0] | NHT[7:0] | NHT[7:0] | NHT[7:0] | NHT[7:0] | NHT[7:0] |
| **Initial Value** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**LCD Number of Characters in Horizontal Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | NHD (Number of Horizontal Display Character), set the number of horizontal display characters. The number of horizontal display characters is calculated as follows:<br>(Number of pixel) / 8 - 1 | 9f9fhex |
| 7 ~ 0 | NHT (Number of Horizontal Total Character), set the total number of horizontal characters. The number of horizontal total characters is calculated in the same way as NHD. | |

### 5.3.4 Start Position of Horizontal Register

LDHNSR, a 16-bit register, serves to specify the output start position and the width of CL1 clock.

**Address: 10001016h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | HSW [3:0] | HSW [3:0] | HSW [3:0] | HSW [3:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| **R/W** | - | - | - | - | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | HSP[7:0] | HSP[7:0] | HSP[7:0] | HSP[7:0] | HSP[7:0] | HSP[7:0] | HSP[7:0] | HSP[7:0] |
| **Initial Value** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 12 | - | 0A80hex |
| 11 ~ 8 | HSW (Horizontal Synchronous Width), set CL1 width via the number of characters. | |
| 7 ~ 0 | HSP (Horizontal Synchronous Position), set CL1 output position via the number of characters. | |

### 5.3.5 Total Vertical Lines Register

LDVNTR, a 16-bit register, is used to specify the total vertical lines.

**Address: 10001018h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | VTL [9:0] | VTL [9:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | VTL[9:0] | VTL[9:0] | VTL[9:0] | VTL[9:0] | VTL[9:0] | VTL[9:0] | VTL[9:0] | VTL[9:0] |
| **Initial Value** | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 10 | - | 00EFhex |
| 9 ~ 0 | VTL (Vertical Total Lines), set **(total number of vertical lines) - 1.** | |

### 5.3.6 Display Vertical Lines Register

LDVNDR, a 16-bit register, serves to specify the number of display vertical lines.

**Address: 1000101Ah**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | VDL [9:0] | VDL [9:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | VDL [9:0] | VDL [9:0] | VDL [9:0] | VDL[9:0] | VDL [9:0] | VDL [9:0] | VDL [9:0] | VDL [9:0] |
| **Initial value :** | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Display Vertical Lines Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 15 ~ 10 | - | 00EFhex |
| 9 ~ 0 | VDL (Display Vertical Lines), set **(total number of display vertical lines) - 1.** | |

### 5.3.7 Vertical Synchronization Position Register

LDVSPR, a 16-bit register, is used to specify the vertical synchronization position and AC number.

**Address: 1000101Ch**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | AC[4:0] | AC[4:0] | AC[4:0] | AC[4:0] | AC[4:0] | Reserved | VSP [9:0] | VSP [9:0] |
| **Initial Value** | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | VSP[9:0] | VSP[9:0] | VSP[9:0] | VSP[9:0] | VSP[9:0] | VSP[9:0] | VSP[9:0] | VSP[9:0] |
| **Initial Value** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 11 | AC (Numbers of AC lines), these bits control the output pin M, and set **(the number of AC lines) -1.** | 68F0hex |
| 10 | Reserved | |
| 9 ~ 0 | VSP (Vertical Synchronization Position), set the **(number of vertical synchronization position) -1.** | |

### 5.3.8 LCD Display Register 3

LDR3, a 16-bit register, is used to control LCD.

**Address: 1000101Eh**

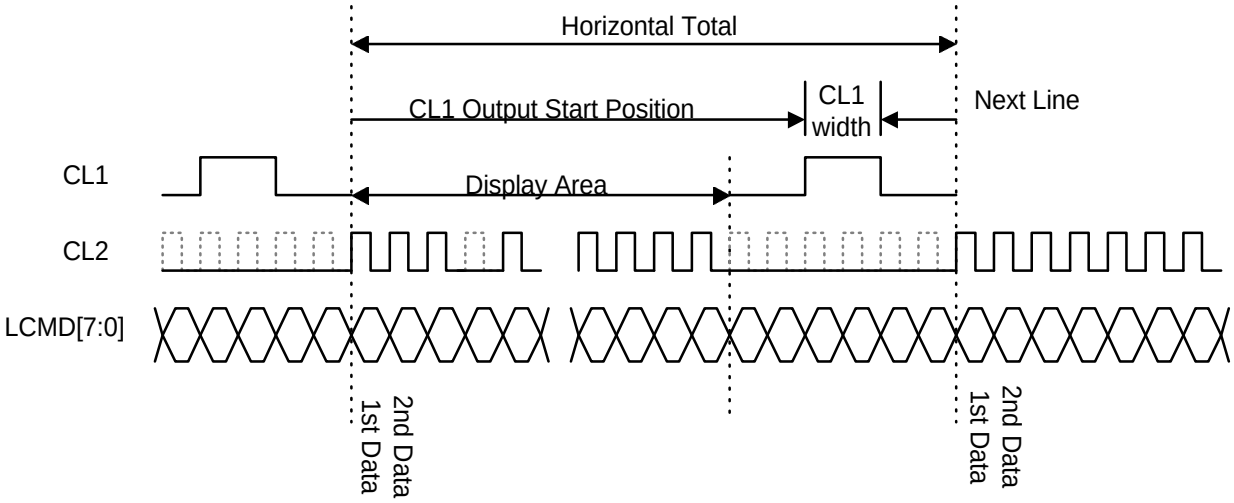
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | CS [4:0] | CS [4:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

**LCD Display Register 3 (cont'd)**

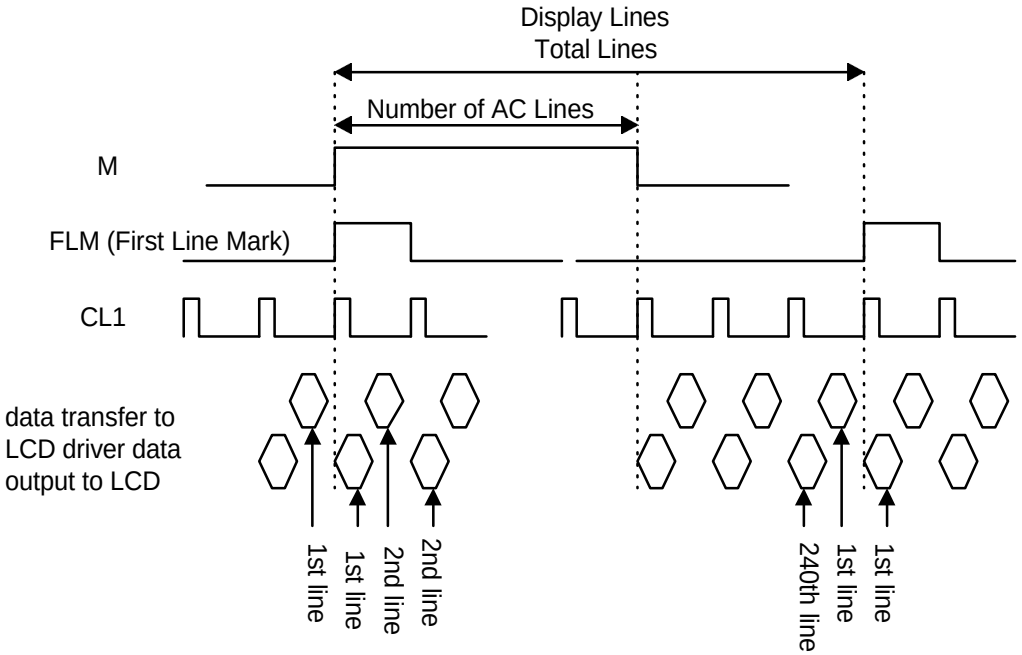
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | CS[4:0] | CS[4:0] | CS[4:0] | Reserved | CG[3:0] | CG[3:0] | CG[3:0] | CG[3:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 10 | - | 0004hex |
| 9 ~ 5 | CS (Clock Select), select CL2 frequency<br>**For color** 10000: 10 MHz **For monochrome 10000: 10/2 MHz**<br>01000: 7.5 MHz **01000: 7.5/2 MHz**<br>00100: 5MHz **00100: 5/2 MHz**<br>00010: 3.75 MHz **00010: 3.75/2 MHz**<br>00001: 2.5 MHz **00001: 2.5/2 MHz**<br>00000: 15MHz **00000: 15/2 MHz** | |
| 4 | Reserved | |
| 3 ~ 0 | CG (Color/Gray scale) select LCD mode<br>1000: Color, 8 bits RGB: 5-6-5 bits/64K colors<br>0100: Color, 8 bits 256 colors<br>0011: Monochrome, 6-bit 64 gray scales<br>0010: Monochrome, 4-bit 16 gray scales<br>0001: Monochrome, 2-bit 4 gray scales<br>0000: Monochrome, 1-bit 2 gray scales | |

## LCD Registers and Output Timings




Horizontal Total is controlled by NHT in LDHNCR.
Display Area is controlled by NHD in LDHNCR.
CL1 Output Start Position is controlled by HSP in LDHNSR.
CL1 width is controlled by HSW in LDHNSR.

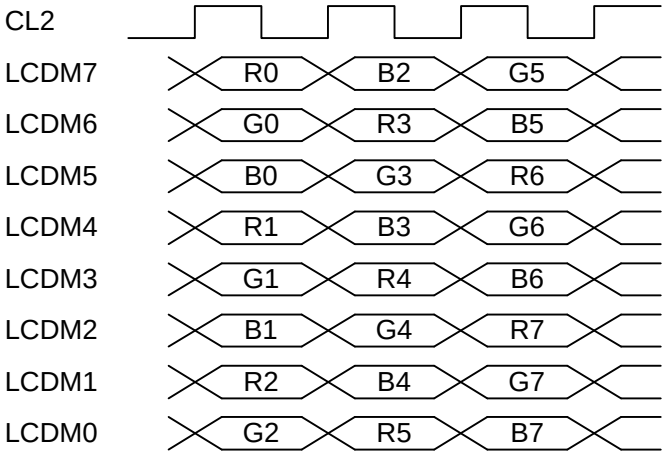



Display Lines are controlled by LDVNDR.
Total Lines are controlled by LDVNTR.
The number of AC Lines is controlled by AC in LDVSPR
The rising edge of FLM is controlled by VSP in LDVSPR.

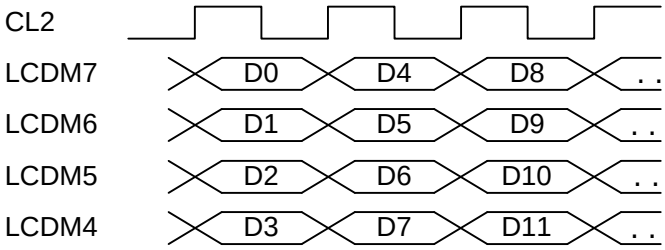
**Figure 5-13. LCD Output Timings**

## LCDM Output Format

**For color 8bit bus width mode**

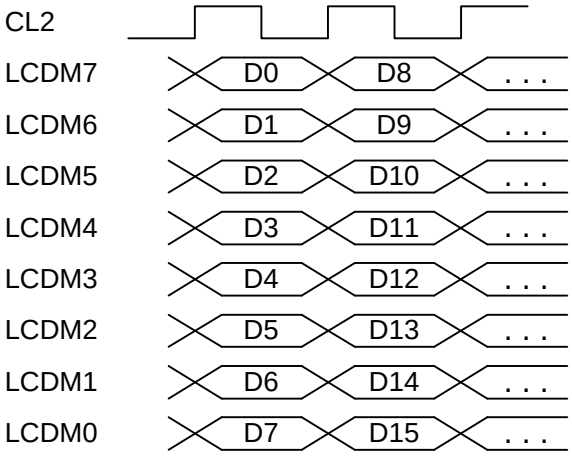



**For monochrome 4bit bus width mode**




LCDM[3:0] unknow

**For monochrome 8bit bus width mode**




Ri: Red for i_th dot Gi: Green for i_th dot
Bi: Blue for i_th dot Di: On/Off for i_th dot

**Figure 5-14. LCDM Output Format**

## 5.4 CRT Control Register

### 5.4.1 CRTC Total Vertical Lines Register

CRTVTL is a 16-bit register, and is used to specify total vertical lines for CRT.

**Address: 10001020h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | CRTVTL [9:0] | CRTVTL [9:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] | CRTVTL [9:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 10 | Reserved | 020Bhex |
| 9 ~ 0 | CRTVTL, set total number of vertical lines for CRT. | |

### 5.4.2 CRTC Vertical Retrace Start Register

CRTVRS is a 16-bit register used to set vertical retrace start line for CRT.

**Address: 10001022h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | CRTVRS [9:0] | CRTVRS [9:0] |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

**CRTC Vertical Retrace Start Register (cont'd)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] | CRTVRS [9:0] |
| Initial Value | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 10 | Reserved | 01EAhex |
| 9 ~ 0 | CRTVRS, set vertical retrace start line. | |

### 5.4.3 CRTC Vertical Retrace End Register

CRTVRE is a 16-bit register, and is used to set vertical retrace end line.

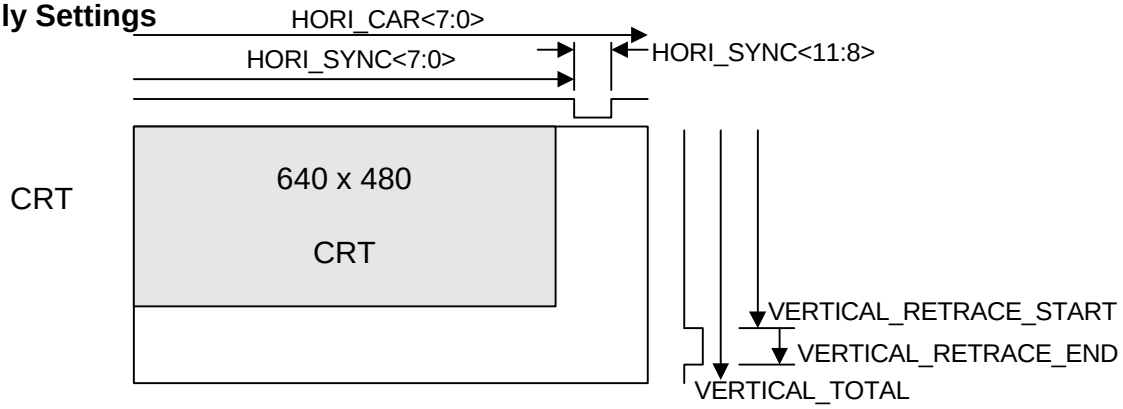
**Address: 10001024h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | CRTVRE [3:0] | CRTVRE [3:0] | CRTVRE [3:0] | CRTVRE [3:0] |
| Initial Value | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

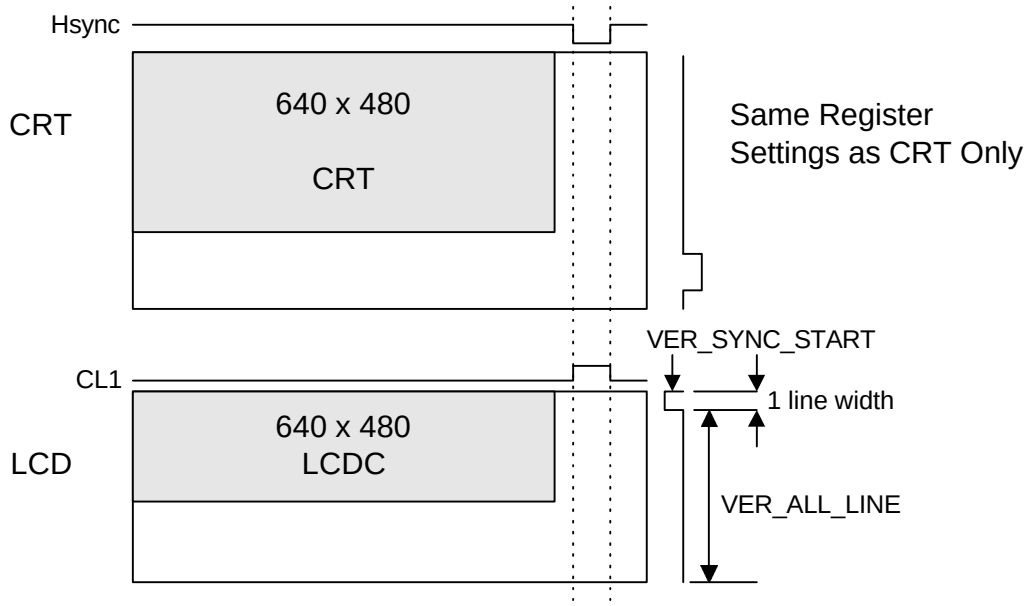
| Bit | Description | Default |
|---|---|---|
| 15 ~ 4 | Reserved | 008Chex |
| 3 ~ 0 | CRTVRE, set vertical retrace end line. | |

**CRT Only Settings**




1) Default VERTICAL_*is set based on VESA standard

**CRT &LCD Register Settings**




1) Set VER_ALL_LINE, VER_SYNC_START as [(total CRT lines)/2

2) Hsync and CL1 must be same setting as above

3) LCD panel displays only even lines on the CRT at this mode.

**Figure 5-15. CRT Output Timing**

### 5.5 Palette Register

#### (1) Color Palette Write Address Register

**CPTWAR**
**Address: 10001030h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | WRITE_PALETTE_NUM[7:0] | | | | | | | |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | W | W | W | W | W | W | W | W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Set up the write palette number. Automatically incremented after the write access to WRITE_PALETTE_D[5:0] is performed for the third time. | 0000hex |
| 7 ~ 0 | - | |

**(2) Color Palette Write Data Register**

**CPTWDR**
**Address: 10001032h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | WRITE_PALETTE_D[5:0] | | | | | |
| Initial Value | - | - | - | - | - | - | - | |
| R/W | - | - | W | W | W | W | W | W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 6 | - | 0000hex |
| 5 ~ 0 | Write data register<br>1st access: Red data<br>2nd access: Green data<br>3rd access: Blue data | |

**(3) Color Palette READ Address Register**

**CPTRAR**
**Address: 10001034h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | READ_PALETTE_NUM[7:0] | | | | | | | |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | W | W | W | W | W | W | W | W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - |

**(3) Color Palette READ Address Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Set up READ palette number. Automatically incremented after the 3rd time READ access to READ_PALETTE_D[7:0]. | XXXXhex |
| 7 ~ 0 | - | |

**(4) Color Palette READ Data Register**

**CPTRDR**
**Address: 10001036h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | - | - |
| **Initial Value** | - | - | - | - | - | - | - | - |
| **R/W** | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | READ_PALETTE_D[5:0] | | | | | |
| **Initial Value** | - | - | - | - | - | - | - | |
| **R/W** | - | - | R | R | R | R | R | R |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 6 | - | XXXXhex |
| 5 ~ 0 | READ data register<br>1st access: Red data<br>2nd access: Green data<br>3rd access: Blue data | |

WRITE Sequence:
1) Write the number of color palette to CPTWAR.
2) Write Red Data to **CPTWDR**.
3) Write Green Data to **CPTWDR**.
4) Write Blue Data to **CPTWDR**.
5) Continue to write R, G, B to **CPTWDR**, and the Data are then written to the next palette.

READ Sequence:
1) Write the number of color palette to CPTRAR.
2) Read **CPTRDR** as Red Data.
3) Read **CPTRDR** as Green Data.
4) Read **CPTRDR** as Blue Data.
5) Continue to read, and the next palette data is then read.


**Figure 5-16. Palette Register**

### 5.6 Acceleration Common Registers

#### (1) Display Resolution Offset Register

**DSPOFFSET**
**Address: 10001040h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | DSPOFFSET [10:0] | | |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | DSPOFFSET [10:0] | | | | | | | |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 11 | - | 027Fhex |
| 10 ~ 0 | Set X coordinate width of display resolution -1. | |

**(2) Solid Color Register**

**SOLIDCOLOR**
**Address: 10001042h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | | | | SOLIDCOLOR [15:0] | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SOLIDCOLOR [15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | Set color data for solid color fill operation. For 8BPP mode, only lower byte is valid. | 0000hex |

**(3) Accelerator Configuration Register**

**ACC_CONFIG**
**Address: 10001044h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | ACCSTATUS | ACCRESET | ACCSTART | | COLORDEPH |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R/W | - | - | - | R/W | R/W | R/W | R/W | R/W |

**(3) Accelerator Configuration Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 4 | ACCSTATUS (READ only). Read this bit as accelerator status. If this bit indicates that the accelerator is in action, it then avoids to access display memory or to issue the ACCELERATION command.<br>1: Active<br>0: Idle | 0001hex |
| 3 | ACCRESET. When this bit is set to 1, SOFTWARE RESET for accelerator is asserted.<br>1: RESET<br>0: Default | |
| 2 ~ 1 | ACCSTART. When these bits are written, the accelerator is initiated.<br>11: BitBLT<br>10: Line drawing<br>01: Reserved<br>00: Acceleration off | |
| 0 | COLORDEPH. Sets sixteen (16) bits/pixel or eight (8) bits/pixel for the accelerator<br>1: 8BPP<br>0: 16BPP | |

## 5.7 Line Drawing Registers

**(1) Line Start Address Register (H)**

**LINE_START (H)**
**Address: 100001046h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | LINE_START [18:16] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 2 ~ 0 | LINE START[18:16]. | 0000hex |

**(2) Line Start Address Register (L)**

**LINE_START (L)**
**Address: 10001048h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LINE _START 5:0]<br>[1 | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LINE _START 5:0]<br>[1 | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | LINE_START[15:0], set VRAM address, which corresponds to the start coordinates of line to be drawn. | 0000hex |

**(3) Axis Pixel Length Register**

**AXIS_LEN**
**Address: 1000104Ah**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | AXIS_LEN[10:0] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | AXIS_LEN[10:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 10 ~ 0 | AXIS_LEN[10:0], set the value of MAX (\|DX\|, \|DY\|) | 0000hex |

**(4) Diagonal Register**

**DIAGONAL**
**Address: 1000104Ch**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DIAGONAL15 | - | - | - | - | DIAGONAL[10:0] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DIAGONAL[10:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 | Sign bit | 0000hex |
| 10 ~ 0 | Set the value 2 * [ min(\|DX\|, \|DY\|) - max(\|DX\|, \|DY\|) ] | |

**(5) Axial Register**

**AXIAL**
**Address: 1000104Eh**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | AXIAL[11:0] | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | AXIAL[11:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 11 ~ 0 | Set the value 2 * min(\|DX\|, \|DY\|) | 0000hex |

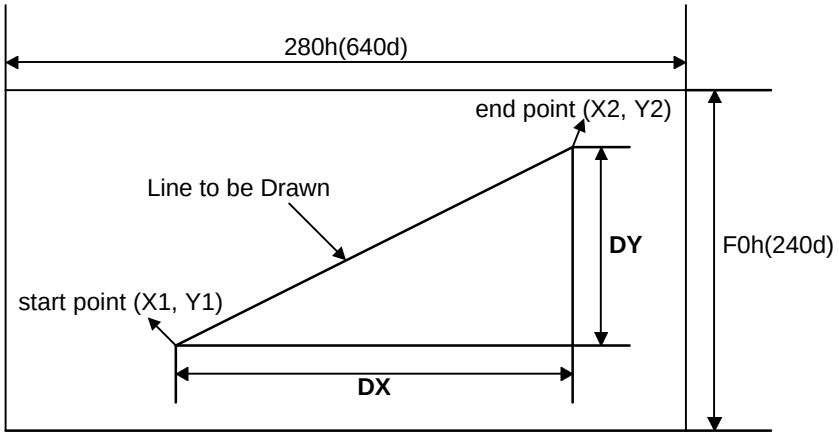
**(6) Start Error Term Register**

**ERROR_TERM**
**Address: 10001050h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ERROR_TERM15 | - | - | - | - | ERROR_TERM[10:0] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ERROR_TERM [10:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 | Sign bit | 0000hex |
| 11 ~ 0 | Set the value 2 * min(\|DX\|, \|DY\|) - max(\|DX\|, \|DY\|). | 0000hex |




640*240dots 256 colors (DX>DY)

(1) LINOFFSET = 280h
(2) START_ADDRESS = LIONFFSET * Y1 + X1
(3) AXIS_LEN = DX
(4) DIAGONAL = 2 (DY - DX)
(5) AXIAL = 2 * DY
(6) ERROR_TERM = 2 * DY - DX

**Figure 5-17. Line Drawing Function**

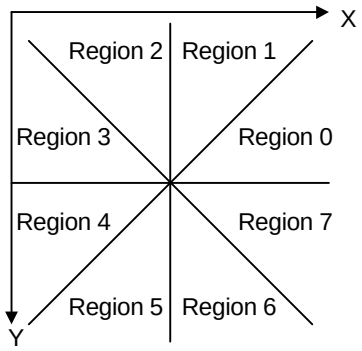
**(7) Line Mode Register**

**LINE_DRAW_MODE**
**Address: 10001052h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | LINE_DRAW _MODE[1:0] | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 1 ~ 0 | DRAWAREA, set the region for lines to be drawn<br>11: Region 1 or 5<br>10: Region 2 or 6<br>01: Region 0 or 4<br>00: Region 3 or 7 | 0000hex |




| Region | Value |
|---|---|
| 1 or 5 | 11 |
| 2 or 6 | 10 |
| 0 or 4 | 01 |
| 3 or 7 | 00 |

**Figure 5-18. Line Drawing Region**

### 5.8 BitBLT Registers

#### (1) Source Start Address Register (H)

**SRCSTART (H)**
**Address: 10001054h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | SRCSTART [18:16] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 2 ~ 0 | SRCSTART[18:16] | 0000hex |

#### (2) Source Start Address Register (L)

**SRCSTART (L)**
**Address: 10001056h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SRCSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SRCSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | SRCSTART[15:0], set VRAM address which corresponds to the upper left corner coordinates of the source block. | 0000hex |

**(3) Destination Start Address Register (H)**

**DSTSTART**
**Address: 10001058h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | DSTSTART [18:16] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 2 ~ 0 | DSTSTART[18:16]. | 0000hex |

**(4) Destination Start Address Register (L)**

**DSTSTART**
**Address: 1000105Ah**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DSTSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DSTSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | DSTSTART[15:0], set VRAM address which corresponds to the upper left corner coordinates of the destination block. | 0000hex |

**(5) Destination Block Width Register**

**DSTWIDTH**
**Address: 1000105Ch**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | DSTWIDTH[10:0] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DSTWIDTH[10:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 10 ~ 0 | DSTWIDTH[10:0], set X coordinate width of the destination block. | 0000hex |

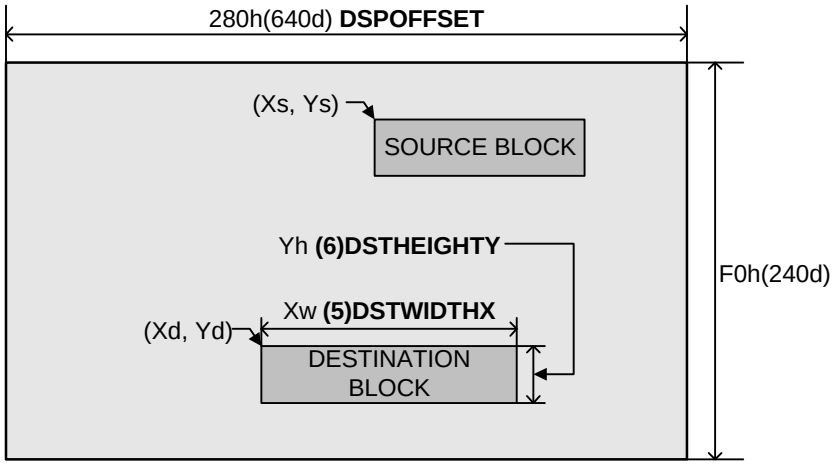
**(6) Destination Block Height Register**

**DSTHEIGHT**
**Address: 1000105Eh**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | DSTHEIGHT [10:0] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | DST HEIGHT [10:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 10 ~ 0 | DSTWIDTH[10:0], set Y coordinate height of the destination block. | 0000hex |




**(1)(2)SRCSTART** = (DSPOFFSET) * Ys + Xs AD: SRCSTART[18:1]
**(3)(4)DSTSTART** = (DSPSFFSET) * Yd + Xd AD: DSTSTART[18:1]

640 * 240 dots 256 colors

**Figure 5-19. BitBLT Function**

### (7) Pattern Start Address Register (H)

**PATSTART**
**Address: 10001060h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | PATSTART [18:16] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 2 ~ 0 | PATSTART[18:16] | 0000hex |

**(8) Pattern Start Address Register (L)**

**PATSTART**
**Address: 10001062h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PATSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PATSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | PATSTART[15:0], set VRAM start address of pattern data | 0000hex |

**(9) Mask Start Address Register (H)**

**MSKSTART**
**Address: 10001064h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | MSKSTART [18:16] | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 2 ~ 0 | MSKSTART[18:16]. | 0000hex |

**(10) Mask Start Address Register**

**MSKSTART**
**Address: 10001066h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MSKSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MSKSTART[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | MSKSTART[15:0], set VRAM start address of mask data | 0000hex |

**(11) ROP Register**

**ROP**
**Address: 10001068h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ROP[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | ROP[15:0] | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 0 | Set four (4) ROP codes for three (3) ROP operations. Only lower byte is valid. | 0000hex |

**BitBLT Mode Register**

**BITBLTMODE**
**Address: 1000106Ah**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | - | - | - | - | - | - |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | MSKENABLE | PATSELECT | SCREENSELECT | | - | SCANDRCT |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | - | - | R/W | R/W | R/W | R/W | - | R/W |

| Bit | Description | Default |
|---|---|---|
| 6 | **Reserved** | 0000hex |
| 5 | MSKENABLE, selects the mask operation or not<br>1: Enable<br>0: Disable | |
| 4 | PATSELECT, selects the filled data<br>1: Solid color<br>0: Bitmap Pattern (8x8 dots) | |
| 3 ~ 2 | **Selects the position of Source block and Destination block**<br>**00: On Screen to On Screen**<br>**01: On Screen to Off Screen**<br>**10: On Screen to On Screen**<br>**11: Off Screen to On Screen** | |
| 1 | **Reserved** | |
| 0 | SCANDRCT, determines the X, Y direction flow for BitBLT operation<br>1: Right to left, bottom to top<br>0: Left to right, top to bottom (default) | |

### 5.9 FRC Registers

Since these registers mainly serve to perform tests, the user access is not allowed for these registers.

**(1) FRC WRITE Data Register**

**FRC_WRITE**
**Address: 10001070h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Indirect address | 0000hex |
| 7 ~ 0 | Data to write | 0000hex |

**(2) FRC READ Address Register**

**FRC_READ_AD**
**Address: 10001072h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | - | - |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - |

**(2) FRC READ Address Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Set indirect address to be read | 0000hex |
| 7 ~ 0 | Reserved | 0000hex |

**(3) FRC READ Data Register**

**FRC_READ**
**Address: 10001074h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] | A[7:0] |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | R | R | R | R | R | R | R | R |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] | D[7:0] |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | R | R | R | R | R | R | R | R |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 8 | Indirect Address | XXXXhex |
| 7 ~ 0 | READ data (READ only) | XXXXhex |

These registers use indirect address access.

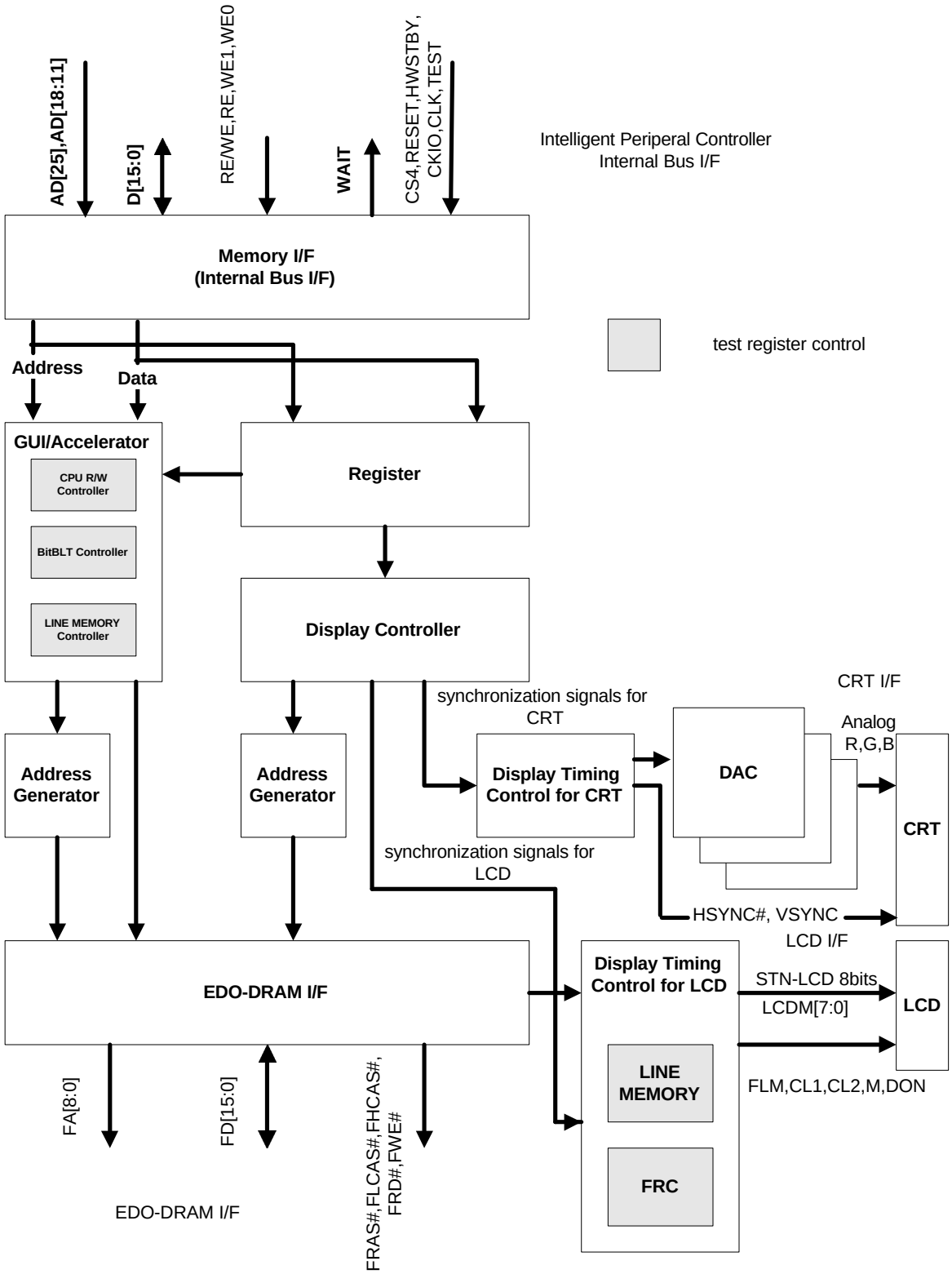



**Figure 5-20. LCD Control Block Diagram**

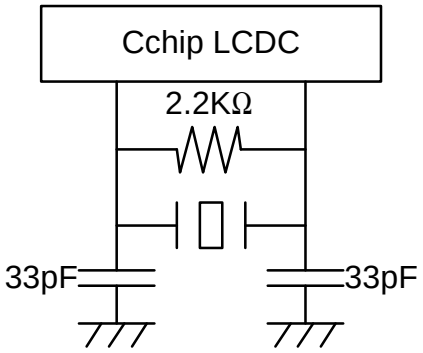



**Figure 5-21. Recommended CR Constants for LCDC Built-in Oscillator**

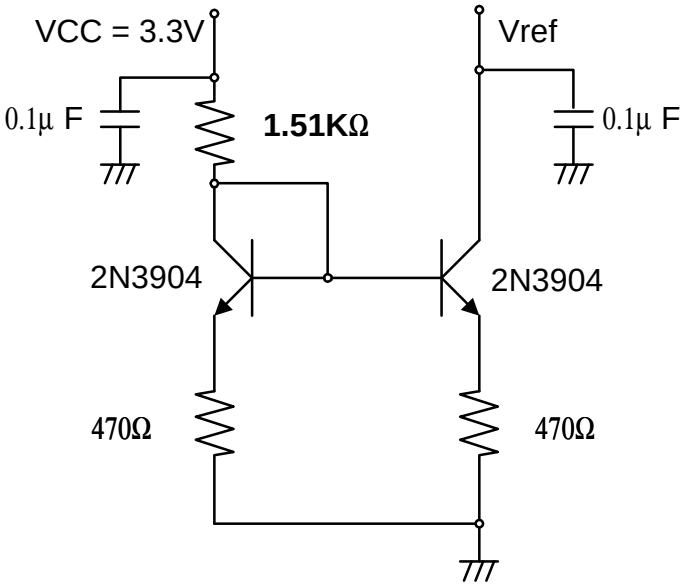



**Figure 5-22. Wilder Current Source Application Circuit for DAC Vref Input Pin**

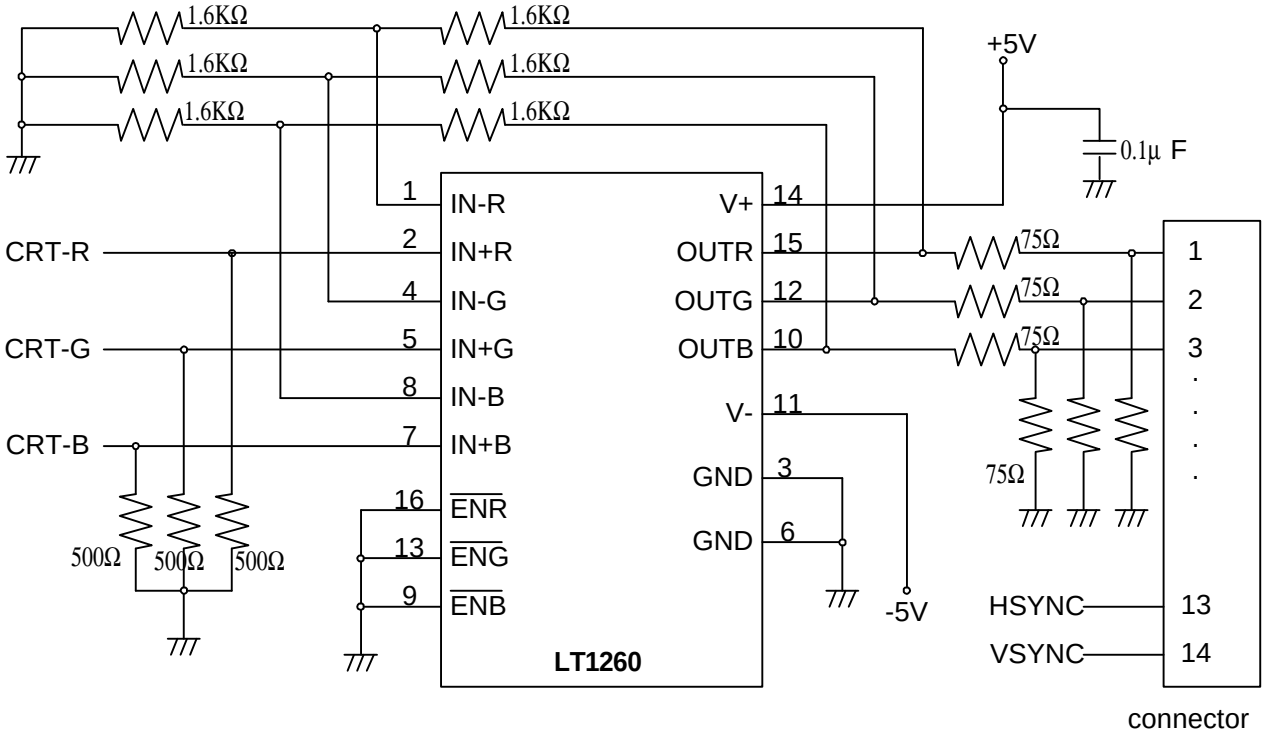



**Figure 5-23. Output Buffer Application Circuit for DAC Analog R, G, B Output Pins**

# 6. PC Card Controller (PCC) and Miniature Card Controller (MCC)

## 6.1 Overview

The PC Card Controller (PCC) controls the external and internal buffers, interrupts, and PCMCIA-defined ports of the PC card interfaces, which should be connected to the LSI. The PCC enables two slots of the PC cards that are compliant with the specifications PCMCIA Rev. 2.1/JEIDA Version 4.2, thereby ensuring a smooth connection to the LSI.

## 6.2 Features

- Two slots of the PC card interfaces can be simultaneously controlled.
- Supports IC memory card interface, and I/O and Memory card interface, which function as PC card interfaces and are connected to physical areas 6 and 5. Area 6, which is referred as channel 0, supports both of the IC memory card interface, and I/O & Memory card interface. Area 5, which is referred as channel 1, only supports IC memory card interface.
- Outputs control signals to the external buffer.
- Able to switch to an Attribute memory or a Common memory, or an I/O space via the CPU addresses.
- Provides a segment bit (an address bit for the PC card) for the Common memory; therefore, a 64-MB space of full PCMCIA specifications can be accessed.

## 6.3 Block Diagram

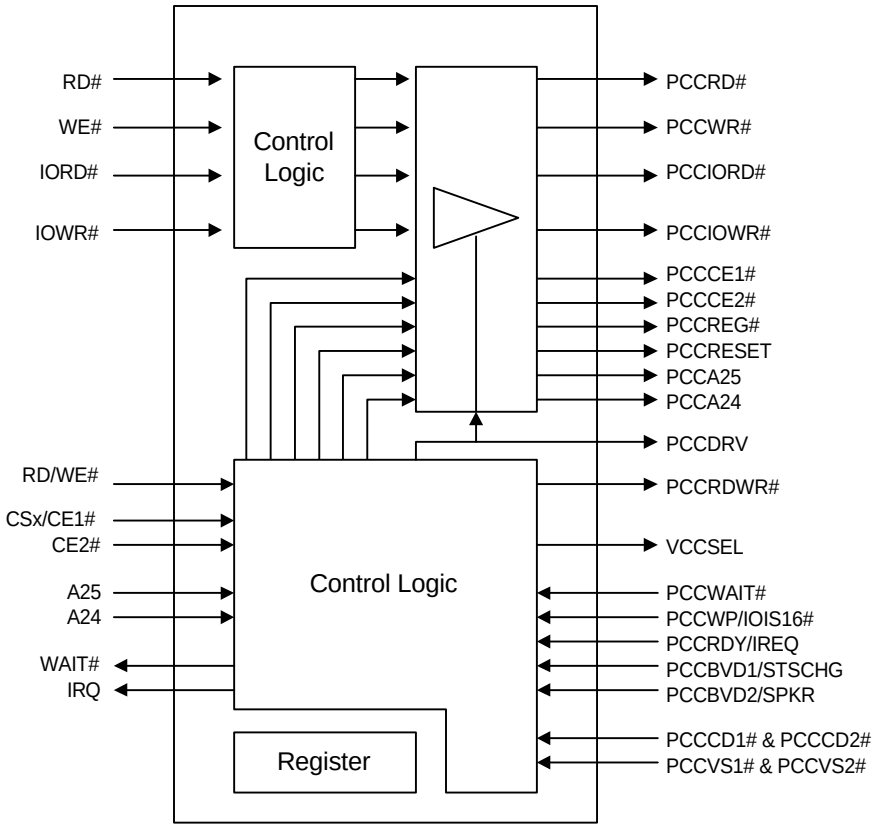



**Figure 6-1. Block Diagram of PC Card Controller**

### 6.4 Register Configuration

**Table 6-1. PC Card Controller Registers**

| Physical Area | Register Name | Symbol | READ/WRITE | Initial Value | Address | Access |
|---|---|---|---|---|---|---|
| Physical Area 6 (PCC0) | PCC0 interface status register | PCC0ISR | R | - | H'10002000 | 8 bits(16 bits) |
| | PCC0 general control register | PCC0GCR | R/W | H'00 | H'10002002 | 8 bits(16 bits) |
| | PCC0 card status change register | PCC0CSCR | R/W | H'00 | H'10002004 | 8 bits(16 bits) |
| | PCC0 card status change interrupt enable register | PCC0CSCIER | R/W | H'00 | H'10002006 | 8 bits(16 bits) |
| | PCC0 software control register | PCC0SCR | R/W | H'00 | H'10002008 | 8 bits(16 bits) |
| Physical Area 5 (PCC1) | PCC1 interface status register | PCC1ISR | R | - | H'10002010 | 8 bits(16 bits) |
| | PCC1 general control register | PCC1GCR | R/W | H'00 | H'10002012 | 8 bits(16 bits) |
| | PCC1 card status change register | PCC1CSCR | R/W | H'00 | H'10002014 | 8 bits(16 bits) |
| | PCC1 card status change interrupt enable register | PCC1CSCIER | R/W | H'00 | H'10002016 | 8 bits(16 bits) |
| | PCC1 software control register | PCC1SCR | R/W | H'00 | H'10002018 | 8 bits(16 bits) |
| General Control | PCC0 Output pins control Register | P0OCR | R/W | H'00 | H'1000202A | 8 bits(16 bits) |
| | PC Card General Control Register | PGCR | R/W | H'00 | H'1000202E | 8 bits(16 bits) |

Note -: The initial value is determined by the status of the PC card.

## 6.5 Register Descriptions

### 6.5.1 PCC0 Interface Status Register (PCC0ISR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | P0READY/ IREQ0 | P0MWP | P0VS2 | P0VS1 | P0CD2 | P0CD1 | P0BVD2 /SPKR0 | P0BVD1/ STSCHG0 |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | R | R | R | R | R | R | R | R |

Note -: The initial value is determined by the status of the PC card.

The PCC0 interface status register (PCC0ISR) is an 8-bit READ-only register, which reads the status of the PC card connected to PCC0. PCC0ISR is subject to the PC card status.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: Indicates that the value of pin PCC0RDY is 1 when the PC card connected to PCC0 is the IC memory card interface. Indicates that the value of pin IREQ is 1 when the I/O and Memory card interface is the PC card connected to PCC0.<br>If this bit is low: Indicates that the value of pin PCC0RDY is 0 when the PC card connected to PCC0 is the IC memory card interface. Indicates that the value of pin IREQ is 0 when the I/O and Memory card interface is the PC card connected to PCC0. | - |
| 6 | If this bit is high: Indicates that the value of pin PCC0WP# is 1 when the Memory card interface is the PC card connected to PCC0.<br>If this bit is low: Indicates that the value of pin PCC0WP# is 0 when the PC card connected to PCC0 is the IC memory card interface. The value of bit 6 is always 0 when the I/O and Memory card interface is the PC card connected to PCC0. | - |
| 5 | If this bit is high: Indicates that the value of pin PCC0VS2# of the PC card connected to PCC0 is 1.<br>If this bit is low: Indicates that the value of pin PCC0VS2# of the PC card connected to PCC0 is 0. | - |

**PCC0 Interface Status Register (PCC0ISR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 4 | If this bit is high: Indicates that the value of pin PCC0VS1# of the PC card connected to PCC0 is 1.<br>If this bit is low: Indicates that the value of pin PCC0VS1# in the PC card connected to PCC0 is 0. | - |
| 3 | If this bit is high: Indicates that the value of pin PCC0CD2# in the PC card connected to PCC0 is 1.<br>If this bit is low: Indicates that the value of pin PCC0CD2# in the PC card connected to PCC0 is 0. | - |
| 2 | If this bit is high: Indicates that the value of pin PCC0CD1# in the PC card connected to PCC0 is 1.<br>If this bit is low: Indicates that the value of pin PCC0CD1# in the PC card connected to PCC0 is 0. | - |
| IC Memory Interface | | |
| 1~0 | 11: Indicates that the battery voltage state of the PC card connected to PCC0 is normal. (Battery Good).<br>01: Indicates that the battery must be replaced although data integrity is guaranteed for the PC card connected to PCC0 (Battery Warning).<br>10: Indicates that the battery voltage state is abnormal and data integrity is not guaranteed for the PC card connected to PCC0 (Battery Dead).<br>00: Indicates that the battery voltage state is abnormal and data integrity is not guaranteed for the PC card connected to PCC0 (Battery Dead). | - |
| I/O Card Interface | | |
| 1 | 1: Indicates that the value of pin SPKR on the PC card connected to PCC0 is 1.<br>0: Indicates that the value of pin SPKR on the PC card connected to PCC0 is 0. | - |
| 0 | 1: Indicates that the value of pin STSCHG in the PC card connected to PCC0 is 1.<br>0: Indicates that the value of pin STSCHG in the PC card connected to PCC0 is 0. | - |

### 6.5.2 PCC0 General Control Register (PCC0GCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | P0DRVE | P0PCCR | P0PCCT | P0VCC0 | P0MMOD | P0PA25 | P0PA24 | P0REG |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The PCC0 general control register (PCC0GCR) is an 8-bit READ/WRITE register. It controls the external buffer, reset, address pins PCC0A25 and PCC0A24, and pin PCC0REG, and sets the PC card type for the PC card connected to PCC0. PCC0GCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

**PCC0 General Control Register (PCC0GCR) [cont'd]**

<table>
<tr><th>Bit</th><th>Description</th><th>Default</th></tr>
<tr><td>7</td><td>If this bit is high: Sets a low level to control pin PCC0DRV of the external buffer for the PC card connected to PCC0.<br>If this bit is low: Sets a high level to control pin PCC0DRV of the external buffer for the PC card connected to PCC0. (Initial value)</td><td>0</td></tr>
<tr><td>6</td><td>If this bit is high: Sets a high level to RESET pin PCC0RESET for the PC card connected to PCC0.<br>If this bit is low: Sets a low level to RESET pin PCC0RESET for the PC card connected to PCC0. (Initial value)</td><td>0</td></tr>
<tr><td>5</td><td>If this bit is high: Handles the PC card connected to PCC0 as the I/O and Memory card interface.<br>If this bit is low: Handles the PC card connected to PCC0 as the IC memory card interface. (Initial value)</td><td>0</td></tr>
<tr><td>4</td><td>If this bit is high: Sets a voltage control pin VCC0SEL0 to high level.<br>If this bit is low: Sets a voltage control pin VCC0SEL0 to low level.</td><td>0</td></tr>
<tr><td>3</td><td>If this bit is high: (continuous 16MB area mode)
<table>
<tr><th>Pin A25</th><th>Pin A24</th><th colspan="2">bit 2 bit 1</th><th>bit 0</th><th>PCMCIA Access Range</th></tr>
<tr><td>0</td><td>0</td><td colspan="2">don't care</td><td>don't care</td><td>16MB Attribute memory Area</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Memory Bank Select</td><td>don't care</td><td>16MB of 64MB Common memory Area</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">don't care</td><td>don't care</td><td>16-MB I/O Space</td></tr>
</table>
If this bit is low: (continuous 32MB area mode)
<table>
<tr><th>Pin A25</th><th>Pin A24</th><th>bit 2</th><th>bit 1</th><th>bit 0</th><th>PCMCIA Access Range</th></tr>
<tr><td>0</td><td>x</td><td>don't care</td><td>don't care</td><td>0</td><td>32MB Attribute memory Area</td></tr>
<tr><td>0</td><td>x</td><td>Memory Bank Select</td><td>don't care</td><td>1</td><td>32MB of 64MB Common memory Area</td></tr>
<tr><td>1</td><td>x</td><td>don't care</td><td>don't care</td><td>don't care</td><td>32MB I/O Space</td></tr>
</table></td><td>0</td></tr>
<tr><td>2</td><td>If this bit is high: When the Common memory space is accessed for the PC card connected to PCC0, 1 is output to pin PCC0A25.<br>If this bit is low: When the Common memory space is accessed for the PC card connected to PCC0, 0 is output to pin PCC0A25. (Initial value)</td><td>0</td></tr>
<tr><td>1</td><td>If this bit is high: When bit P0MMOD is 1 and the Common memory space is accessed for the PC card connected to PCC0, 1 is output to pin PCC0A24.<br>If this bit is low: When bit P0MMOD is 1 and the Common memory space is accessed for the PC card connected to PCC0, 0 is output to pin PCC0A24. (Initial value)</td><td>0</td></tr>
</table>

**PCC0 General Control Register (PCC0GCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 0 | If this bit is high: When bit 3 is 0 and the PC card connected to PCC0 is accessed, 1 is output to pin PCC0REG#.<br>If this bit is low: When bit 3 is 0 and the PC card connected to PCC0 is accessed, 0 is output to pin PCC0REG#. (Initial value) | 0 |

### 6.5.3 PCC0 Card Status Register (PCC0CSCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | P0SCDI | - | P0IREQ | P0SC | P0CDC | P0RC | P0BW | P0BD |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | - | R/W | R/W | R/W | R/W | R/W | R/W |

The PCC0 Card Status Change Register (PCC0CSCR) is an 8-bit READ and WRITE register. PCC0CSCR is set to 1 by each interrupt factor of the PC card connected to PCC0 (only bit 7 can be set to 1 as required). PCC0CSCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: Software card detection interrupt occurs for the PC card connected to PCC0.<br>If this bit is low: No software card detection interrupt occurs for the PC card connected to PCC0. (Initial value)<br>If bit 3 (card detection enable) in the PCC0 card status change interrupt enable register (PCC0CSCIER) is set to 1, a software card detect change interrupt can be generated by writing 1 to this bit.<br>If bit 3 (card detection enable) in the PCC0CSCIER is RESET to 0, interrupts will not occur even when writing "1" to this bit. | 0 |
| 6 | Reserved: The value to be written must be 0. | 0 |
| 5 | If this bit is high: Indicates that an interrupt request for the IREQ pin in the PC card has occurred when the PC card is in the I/O and Memory card interface.<br>If this bit is low: Indicates no interrupt request for the IREQ pin in the PC card when the PC card is in the I/O and Memory card interface. (Initial value)<br>This bit can be RESET to 0 only in the pulse mode. To RESET, write "0" to this bit. This bit is not changed if 1 is written.<br>In the level mode, bit 5 is a READ-only bit which reflects the state of IREQ pin(if the IREQ pin is in the low level, 1 is read). In this bit, 0 is always read in the IC memory card interface. | 0 |

**PCC0 Card Status Register (PCC0CSCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 4 | If this bit is high: Indicates that the STSCHG pin in the PC card is changed from 1 to 0 when the PC card is in the I/O and Memory card interface.<br>If this bit is low: Indicates that the value of pin STSCHG on the PC card remains unchanged when the PC card is in the I/O and Memory card interface. (Initial value)<br>When the STSCHG pin is changed from 1 to 0, this bit is set to 1. To RESET, write "0" to this bit when it is set to "1". This bit is not changed if 1 is written. In this bit, 0 is always read in the IC memory card interface. | 0 |
| 3 | If this bit is high: Indicates that CD1 and CD2 in the PC card are changed.<br>If this bit is low: Indicates that CD1 and CD2 in the PC card are not changed. (Initial value)<br>Write 0 to bit 3 in order to RESET this bit to 0. This bit is not changed if 1 is written. | 0 |
| 2 | If this bit is high: Indicates that pin READY in the PC card is changed from 0 to 1 when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pin READY in the PC card is not changed when the PC card is in the IC memory card interface. (Initial value)<br>WRITE 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |
| 1 | If this bit is high: Indicates that pins BVD2 and BVD1 in the PC card are in the battery warning state that "the battery must be replaced although the data integrity is guaranteed" when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pins BVD2 and BVD1 in the PC card are not in the battery warning state when the PC card is in the IC memory card interface. (Initial value)<br>This bit is updated when the BVD2 and BVD1 pins are changed. Write 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |
| 0 | If this bit is high: Indicates that pins BVD2 and BVD1 in the PC card are in the state that "the battery must be replaced since the data integrity is not guaranteed" when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pins BVD2 and BVD1 in the PC card are not in the state that "the battery must be replaced since the data integrity is not guaranteed" when the PC card is in the IC memory card interface. (Initial value)<br>This bit is updated when the BVD2 and BVD1 pins are changed. WRITE 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |

### 6.5.4 PCC0 Card Status Change Interrupt Enable Register (PCC0CSCIER)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | P0CRE | P0IREQE1 | P0IREQE0 | P0SCE | P0CDE | P0RE | P0BWE | P0BDE |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The PCC0 card status change interrupt enable register (PCC0CSCIER) is an 8-bit READ and WRITE register. PCC0CSCIER is capable of setting a valid or invalid interrupt for each interrupt factor of the PC card connected to PCC0. When register PCC0CSCIER is set to 1, the interrupt is valid, and invalid when the register is set to 0. PCC0CSCR can be initialized by power-up RESET. PCC0CSCIER is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: The general control register (PCC0GCR) and software control register (PCC0SCR) in the PCC0 are initialized when a PC card connection change is detected in PCC0.<br>If this bit is low: The general control register (PCC0GCR) and software control register (PCC0SCR) in the PCC0 are not initialized even when a PC card change is detected in PCC0. (Initial value) | 0 |
| 6 ~ 5 | 00: Any kind of IREQ interrupt request signal is not accepted for the PC card connected to PCC0. Bit 5 in the status change register (PCC0CSCR) functions as a READ-only bit, and can indicate the status of the inversion signal of the IREQ pin. (Initial value)<br>01: The level-mode IREQ interrupt request signal is accepted for the PC card connected to PCC0. In the level mode, an interrupt occurs when level 0 of the signal input from the IREQ pin is detected.<br>10: The pulse-mode IREQ interrupt request signal is accepted for the PC card connected to PCC0. In the pulse mode, an interrupt occurs when a falling edge from 1 to 0 of the signal input from the IREQ pin is detected.<br>11: The pulse-mode IREQ interrupt request signal is accepted for the PC card connected to PCC0. In the pulse mode, an interrupt occurs when a rising edge from 0 to 1 of the signal input from the IREQ pin is detected. | 0 |
| 4 | If this bit is high: An interrupt occurs for the PC card connected to PCC0 when the value of the PCC0BVD1 pin (STSCHG) is changed from 1 to 0.<br>If this bit is low: No interrupt occurs for the PC card connected to PCC0 regardless of the value of the PCC0BVD1 pin. (STSCHG) (Initial value) | 0 |
| 3 | If this bit is high: An interrupt occurs for the PC card connected to PCC0 when the values of the PCC0CD1# and PCC0CD2# pins are changed.<br>If this bit is low: No interrupt occurs for the PC card connected to PCC0 regardless of the values of the PCC0CD1# and PCC0CD2# pins. (Initial value) | 0 |

**PCC0 Card Status Change Interrupt Enable Register (PCC0CSCIER) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 2 | If this bit is high: An interrupt occurs for the PC card connected to PCC0 when the value of pin PCC0RDY is changed from 0 to 1.<br>If this bit is low: No interrupt occurs for the PC card connected to PCC0 regardless of the value of pin PCC0RDY. (Initial value) | 0 |
| 1 | If this bit is high: An interrupt occurs when pins PCC0BVD2 and PCC0BVD1 are in the state that "the battery must be replaced although the data integrity is guaranteed".<br>If this bit is low: No interrupt occurs when pins PCC0BVD2 and PCC0BVD1 are in the state that "the battery must be replaced although the data integrity is guaranteed". (Initial value) | 0 |
| 0 | If this bit is high: An interrupt occurs when pins PCC0BVD2 and PCC0BVD1 are in the state that "the battery must be replaced since the data integrity is not guaranteed".<br>If this bit is low: No interrupt occurs when the value of pins PCC0BVD2 and PCC0BVD1 are in the state that "the battery must be replaced since the data integrity is not guaranteed".<br>(Initial value) | 0 |

### 6.5.5 PCC0 Software Control Register (PCC0SCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | - | - | - | - | - | - | P0VCC1 | P0SWP |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The PCC0 Software Control Register (PCC0CSCR) is an 8-bit READ and WRITE register. The way it controls pin VCC0SEL1 resembles to that of pin P0VCC0 in the PCC0GCR register does to pin VCC0SEL0. This register is also responsible for PC Card memory window write protect. PCC0SCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 ~ 2 | Reserved | 0 |
| 1 | If this bit is high: Sets the voltage control pin VCC0SEL1 as high level.<br>If this bit is low: Sets the voltage control pin VCC0SEL1 as low level. | 0 |
| 0 | If this bit is high: Enables write protect. Write operations to the PC Card yield no response.<br>If this bit is low: Disables write protect. Write operations to the PC Card are allowed. | 0 |

### 6.5.6 PCC1 Interface Status Register (PCC1ISR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | P1READY | P1MWP | P1VS2 | P1VS1 | P1CD2 | P1CD1 | P1BVD2 | P1BVD1 |
| Initial Value | - | - | - | - | - | - | - | - |
| R/W | R | R | R | R | R | R | R | R |

Note - : The initial value is always reflected by the status of the PC card.

PCC1 Interface Status Register (PCC1ISR) is an 8-bit READ register, and reads the status of the PC card connected to PCC1. PCC1ISR always reflects the status of the connected PC card.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: Indicates that the value of pin READY is 1 when the IC memory card interface is the PC card connected to PCC1.<br>If this bit is low: Indicates that the value of pin READY is 0 when the IC memory card interface is the PC card connected to PCC1. | - |
| 6 | If this bit is high: Indicates that pin WP in the PC card connected to PCC1 is 1.<br>If this bit is low: Indicates that pin WP in the PC card connected to PCC1 is 0. | - |
| 5 | If this bit is high: Indicates that of pin VS2 in the PC card connected to PCC1 is 1.<br>If this bit is low: Indicates that pin VS2 in the PC card connected to PCC1 is 0. | - |
| 4 | If this bit is high: Indicates that pin VS1 in the PC card connected to PCC1 is 1.<br>If this bit is low: Indicates that pin VS1 in the PC card connected to PCC1 is 0. | - |
| 3 | If this bit is high: Indicates that pin CD2 on the PC card connected to PCC1 is 1.<br>If this bit is low: Indicates that pin CD2 on the PC card connected to PCC1 is 0. | - |
| 2 | If this bit is high: Indicates that pin CD1 in the PC card connected to PCC1 is 1.<br>If this bit is low: Indicates that pin CD1 in the PC card connected to PCC1 is 0. | - |

**PCC1 Interface Status Register (PCC1ISR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 1 ~ 0 | 00: Indicate that the battery voltage state for the PC card connected to PCC1 is abnormal and the data integrity is not guaranteed. (Battery Dead)<br>01: Indicate that the battery must be replaced although the data integrity is guaranteed for the PC card connected to PCC1. (Battery Warning)<br>10: Indicate that the battery voltage state for the PC card connected to PCC1 is abnormal and the data integrity is not guaranteed. (Battery Dead)<br>11: Indicate that the battery voltage state for the PC card connected to PCC1 is normal. (Battery Good) | - |

### 6.5.7 PCC1 General Control Register (PCC1GCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | P1DRVE | P1PCCR | - | P1VCC0 | P1MMOD | P1PA25 | P1PA24 | P1REG |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | - | R/W | R/W | R/W | R/W | R/W |

The PCC1 General Control Register (PCC1GCR) is an 8-bit READ/WRITE register, and controls the external buffer, reset, address pins PCC1A25 and PCC1A24, and pin PCC1REG, and sets the PC card type for the PC card connected to PCC1. PCC1GCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: Sets a low level to control pin PCC1DRV of the external buffer for the PC card connected to PCC1.<br>If this bit is low: Sets a high level to control pin PCC1DRV of the external buffer for the PC card connected to PCC1. (Initial value) | 0 |
| 6 | If this bit is high: Sets a high level to RESET pin PCC1RESET for the PC card connected to PCC1.<br>If this bit is low: Sets a low level to RESET pin PCC1RESET for the PC card connected to PCC1. (Initial value) | 0 |
| 5 | Reserved: The value to be written must be 0. | 0 |
| 4 | If this bit is high: Sets the voltage control pin VCC1SEL0 as high level.<br>If this bit is low: Sets the voltage control pin VCC1SEL0 as low level. | 0 |
| 3 | If this bit is high: Outputs the address pin A24 if accessed to pin PCCREG. When the Common memory space is accessed, outputs P1PA24 to pin PCC0A24 (continuous 16-MB area mode).<br>If this bit is low: Outputs bit P1REG to pin PCCREG, and outputs the address pin A24 if accessed to pin PCC0A24 (continuous 32-MB area mode). (Initial value) | 0 |

**PCC1 General Control Register (PCC1GCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 2 | If this bit is high: When the Common memory space is accessed for the PC card connected to PCC1, 1 is output to pin PCC0A25.<br>If this bit is low: When the Common memory space is accessed for the PC card connected to PCC1, 0 is output to pin PCC0A25. (Initial value) | 0 |
| 1 | If this bit is high: When bit P1MMOD is 1 and the Common memory space is accessed for the PC card connected to PCC1, 1 is output to pin PCC0A24.<br>If this bit is low: When bit P1MMOD is 1 and the Common memory space is accessed for the PC card connected to PCC1, 0 is output to pin PCC0A24. (Initial value) | 0 |
| 0 | If this bit is high: When the value of bit P1MMOD is 0 and the PC card connected to PCC1 is accessed, 1 is output to pin PCCREG.<br>If this bit is low: When the value of bit P1MMOD is 0 and the PC card connected to PCC1 is accessed, 0 is output to pin PCCREG. (Initial value) | 0 |

### 6.5.8 PCC1 Card Status Change Register (PCC1CSCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | P1SCDI | - | - | - | P1CDC | P1RC | P1BW | P1BD |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | - | - | - | R/W | R/W | R/W | R/W |

The PCC1 Card Status Change Register (PCC1CSCR) is an 8-bit READ and WRITE register. PCC1CSCR is set to 1 by each interrupt factor of the PC card connected to PCC1 (only bit 7 can be set to 1 as required). PCC1CSCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: Software card detection interrupt occurs for the PC card connected to PCC1.<br>If this bit is low: No software card detection interrupt occurs for the PC card connected to PCC1. (Initial value)<br>If bit 3 (card detection enable) in the PCC0 card status change interrupt enable register (PCC0CSCIER) is set to 1, a software card detect change interrupt can be generated by writing 1 to this bit.<br>If bit 3 (card detection enable) in the PCC0CSCIER is RESET to 0, interrupts will not occur even when writing "1" to this bit. | 0 |
| 6 ~ 4 | Reserved: The value to be written must be 0. | |

**PCC1 Card Status Change Register (PCC1CSCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 3 | If this bit is high: Indicates the values of pins CD1 and CD2 in the PC card has been changed.<br>If this bit is low: Indicates the values of pins CD1 and CD2 in the PC card are not changed. (Initial value)<br>Write 0 to bit 3 in order to RESET this bit to 0. This bit is not changed if 1 is written. | 0 |
| 2 | If this bit is high: Indicates that pin READY in the PC card is changed from 0 to 1 when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pin READY in the PC card is not changed when the PC card is in the IC memory card interface. (Initial value)<br>Write 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |
| 1 | If this bit is high: Indicates that pins BVD2 and BVD1 in the PC card are in the BATTERY WARNING state that "the battery must be replaced although the data integrity is guaranteed" when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pins BVD2 and BVD1 in the PC card are not in the BATTERY WARNING state when the PC card is in the IC memory card interface. (Initial value)<br>This bit is updated when the BVD2 and BVD1 pins are changed. Write 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |
| 0 | If this bit is high: Indicates that pins BVD2 and BVD1 in the PC card are in the state that "the battery must be replaced since the data integrity is not guaranteed" when the PC card is in the IC memory card interface.<br>If this bit is low: Indicates that pins BVD2 and BVD1 in the PC card are not in the state that "the battery must be replaced since the data integrity is not guaranteed" when the PC card is in the IC memory card interface. (Initial value)<br>This bit is updated when the BVD2 and BVD1 pins are changed. Write 0 to bit 2 in order to RESET this bit to 0. This bit is not changed if 1 is written. In this bit, 0 is always read in the I/O and Memory card interface. | 0 |

### 6.5.9 PCC1 Card Change Interrupt Enable Register (PCC1CSCIER)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | P1CRE | - | - | - | P1CDE | P1RE | P1BWE | P1BDE |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | - | - | - | R/W | R/W | R/W | R/W |

The PCC1 card status change interrupt enable register (PCC1CSCIER) is an 8-bit READ and WRITE register. PCC1CSCIER determines to issue valid or invalid interrupts for each interrupt factor of the PC card connected to PCC1. When PCC1CSCIER is set to 1, the interrupt is valid, and invalid when the register is set to 0. PCC1CSCIER is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: The general control register (PCC1GCR) and software control register (PCC1SCR) in the PCC1 is initialized when the PC card connection to PCC1 is detected.<br>If this bit is low: The general control register (PCC1GCR) and software control register (PCC1SCR) in the PCC1 is not initialized even when the PC card is detected in PCC1. (Initial value) | 0 |
| 6 ~ 4 | Reserved: The value to be written must be 0. | 0 |
| 3 | If this bit is high: An interrupt occurs for the PC card connected to PCC1 when there is a value change for pins CD1# and CD2# .<br>If this bit is low: No interrupt occurs for the PC card connected to PCC1 regardless of the values of the CD1# and CD2# pins. (Initial value) | 0 |
| 2 | If this bit is high: An interrupt occurs for the PC card connected to PCC1 when the value of pin READY is changed from 0 to 1.<br>If this bit is low: No interrupt occurs for the PC card connected to PCC1 regardless of the value of pin READY. (Initial value) | 0 |
| 1 | If this bit is high: An interrupt occurs when pins BVD2 and BVD1 are in the state that “the battery must be replaced although the data integrity is guaranteed”.<br>If this bit is low: No interrupt occurs when pins BVD2 and BVD1 are in the states that “the battery must be replaced although the data integrity is guaranteed” (Initial value) | 0 |
| 0 | If this bit is high: An interrupt occurs when pins BVD2 and BVD1 are in the state that “the battery must be replaced since the data integrity is not guaranteed”.<br>If this bit is low: No interrupt occurs when pins BVD2 and BVD1 are in the state that “the battery must be replaced since the data integrity is not guaranteed”. (Initial value) | 0 |

### 6.5.10 PCC1 Software Control Register (PCC1SCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | P1VCC1 | P1SWP |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The PCC1 Software Control Register (PCC1CSCR) is an 8-bit READ and WRITE register. The way it controls pin VCC1SEL1 resembles to that of pin P1VCC0 in the PCC1GCR register does to pin VCC1SEL0. This register is also responsible for PC Card memory window write protect. PCC1SCR is initialized at power-up RESET, and holds its value at soft RESET or in software-based STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 ~ 2 | Reserved | 0 |
| 1 | If this bit is high: Sets the voltage control pin VCC1SEL1 to high level.<br>If this bit is low: Sets the voltage control pin VCC1SEL1 to low level. | 0 |
| 0 | If this bit is high: Enables write protect. Write operations to the PC Card yield no response.<br>If this bit is low: Disables write protect. Write operations to the PC Card are allowed. | 0 |

### 6.5.11 PCC0 Output Control Register (P0OCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | P0DEPLUP | - | - | P0AEPLUP | - | - | - | - |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | - | - | R/W | - | - | - | - |

The PCC0 Output Control Register (P0OCR), an 8-bit READ and WRITE register, controls the output pull-up for address bus and data bus.

P0OCR is initialized at power-up RESET, and holds its value at SOFTWARE RESET or in software STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 | If this bit is high: PCC0D15 - PCC0D0 supports the pull up resistance.<br>If this bit is low: PCC0D15 - PCC0D0 does not support the pull up resistance. | 0 |
| 6 ~ 5 | Reserved | 0 |
| 4 | If this bit is high: PCC0A25 - PCC0A0 supports the pull up resistance.<br>If this bit is low: PCC0A25 - PCC0A0 does not support the pull up resistance. | 0 |
| 3 ~ 0 | Reserved | 0 |

### 6.5.12 General Control Register (PGCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | - | - | - | - | PSSDIR | PSSRDWR |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | - | - | - | - | - | - | R/W | R/W |

The general control register (PGCR), an 8-bit READ and WRITE register, controls the PCCRDWR.

PGCR is initialized at power-up RESET, and holds its value at SOFTWARE RESET or in software STANDBY mode.

| Bit | Description | Default |
|---|---|---|
| 7 ~ 2 | Reserved: The read value is always 0. | 0 |
| 1 | If this bit is high: PCCRDWR is invert CPU RDWR# signal.<br>If this bit is low: PCCRDWR is the same as the CPU RDWR# signal. | 0 |
| 0 | If this bit is high: Always toggles when the CPU RDWR# is toggled.<br>If this bit is low: When not accessing PC card or Miniature card, PCCRDWR is not toggled. | 0 |

# 7. AFE Interface

## 7.1 Overview

An AFE interface is a circuit to interface with Modem AFE; and is capable of performing a serial data transfer function. A divider is also incorporated to transmit a master clock to Modem AFE.

### 7.1.1 Features

1) Supports full-duplex serial-data transfer can be achieved with the presence of buffers. The buffers can be independently used for data transmit and receive.

2) Data can be transmitted to and received from the CPU in each 1-word unit to 48-word unit. An AFE interface contains a 1-word data register and two 48-word data buffers, which can be selected for data READ or WRITE by users based on the applications.

3) Users can perform READ or WRITE operations to only one buffer. Although two buffers are generally involved for each data transmit or receive, users can use just one buffer, which is not currently used for the external transfer.

4) All the transmit/receive registers and accessible buffers are memory-mapped.

5) Data transmit/receive is performed via an interrupt signal. An AFE interface generates a transmit data empty interrupt and a receive data full interrupt to request data transmit or receive.

6) Data transfer is performed in the MSB-First way.

7) Supports three division ratio options: 1/8, 1/7, or 1/6.

### 7.1.2 Block Diagram

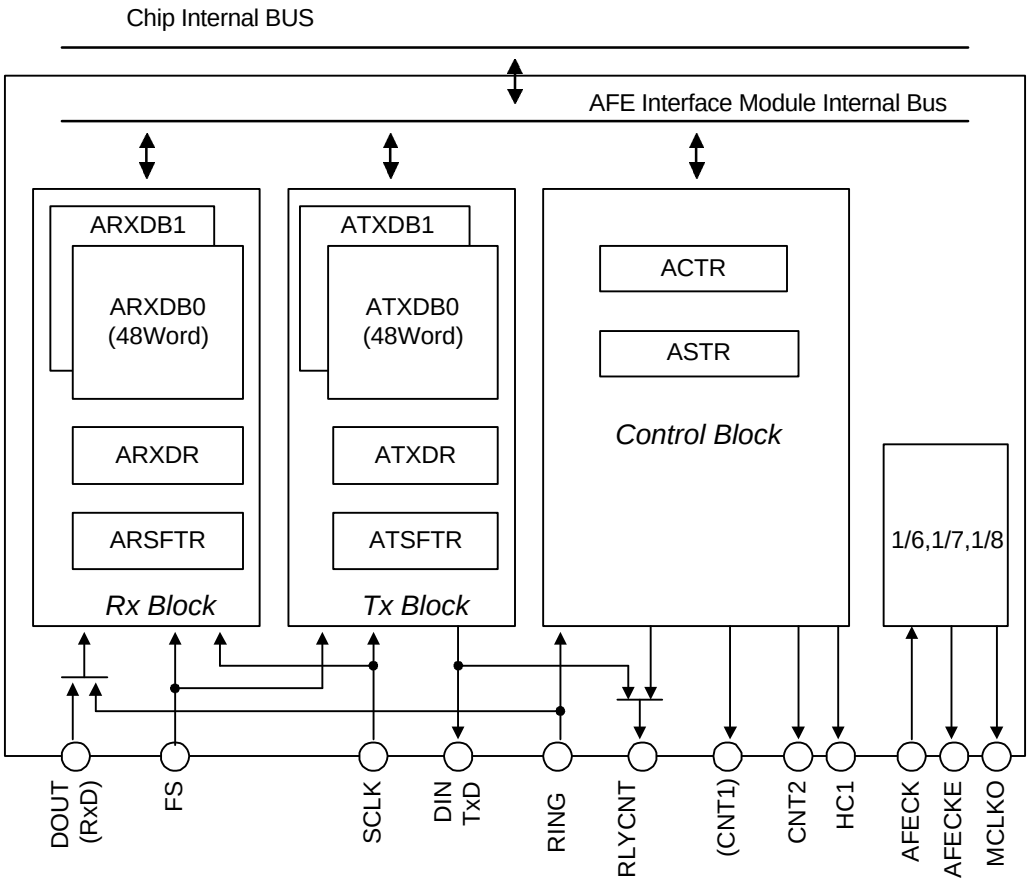



**Figure 7-1. AFE Interface Block Diagram**

**Table 7-1. Pin Function of AFE Interface Module**

| Name | I/O | Pin Function |
|---|---|---|
| DOUT(RxD) | I | Serial Receive Data Input Pin, from AFE module |
| FS | I | Frame Sync Signal Input Pin |
| SCLK | I | Shift Clock Input Pin |
| DIN(TxD) | O | Serial Transmit Data Output Pin, to AFE module |
| RESETO# (CNT1) | O | External Chip Control Signal 1 Output Pin (RESETO#) |
| PWRDWNO #(CNT2) | O | External Chip Control Signal 2 Output Pin (PWRDWNO#) |
| RLYCNT | O | RLYCNT Control and Dial Pulse Output Pin |
| HC1 | O | Hardware Control Signal 1 for STLC7546 |

**Table 7-1. Pin Function of AFE Interface Module (cont'd)**

| Name | I/O | Pin Function |
|---|---|---|
| RING | I | Ringing Signal Input Pin |
| AFECK | I | Crystal Oscillator clock input Pin |
| AFECKE | I/O | Crystal Oscillator Output Pin |
| MCKO | O | Master Clock for Modem Pin |

### 7.2 Register Description

An AFE interface contains registers and buffers shown in the table below.

**Table 7-2. Registers of AFE Interface**

| Register or Buffer | Function | Access Size | Address |
|---|---|---|---|
| ACTR | AFE I/F Control Register | 16 bits | 10003200 |
| ASTR | AFE I/F Status Register | 16 bits | 10003202 |
| ATXDR | Transmit Data Register | 16 bits | 10003206 |
| ARXDR | Receive Data Register | 16 bits | 10003204 |
| ATXDB0,1 | Transmit Data Buffers 0,1 | 16 bits | 10003100 - 5F |
| ATSFTR | Transmit Shift Register | Can not be accessed | * |
| ARXDB0,1 | Receive Data Buffers Register 0,1 | 16 bits | 10003000 - 5F |
| ARSFTR | Receive Shift register | Can not be accessed | * |

#### 7.2.1 AFE Control Register (ACTR)

**ACTR**, a 16-bit READ/WRITE register, is used to control an AFE interface. All the bits on this register are initialized to 0 at RESET. **ACTR** is not initialized in the STANDBY mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | HC | Div2 | Div1 | RLYCNT | CNT2 | CNT1 | TSW | RSW |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | RDETM | TEIE | REIE | TXIE | RXIE | BUFD | TE | RE |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**AFE Control Register (ACTR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 15 | When this bit is set to 1, 1 is output from the HC1 pin when the next transmit ends, and then the value of ATXDR is output when the second FS is received. After that, this bit is cleared to 0. | 0 |
| 14, 13 | Variable M setting for division ratio<br>00: Division ratio is 1/8<br>01: Division ratio is 1/7<br>10: Division ratio is 1/6<br>11: Reserved | 0 |
| 12 | RLYCNT pin output setting. Output from the RLYCNT pin. | 0 |
| 11 | External control signal 2 (CNT2) setting. Output from the PWRDWNO# pin. | 0 |
| 10 | External control signal 1 (CNT1) setting. Output from the RESETO# Pin. | 0 |
| 9 | RLYCNT pin output switch<br>1: transmitted data is output from the RLYCNT pin.<br>0: the value is output, and is set via bit 12 of the RLYCNT pin. | 0 |
| 8 | Receive data input pin switch<br>1: RING pin input indicates the received data.<br>0: DOUT (RxD) pin input indicates the received data. | 0 |
| 7 | RDET Interrupt MASK<br>1: disable 0: enable | 0 |
| 6 | Transmit Error Interrupt (TERI) enable<br>1: enable 0: disable | 0 |
| 5 | Receive Error Interrupt (RERI) enable<br>1: enable 0: disable | 0 |
| 4 | Transmit Data Empty Interrupt (TDEI) enable<br>1: enable 0: disable | 0 |
| 3 | Receive Data Full Interrupt (RDFI) enable<br>1: enable 0: disable | 0 |
| 2 | Buffer Disable<br>1: data is transferred with register (ATXDB and ARXDB).<br>0: data is transferred with buffers (ATXDB and ARXDB). | 0 |
| 1 | Transmit Enable<br>1: enable 0: disable | 0 |
| 0 | Receive enable.<br>1: enable 0: disable | 0 |

### 7.2.2 AFE Status Register (ASTR)

**ASTR**, a 6-bit READ only register (0s can only be written to lower four bits for clearing after 1s are read), indicates the status of an AFE interface. **ASTR** is not initialized in the STANDBY mode. **ASTR** must be read in word. The valid values cannot be guaranteed after a byte read is performed.

| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | TAB | RAB | reserved | reserved | reserved | reserved | reserved | reserved |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/(W) | R/(W) | R | R | R | R | R | R |

| **Bit** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | reserved | reserved | reserved | reserved | TERR | RERR | TDE | RDF |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| **R/W** | R | R | R | R | R/(W) | R/(W) | R/(W) | R/(W) |

| **Bit** | **Description** | **Default** |
|---|---|---|
| 15 | Indicates the transmit buffer is accessible<br>1: READ/WRITE can be performed to ATXDB1.<br>0: READ/WRITE can be performed to ATXDB0.<br><br>This bit will be set when the following two conditions are met.<br>1) When only transmit data buffer 1 is empty<br>2) When the TE bit in **ACTR** is set to 1<br><br>The bit will be cleared when either one of the following conditions is met.<br>1) When transmit data buffer 0 becomes empty<br>2) When the TE bit in ACTR is cleared to 0<br>3) At RESET<br>This bit can be written to when the TE bit is 0. | 0 |
| 14 | Indicates the receive-buffer is accessible<br>1: READ/WRITE can be performed to ARXDB1.<br>0: READ/WRITE can be performed to ARXDB0.<br><br>Set condition:<br>1) This bit will be set when the receive data buffer 1 is full and receive data buffer 0 is not full<br>2) When the RE bit in **ACTR** is set to 1<br><br>This bit will be cleared when either one of the following conditions is met.<br>1) When receive data buffer 0 becomes full<br>2) When RE bit in **ACTR** is cleared to 0<br>3) At RESET<br>This bit can be written to when the RE bit is 0. | 0 |
| 13 ~ 4 | Reserved | 0 |

**AFE Status Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 3 | Indicates a transmit error<br>1: indicates that a transmission error has occurred.<br>0: indicates that a transmission error does not occur.<br><br>This bit will be set when the next FS is received while both transmit data buffers are empty.<br><br>This bit will be cleared when either one of the following conditions is met.<br>1) At RESET<br>2) When **ASTR** is read and 0 is written to this bit, after the bit is set to 1 | 0 |
| 2 | Receive error indication<br>1: indicates that a receive error has occurred.<br>0: indicates that a receive error does not occur.<br><br>This bit will be set when the next data receive is completed while both receive data buffers are full.<br><br>This bit will be cleared when either one of the following conditions is met.<br>1) At RESET<br>2) When **ASTR** is read and 0 is written to this bit, after the bit is set to 1 | 0 |
| 1 | Indicates that no transmitted data are in either one of the two transmit data buffers (**ATXDR**).<br>1: indicates that at least either one of the two transmit data buffers (**ATXDR**) does not have the transmitted data.<br>0: indicates that both transmit data buffers contain the transmitted data.<br><br>This bit will be set when the following conditions are met.<br>1) At RESET<br>2) When the data in either one of the two transmit data buffers are Completely transmitted.<br>3) When the TE bit in **ACTR** is cleared to 0<br><br>This bit will be cleared when **ASTR** is read and 0 is written to this bit, after the bit is set to 1.<br><br>Note: When both of the transmit data buffers are empty (as in the cases when the TE bit is cleared to 0), a clear operation must be performed twice since the empty status of only one buffer is canceled, which is indicated by the TAB bit. | 0 |

**AFE Status Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 0 | Indicates that one or two receive data buffers (ARXDR) are full of the received data.<br>1: indicates that at least one receive data buffer is full of the received data.<br>0: indicates that two receive data buffers are not completely full.<br><br>This bit will be set when data are stored in ARXDR, or in all the words in ARXDB0 or ARXDB1.<br><br>This bit will be cleared when either one of the following conditions is met.<br>1) At RESET<br>2) When STR is READ and 0 is written to this bit, after the bit is set to 1.<br>3) When the RE bit in **ACTR** is cleared to 0<br><br>Note: A clear operation must be performed twice when both of the receive data buffers are full since the full status of only one receive data buffer has been canceled as indicated by RAB. | 0 |

### 7.2.3 AFE Transmit Data Register (ATXDR)

**ATXDR**, a 16-bit READ/WRITE register, is used to transmit the stored data. All the bits in this register are initialized to 0 at RESET. **ATXDR** is not initialized in the STANDBY mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

ATXDR functions as a transmit data register when the BUFD bit (bit 15) in CTR is 1, and an AFE control data transmit register when the BUFD bit is 0. (see Figure 5.1)

### 7.2.4 AFE Receive Data Register (ARXDR)

**ARXDR**, a 16-bit READ only register, is used to receive the stored data. All the bits in this register are initialized to 0 at RESET. **ARXDR** is not initialized in the STANDBY mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

**ARXDR** functions as a receive data register when the BUFD bit (bit 15) in CTR is 1, and an AFC control data receive register when the BUFD bit is 0. AFE control data are stored and transmitted to **ATXDR** at the same time.

### 7.2.5 AFE Transmit Data Buffers (ATXDB0,1)

**ATXDB0** and **ATXDB1** act as transmit data storage buffers, and are able to store 48-word data. The hardware configuration determines the buffer, from which the data are transmitted. From which buffer data is transmitted depends on a hardware configuration. Users can access only one buffer, which is not currently used for data transmit. **ATDB0** and **ATDB1** are not initialized in the STANDBY mode.

### 7.2.6 AFE Transmit Shift Register (ATSFTR)

**ATSFTR**, a 16-bit register, is used to convert a parallel transmit data into a serial one. Note that READ/WRITE operations cannot be performed to this register. The initial value of this register is undefined at RESET or in the STANDBY mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

### 7.2.7 AFE Receive Data Buffers (ARXDB0,1)

**ARXDB0** and **ARXDB1** are receive data storage buffers, and are able to store 48-word data. The hardware configuration determines the buffer, where the data are received. Users can access only one buffer that is not used to receive data. **ARDB0** and **ARDB1** are not initialized in the STANDBY mode.

### 7.2.8 AFE Receive Shift Register (ARSFTR)

**ARSFTR**, a 16-bit register, is used to convert a serial receive data into a parallel one. Note that READ/WRITE operations cannot be performed to this register. The initial value of this register is undefined at RESET or in the STANDBY mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R/W | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

## 7.3 Data Transfer

### 7.3.1 Data Transmit

Data are transmitted by setting the TE bit in ACTR to 1. The transmitted data are stored in ATXDR (transmit data register), or ATXSB0/ATXDB1 (transmit data buffers 0 or 1), which can be selected by the BUFD bit in ACTR.

#### 7.3.1.1 Data Transmit with Buffer

When data are transmitted via ATXDB0/ATXDB1, buffer 0 or 1, which is used for data transmission, is selected by hardware. This will enable the CPU (SH3) to access only one buffer, which not used for data transmission.
When the data in the buffer 0 data are completely transmitted, a transmit data empty interrupt (TDEI) is generated to the CPU interface, and an interrupt request is then output as a chip interrupt from the CPU interface to the CPU (SH3). A transmit data error interrupt (TERI) is then output if FS (frame synchronous signal) are received when the data in the buffer 1 are completely transmitted and the next data to be transmitted is not written. When a buffer (ATXDB0/ATXDB1) is used for data transmission, a transmit data register (ATXDR) is used as a transmit register to control the AFE data. (see section 7.5)

#### 7.3.1.2 Data Transmit with Register

When data are transmitted via ATXDR, data stored in ATXDR are used as the transmitted data. When data transmission starts in ATXDR, TDEI is output. ATERI is output when the next FX is received before the transmitted data are written to ATXDR.

#### 7.3.1.3 Before 1st Data Transmit in Buffer Use Mode

In an AFE-I/F module, it is defined that both transmit data buffers are empty when the TE bit is 0. Consequently, data must be written to both transmit data buffers and the TDE bit in ASTR must be cleared before initiating the data transmit (before the TE bit is set to 1). Since the TAB bit is 0 when they are empty, the TAB bit should be first set to 1 by the first clear operation, and then cleared to 0 by the second clear operation.

The following details how the whole procedure works:

1. 48 words of data are written to one transmit data buffer.
2. STR is read and 0 is written to bit 1.
3. Further 48 words of data are written to the other transmit data buffer.
4. STR is read and 0 is written to bit 1.

If the TDE bit is cleared without writing any data to transmit data buffers (only steps 2 and 4 in the above procedure are performed), the output value cannot be guaranteed for the first 96 words of data.

### 7.3.2 Data Receive

Data are received by setting the RE bit in ACTR to 1.Received data can be stored in ARXDR (receive data register) or ARXDB0/ARXDB1 (receive data buffer 0 or 1), which is determined by the BUFD bit in ACTR.

#### 7.3.2.1 Data Receive with Buffer

When data are received via RXDB0/RXDB1, in which the data received in buffer 0 or 1 are stored and selected by hardware. At this moment, the CPU (SH3) can only access one buffer, which is not used to receive data.

When the received data are completely stored in one buffer, a receive data full interrupt (RDFI) is output. A receive data error interrupt (RERI) is output when a received data is pending while the received data have been fully written in the two buffers.

When a buffer is used to receive data, RXDR is used as an AFE control data receive register, in which data are stored and transmitted synchronously via the third FS (frame synchronous single) after the HC bit is set to 1.

#### 7.3.2.2 Data Receive with Register

When data are received in RXDR, the received data are stored in RXDR.

When data are stored in RXDR, RDFI is output. A receive data error interrupt is output when the next data are received in the receive data full status.

#### 7.3.2.3 When Both Receive Data Buffers Are Full

If both receive data buffers become full, the RDF bit must be cleared (clearing to 0 after reading 1) twice in the same way as described in section 7.3.1.3 on the last page. (However, since both receive data buffers are initially empty, it can be considered erroneous occurrences if they are simultaneously full.)

### 7.4 Divider

In the divider, division ratio can be selected among 1/8, 1/7, and 1/6 via the Div1 and the Div2 bits in CTR (see figure 7-2 below).

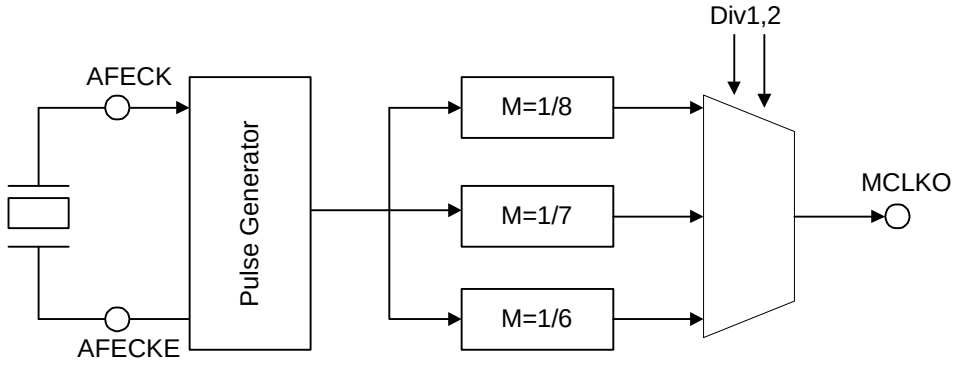



**Figure 7-2. Divider Configuration**

### 7.5 External Chip Control Signal

An AFE interface is capable of transmitting the three external chip control signals of RESETO#, PWRDWNO# and HC1. The output for each of the signals is individually controlled by the corresponding bits in CRT. For the two signals of CNT1(RESETO#) and CNT2(PWRDWNO#), the values set in CTR are output without delay. HC1, on the other hand, is output when the data transfer finishes (point A of figure 7-3) immediately after the HC1 bit is set to 1. After a data is successfully transferred into a control data (point B of figure 7-3), the output value of HC1 output is 0 and the bit in CTR is cleared to 0 (see figure 7-3).
Note that the HC1 bit can be used for the HC1 pin in STL7546 of SGS Thomson.

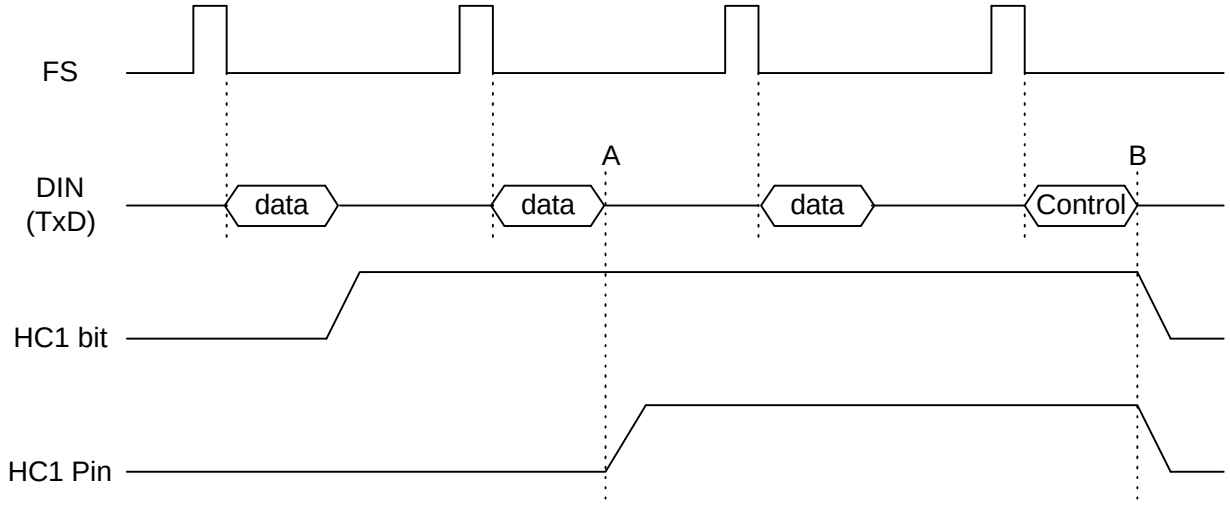



**Figure 7-3. HC1 Pin and Control Data Outputs**

### 7.6 Interrupt

An AFE interface is capable of generating five interrupts. Among these interrupts, four interrupts of TDEI, RDFI, TERI, and RERI are issued by setting the enable bits in CTR to 1. On the other hand, an interrupt of RDWT is masked by setting the RDETM bit to 1.

| Interrupt Source | Issuance Condition | How to clear the interrupt |
|---|---|---|
| TDEI | Transmit register or buffer includes no transmit data. | Clear the TDE bit in STR |
| RDFI | Receive register or buffer is full of received data. | Clear the RDF bit in STR |
| TERI | Next data transmit starts while no transmit data is included. | Clear the TERR bit in STR |
| RERI | Receive register or buffer receives the next data in spite of being in the full status. | Clear the RERR bit in STR |
| RDET | When a low level is input to the RING pin (this is a level interrupt). | Write 1 to the RSW bit in CTR |

Figures 7-4 and 7-5 shown below display the output timings of TDEI and RDFI.
For timings of TERI and RERI, TERI is output when the last word data transmission starts while RERI is output when the last word data transmission is completed. When the BUFD bit is set to 1, transmission is performed in 1 word, but output timings do not differ from those of TDEI and RDFI.

**The procedure required to clear TERI and RERI is as follows: Stop the XMTR (TERR) or RCV (RERR), clear the (TDE, TERR) or (RDE, RERR) bit pairs in the STR, then re-enable the SHTR or RCVR. Note, for duplex transfer, both RERR and TERR occur simultaneously as per timing outlined in Figures 7.4/7.5.**

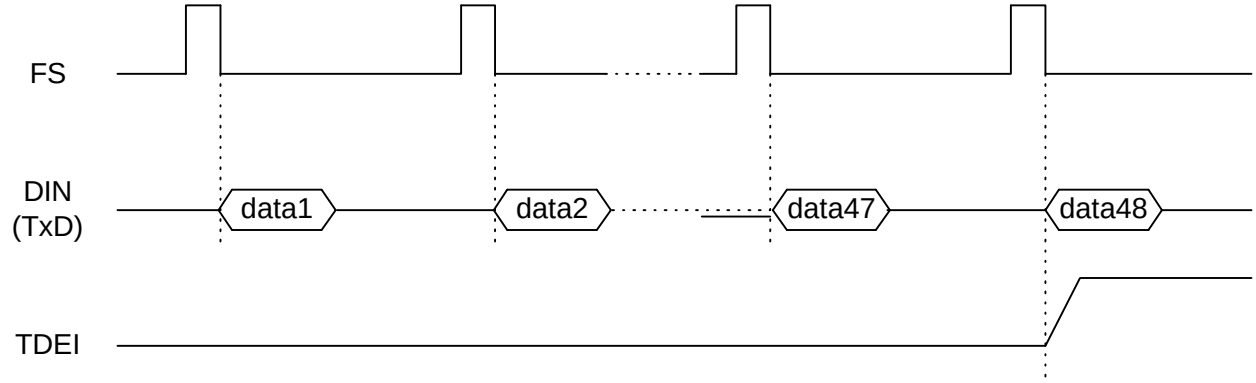



**Figure 7-4. TDEI Output Timing**

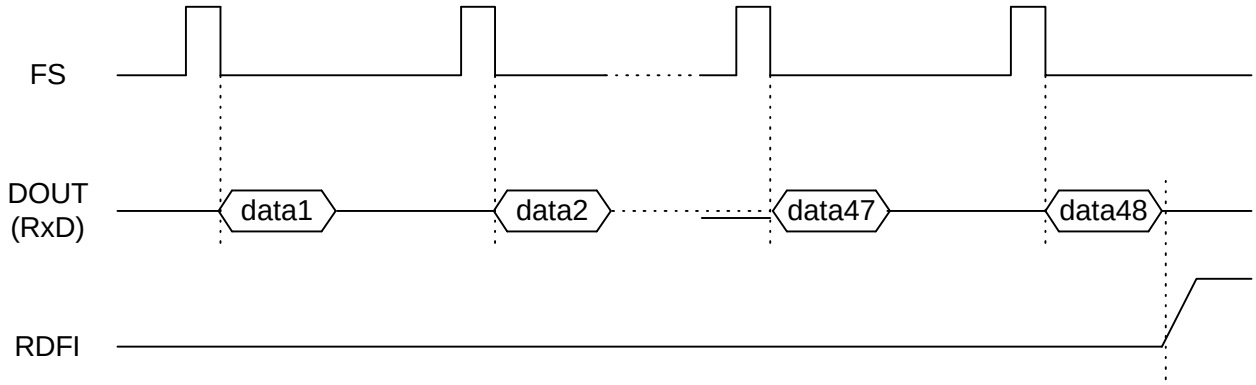



**Figure 7-5. RDFI Output Timing**

### 7.7 How to Use the Special Pin (RLYCNT, RING)

An AFE interface contains two special pins : RLYCNT and RING.

#### 7.7.1 How to Use the RLYCNT Pin

The RLYCNT pin is used for relay control and dial pulse generation. Relay control is achieved by writing a value to the RLYCNT bit in CTR while the TSW bit in CTR is 0. A RLYCNT pin output is the value set in the RLYCNT bit.

Dial pulses can be generated by setting the TSW bit in CTR to 1 and writing data to buffers of data transmission. At this moment, an Modem interface must be activated and the FS must be accepted after one word of data is transmitted. The value of the last bit is maintained until the next data transmission starts.)

#### 7.7.2 How to Use the RING Pin

The RING pin is used to detect a ringing signal. For this purpose, an AFE interface issues an interrupt when the RING pin goes low (the RDETM bit must remain at 0). By setting the RSW and the RDETM bits to 1, reading the value of the RING pin at a receive data buffer and calculating the cycles of 0 and 1 can be performed while the ringing signal is detected. **Receiving data requires AFE to generate FS and SCLK.**

Note that a RING interrupt is canceled when the RDETM bit is set to 1.

### 7.8 Attachment

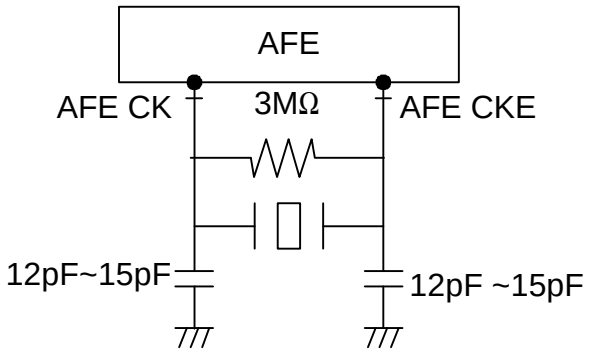



**Figure 7-6. Recommended CR Constants for AFE Built-in Oscillator**

# 8. Pin Function Controller & I/O Port

## 8.1 Overview

The LSI incorporates four (4) 8-bit ports (Port A-Port D). As shown in the table 8-1, the port pins are multiplexed with other functions, which are controlled by Port Control Registers (GPACR - GPDCR). Each port contains an 8-bit data register which stores the data to the pins. Each I/O port pin has a pull-up MOS, which is controlled by Port Control Register to determine if this pin will be pulled up or not. The Interrupt Control Registers (GPAICR - GPDICR) are also included to control each pin which can be enabled or disabled to generate an Interrupt signal. As interrupt events occur at any GPIO pin, the Interrupt status Register (GPAISR - GPDISR) can record the occurring interrupt events, which can be read by system.

### 8.1.1 Features

- Input pull-up on/off control
- Interrupt events can be independently generated or masked on each I/O pin.
- Function multiplex with IrDA, UART, miniature and PCMCIA
- Power down control by software

**Table 8-1. The List of I/O Port Pin Function Configurations**

| Port | Function 1 | Function 2 |
|---|---|---|
| A | PA7 I/O (port) | MODSEL / RX2 (IrDA) |
| A | PA6 I/O (port) | TXD (IrDA) |
| A | PA5 I/O (port) | RX# (IrDA) |
| A | PA4 I/O (port) | IRCLK (IrDA) |
| A | PA3 I/O (port) | TMO1# (Timer) |
| A | PA2 I/O (port) | TMO0# (Timer) |
| A | PA1 I/O (port) | no function |
| A | PA0 I/O (port) | no function |
| B | PB7 I/O (port) | Tx# (UART) |
| B | PB6 I/O (port) | Rx# (UART) |
| B | PB5 I/O (port) | RTS# (UART) |
| B | PB4 I/O (port) | CTS# (UART) |
| B | PB3 I/O (port) | DTR# (UART) |
| B | PB2 I/O (port) | DSR# (UART) |
| B | PB1 I/O (port) | DCD# (UART) |
| B | PB0 I/O (port) | RI# (UART) |
| C | PC7 I/O (port) | PCC1CD2# (PCMCIA1) |
| C | PC6 I/O (port) | PCC1CD1# (PCMCIA1) |
| C | PC5 I/O (port) | PCC1WAIT# (PCMCIA1) |

**Table 8-1. The List of I/O Port Pin Function Configurations (cont'd)**

| Port | Function 1 | Function 2 |
|---|---|---|
| C | PC4 I/O (port) | WEA# (PCMCIA1) |
| C | PC3 I/O (port) | RDA# (PCMCIA1) |
| C | PC2 I/O (port) | CE2A# (PCMCIA1) |
| C | PC1 I/O (port) | CE1A# (PCMCIA1) |
| C | PC0 I/O (port) | PCC1DRV (PCMCIA1) |
| D | PD7 I/O (port) | PCC1BVD2 (PCMCIA1) |
| D | PD6 I/O (port) | PCC1BVD1 (PCMCIA1) |
| D | PD5 I/O (port) | PCC1RDY (PCMCIA1) |
| D | PD4 I/O (port) | PCC1WP# (PCMCIA1) |
| D | PD3 I/O (port) | PCC1A24 (PCMCIA1) |
| D | PD2 I/O (port) | PCC1A25 (PCMCIA1) |
| D | PD1 I/O (port) | PCC1VS2# (PCMCIA1) |
| D | PD0 I/O (port) | PCC1VS1# (PCMCIA1) |

### 8.2 Register Configuration

Each I/O Port consists of four (4) registers: I/O Control register, Data register, Interrupt Control register and Interrupt Status register. Table 8-2 below summarizes the port address configuration of each register.

**Table 8-2. The List of Register Configurations**

| Name | Abbr. | R/W | Initial Value | Address | Register Size | Access Size |
|---|---|---|---|---|---|---|
| Port A Control Register | GPACR | R/W | H'AAAA | H'10004000 | 16 | 16 |
| Port B Control Register | GPBCR | R/W | H'AAAA | H'10004002 | 16 | 16 |
| Port C Control Register | GPCCR | R/W | H'AAAA | H'10004004 | 16 | 16 |
| Port D Control Register | GPDCR | R/W | H'AAAA | H'10004006 | 16 | 16 |
| Port A Data Register | GPADR | R/W | H'0000 | H'10004010 | 8 | 16 |
| Port B Data Register | GPBDR | R/W | H'0000 | H'10004012 | 8 | 16 |
| Port C Data Register | GPCDR | R/W | H'0000 | H'10004014 | 8 | 16 |
| Port D Data Register | GPDDR | R/W | H'0000 | H'10004016 | 8 | 16 |
| Port A Interrupt Control Register | GPAICR | R/W | H'0000 | H'10004020 | 8 | 16 |

**Table 8-2. The List of Register Configurations (cont'd)**

| Name | Abbr. | R/W | Initial Value | Address | Register Size | Access Size |
|---|---|---|---|---|---|---|
| Port B Interrupt Control Register | GPBICR | R/W | H'0000 | H'10004022 | 8 | 16 |
| Port C Interrupt Control Register | GPCICR | R/W | H'0000 | H'10004024 | 8 | 16 |
| Port D Interrupt Control Register | GPDICR | R/W | H'0000 | H'10004026 | 8 | 16 |
| Port A Interrupt Status Register | GPAISR | R | H'0000 | H'10004040 | 8 | 16 |
| Port B Interrupt Status Register | GPBISR | R | H'0000 | H'10004042 | 8 | 16 |
| Port C Interrupt Status Register | GPCISR | R | H'0000 | H'10004044 | 8 | 16 |
| Port D Interrupt Status Register | GPDISR | R | H'0000 | H'10004046 | 8 | 16 |

### 8.3 Register Descriptions

Ports A-D are 8-bit input/output ports with the pin configuration shown in Figure 8-1 below. Each pin contains an input pull-up MOS, which is controlled by I/O Control Registers (GPACR - GPDCR). The Function 2 of each I/O port pin in PFC (Refer to Table 8-1.on page 109) can be selected by system Configuration Register described on pages 119 and 120.

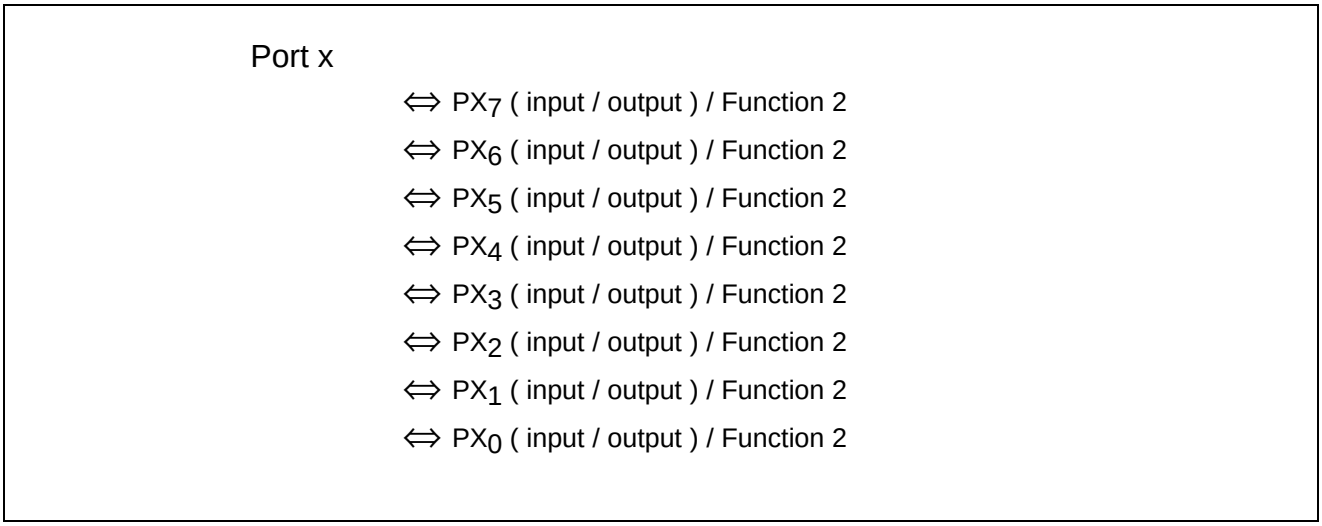



**Figure 8-1. Pin Configuration of Ports A-D**

### 8.3.1 Port x (A to D) Data Register (GPADR to GPDDR)

**Address: 110004010h, 10004012h, 10004014h, 10004016h**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | Px7DT | Px6DT | Px5DT | Px4DT | Px3DT | Px2DT | Px1DT | Px0DT |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Port x (A to D) Data register **(GPADR to GPDDR)** is an 8-bit readable/writable register, and stores data for pins **Px7 ~ Px0 (x: A to D). Px7DT ~ Px0DT** bits correspond to **Px7 ~ Px0** pins. When the pin function is general output port, the value of the corresponding **PxDR** bit is directly returned if the port is read. When the function is general input port, the corresponding pin level is read if the port is read. **Table 8-3** below shows the function of **PxDR**.

**Table 8-3. READ/WRITE Operation of the Port x (A to D) Data Register (GPADR to GPDDR)**

| PxnMD1 | PxnMD0 | Pin Status | READ | WRITE |
|---|---|---|---|---|
| 0 | 0 | Function 2 Output | GPXDR value | Can write to GPXDR, but has no effect on pin status. |
| | 1 | Output | GPXDR value | Value written to GPXDR is output by pin. |
| 1 | 0 | Input (Pull-up MOS on) | Pin status | Can write to GPXDR, but has no effect on pin status. |
| | 1 | Input (Pull-up MOS off) | Pin status | Can write to GPXDR, but has no effect on pin status. |

### 8.3.2 Port Control Register (GPACR to GPDCR)

The register is used to control the functions of each I/O port pin. Control bits of MD0 and MD1 are defined in table 8-4 on the next page.

**Address: 10004000h, 10004002h, 10004004h, 10004006h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PX7MD1 | PX7MD0 | PX6MD1 | PX6MD0 | PX5MD1 | PX5MD0 | PX4MD1 | PX4MD0 |
| Initial Value | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PX3MD1 | PX3MD0 | PX2MD1 | PX2MD0 | PX1MD1 | PX1MD0 | PX0MD1 | PX0MD0 |
| Initial Value | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

* X is A or B or C or D.

**Table 8-4. The Definitions of Control Bits**

| PxnMD1 | PxnMD0 | Pin Status | READ | WRITE |
|---|---|---|---|---|
| 0 | 0 | Function 2 Output | GPXDR value | Can write to GPXDR, but has no effect on pin status. |
| | 1 | Output | GPXDR value | Value written to Data register is output. |
| 1 | 0 | Input (Pull-up MOS on) | Pin status | Can write to Data register, but dose not affect on pin status. |
| | 1 | Input (Pull-up MOS off) | Pin status | Can write to Data register, but dose not affect on pin status. |

* X is A or B or C or D.

### 8.3.3 Port Interrupt Control Register (GPAICR - GPDICR)

This register is used to control each GPIO pin to generate the interrupt output or not when an interrupt event (low) is triggered at each I/O port pin. An interrupt is generated when an interrupt event is triggered and its corresponding register bit is set to "1." An Interrupt event will not be generated when its corresponding control register bit is "0."

**Address: 10004020h, 10004022h, 10004024h, 10004026h**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PX7ICR | PX6ICR | PX5ICR | PX4ICR | PX3ICR | PX2ICR | PX1ICR | PX0ICR |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

* X is A or B or C or D.

### 8.3.4 Port Interrupt Status Register (GPAISR - GPDISR)

**Address: 10004040h, 10004042h, 10004044h, 10004046h**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PX7ISR | PX6ISR | PX5ISR | PX4ISR | PX3ISR | PX2ISR | PX1ISR | PX0ISR |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |

* X is A or B or C or D.

When an interrupt event occurs at an I/O port pin (going low) and its corresponding interrupt control register (GPXICR) bit is set to "1" (enable), the corresponding interrupt status bit is read as "1". As the interrupt event is deasserted (going high), the interrupt status bit is read as "0."

# 9. Interrupt Controller (INTC)

## 9.1 Overview

The Intelligent Peripheral Controller interrupts are issued from the modules of PCMCIA, AFE, GPIO port, Timer, IrDA and UART. The controller contains a register for the interrupt request status issued from each module.

After SH7709 detects the interrupt, it reads the interrupt request register to see which module generates the interrupt, and then reads the interrupt request register in each module. As the controller provides the feature of gathering interrupts from all modules into one register, it will help to simplify the CPU interrupt processing of the PDA/HPC product.

### 9.1.1 Features

- All interrupts issued from the internal modules are gathered into one register.
- Only one external interrupt output pin is used for SH7709 External interrupt input.
- Interrupt request lines from each module are high active and level trigger signals
- The priority order of interrupt request lines is determined by software.
- Each module provides an interrupt mask bit. A mask register, which is able to perform masking for each module interrupt, is also included.

### 9.1.2 Block Diagram

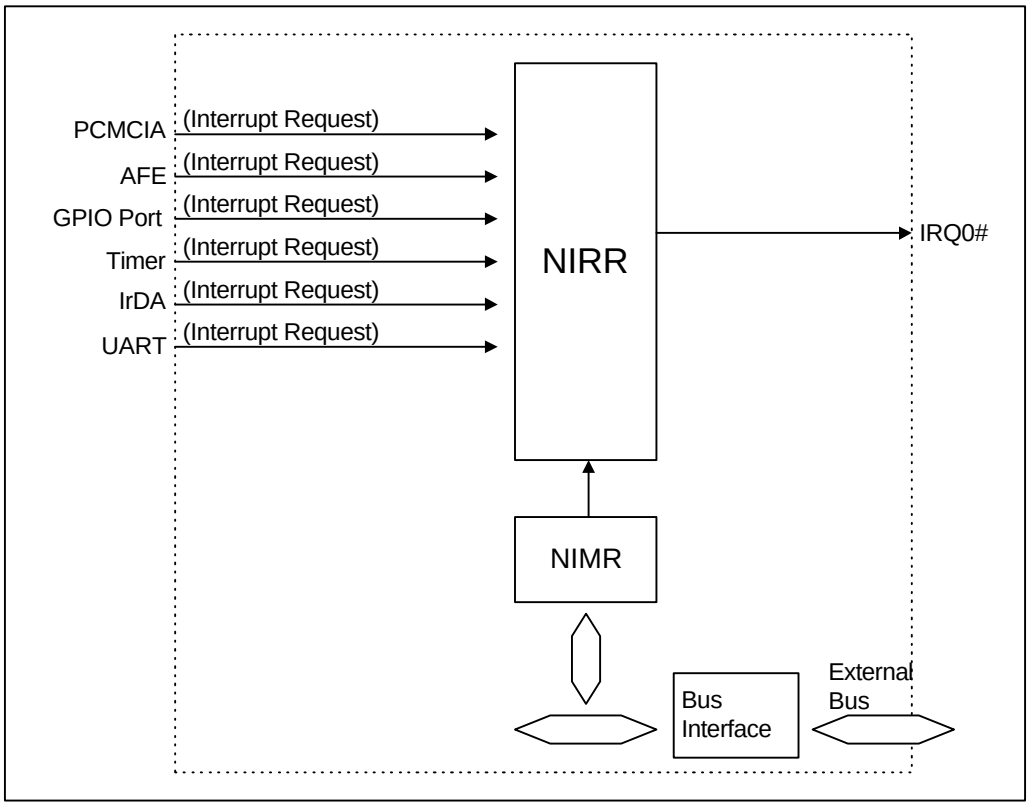



**Figure 9-1. Block Diagram of the Interrupt Controller**

### 9.1.3 Pin Configuration

| Name | Abbr. | I/O | Description |
|---|---|---|---|
| IRQ output | IRQ0# | O | Interrupt output to SH7709 from the Intelligent Peripheral Controller |

### 9.1.4 Register Configuration

The INTC includes two (2) registers listed below:

| Name | Abbr. | R/W | Initial Value | Address | Access Size |
|---|---|---|---|---|---|
| Interrupt Request register | NIRR | R | - | H'10005000 | 16 |
| Interrupt Mask register | NIMR | R/W | H'0000 | H'10005002 | 16 |

## 9.2 Interrupt Sources

### 9.2.1 On-Chip Module Interrupt

Interrupt sources are derived from on-chip peripheral module Interrupts. Each interrupt provides a mask bit in each module listed below:

- PCMCIA Controller (PCC)
- Analog Front End (AFE) Interface
- GPIO
- Timer
- IrDA
- UART
- Miniature

### 9.2.2 Interrupt Exception Processing and Priority

The priority order of the on-chip module is decided by software. After detecting interrupt requests from the Intelligent Peripheral Controller, the CPU must read the NIRR (Interrupt Request Register) to check the interrupt sources. The interrupt sources will be recorded by the CPU. The CPU will then determine the priority order and execute the interrupt service based on the determined priority order. That is to say, the interrupt service will be executed for the interrupt requests in the order from the highest priority to the lowest.

After the highest priority interrupt service is decided by the CPU, the CPU will set mask bit of NIMR (Interrupt Mask Register) to those lower priority interrupts and set CPU's priority level to the current serviced one.

One exception is that the CPU can still accept an incoming interrupt, which has higher priority than the one being serviced. After the CPU completes reading the interrupt request register in each module, the status of interrupt request for each module is cleared automatically, or by software.

### 9.3 NIRR: Interrupt Request Register

The NIRR, a 16-bit register, indicates interrupt requests from the internal modules of PCMCIA, AFE, GPIO, Timer, IrDA and UART.

**Address: 10005000h**

| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | **reserved** | PCC0R | PCC1R | AFER | GPIOR | TMU0R | TMU1R | **reserved** |
| **Initial Value** | - | - | - | - | - | - | - | - |
| **R/W** | **R** | **R** | **R** | **R** | **R** | **R** | **R** | **R** |

| **Bit** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | **reserved** | IrDAR | UARTR | reserved | reserved | reserved | reserved | reserved |
| **Initial Value** | - | - | - | 0 | 0 | 0 | 0 | 0 |
| **R/W** | **R** | **R** | **R** | **R** | **R** | **R** | **R** | **R** |

| Bit | Description | Default |
|---|---|---|
| 15 | **Reserved** | - |
| 14 | This bit represents PCMCIA0 interrupt request status.<br>1: The interrupt request is generated from PCMCIA0.<br>0: No interrupt requests are generated from PCMCIA0. | - |
| 13 | This bit represents PCMCIA1 interrupt request status.<br>1: The interrupt request is generated from PCMCIA1.<br>0: No interrupt requests are generated from PCMCIA1. | - |
| 12 | This bit represents AFE interrupt requests status.<br>1: The interrupt request is generated from AFE,<br>0: No interrupt requests are generated from AFE. | - |
| 11 | This bit represents GPIO interrupt request status.<br>1: The interrupt request is generated from GPIO.<br>0: No interrupt requests are generated from GPIO. | - |
| 10 | This bit represents timer 0 interrupt request status.<br>1: The interrupt request is generated from timer 0.<br>0: No interrupt requests are generated from timer 0. | - |
| 9 | This bit represents timer 1 interrupt request status.<br>1: The interrupt request is generated from timer 1.<br>0: No interrupt requests are generated from timer 1. | - |

**Interrupt Request Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 8 | **Reserved** | - |
| 7 | **Reserved** | - |
| 6 | This bit represents IrDA interrupt request status.<br>1: The interrupt request is generated from IrDA.<br>0: No interrupt requests are generated from IrDA. | - |
| 5 | This bit represents UART interrupt request status.<br>1: The interrupt request is generated from UART.<br>0: No interrupt requests are generated from UART. | - |
| 4~0 | Reserved | - |

### 9.4 NIMR: Interrupt Mask Register

The NIMR, a 16-bit register, serves to mask interrupt requests from the internal modules of PCMCIA, AFE, GPIO, Timer, IrDA, and UART. This register is initialized to H'0000 at power-on RESET.

**Address: 10005002h**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | reserved | PCC0M | PCC1M | AFEM | GPIOM | TMU0M | TMU1M | Reserved |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | Reserved | IRDAM | UARTM | reserved | reserved | reserved | reserved | reserved |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 | Reserved | - |

**NIMR: Interrupt Mask Register (cont'd)**

| Bit | Description | Default |
|---|---|---|
| 14 | This bit is used to control the mask option for PCMCIA0 interrupt request.<br>1: The interrupt request from PCMCIA0 is masked.<br>0: The interrupt request from PCMCIA0 is not masked. | 0 |
| 13 | This bit is used to control the mask option for PCMCIA1 interrupt request.<br>1: The interrupt request from PCMCIA1 is masked.<br>0: The interrupt request from PCMCIA1 is not masked. | 0 |
| 12 | This bit is used to control the mask option for AFE interrupt request.<br>1: The interrupt request from AFE is masked.<br>0: The interrupt request from AFE is not masked. | 0 |
| 11 | This bit is used to control the mask option for GPIO interrupt request.<br>1: The interrupt request from GPIO is masked.<br>0: The interrupt request from GPIO is not masked. | 0 |
| 10 | This bit is used to control the mask option for timer 0 interrupt request.<br>1: The interrupt request from timer 0 is masked.<br>0: The interrupt request from timer 0 is not masked. | 0 |
| 9 | This bit is used to control the mask option for timer 1 interrupt request.<br>1: The interrupt request from timer 1 is masked.<br>0: The interrupt request from timer 1 is not masked. | 0 |
| 8 | Reserved | - |
| 7 | Reserved | - |
| 6 | This bit is used to control the mask option for IrDA interrupt request.<br>1: The interrupt request from IrDA is masked.<br>0: The interrupt request from IrDA is not masked. | 0 |
| 5 | This bit is used to control the mask option for UART interrupt request.<br>1: The interrupt request from UART is masked.<br>0: The interrupt request from UART is not masked. | 0 |
| 4~0 | Reserved | - |

### 9.5 Power-on RESET Requirement

The power-on RESET requirement is the same as that of the interface with SH7709.

### 9.6 Special Register Programming Sequence

The special register programming sequence is not required. However, the CPU supports the priority programming control to handle the protocol.

## 10. Standby Mode and System Configuration

Each module in the Intelligent Peripheral Controller is provided with the STANDBY mode. All peripheral module functions are halted in the STANDBY mode; thereby reducing the power consumption.

The System Configuration registers determines the functions of multifunction pins.

**System Configuration Register and STANDBY mode**

**Standby Control Register (STBCR)**

**Address: H'10000000, Access Size: 16 bits**

| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | - | - | CKIO_ STBY | SAFECKE _IST | SLCKE_ IST | SAFECKE _ OST | SLCKE_ OST | SMIAST |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| **Bit** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | SLCDST | SPC0ST | SPC1ST | SAFEST | STM0ST | STM1ST | SIrST | SURTSD |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| **Bit** | **Description** | **Default** |
|---|---|---|
| 15 ~ 14 | Reserved (The READ value is always 0.) | 0 |
| 13 | CKIO input gating (when all modules are at standby mode, address 10000000h bits 12, 11and 8 - 0 are set to one.)<br>1: **CKIO is gated (fix high for internal module)**<br>0: **Normal operation** | 0 |
| 12 | Stops AFECKE input clock (SAFECKE_IST) **for AFE module**<br>1: **AFECKE input is gated**<br>0: **Normal operation** | 0 |
| 11 | Stops LCKE input clock (SLCKE_IST) **for LCDC module**<br>1: **LCKE input is gated**<br>0: **Normal operation** | 0 |
| 10 | **Stops AFECK oscillation (SAFECKE_OST)**<br>1: **AFECKE oscillation stop**<br>0: **AFECKE oscillation run** | 0 |
| 9 | **Stops LCKE oscillation (SLCKE_OST)**<br>1: **LCKE oscillation stop**<br>0: **LCKE oscillation run** | 0 |

**Standby Control Register (STBCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 8 | Standby Miniature Card I/F (SMIAST) *<br>1: Clock supply to Miniature Card I/F halted<br>0: Miniature Card I/F runs (initial value) | 0 |
| 7 | Standby LCD Controller (SLCDST)<br>1: Clock supply to LCD Controller halted<br>0: LCD Controller runs (initial value) | 0 |
| 6 | Standby PCMCIA I/F channel 0 (SPC0ST)<br>1: Clock supply to PCMCIA I/F channel 0 halted<br>0: PCMCIA I/F channel 0 runs (initial value) | 0 |
| 5 | Standby PCMCIA I/F channel 1 (SPC1ST)<br>1: Clock supply to PCMCIA I/F channel 1 halted<br>0: PCMCIA I/F channel 1 runs (initial value) | 0 |
| 4 | Standby AFE I/F (SAFEST)<br>1: Clock supply to AFE I/F halted<br>0: AFE I/F runs (initial value) | 0 |
| 3 | Standby Timer 0 (STM0ST)<br>1: Clock supply to Timer 0 halted<br>0: Timer 0 runs (initial value) | 0 |
| 2 | Standby Timer 1 (STM1ST).<br>1: Clock supply to Timer 1 halted<br>0: Timer 1 runs (initial value) | 0 |
| 1 | Standby IrDA Controller (SIrST)<br>1: Clock supply to IrDA Controller halted<br>0: IrDA Controller runs (initial value) | 0 |
| 0 | Standby UART communication module (SURTST)<br>1: Clock supply to UART communication module halted<br>0: UART communication module runs (initial value) | 0 |

* Do not support. Please set, if reduce power consumption.

**System Configuration Register (SYSCR)**

**Address: H'10000002, Access Size: 16 bits**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | **-** | **-** | SCPU_ BUS_IGAT | - | - | **-** | - | - |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**System Configuration Register (SYSCR) [cont'd]**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | SPTA_Ir | SPTA_TM | SPTB_UR | WAIT_CTL_sel | - | - | SMODE1 | SMODE0 |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/O | R/O |

| Bit | Description | Default |
|---|---|---|
| 15 ~ 14 | Reserved | 0 |
| 13 | CPU bus input gating control(SCPU_BUS_IGAT) (A25-A0, RE_, WE0_, WE1_, RDWR)<br>1 - enable(gating)<br>0 – disable **(Normal operation)** | 0 |
| 12 ~ 8 | **Reserved** | 0 |
| 7 | GPIO Port A[7:4] or IrDA function select (SPTA_Ir)<br>1: IrDA<br>0: GPIO Port A[7:4] (initial value) | 0 |
| 6 | GPIO Port A[3:2], or Timer output 1, 0 function select (**SPTA_TM**)<br>For mode00, mode 10<br>1: Timer output 1, 0<br>0: GPIO Port A[3:2] (initial value) | 0 |
| 5 | GPIO Port B or UART function select (SPTB_UR)<br>1: UART<br>0: GPIO Port B (initial value) | 0 |
| 4 | WAIT_ output enable control select (WAIT_CTL_sel)<br>1: **WAIT_ output only when Access space is defined in this spec.**<br>0: **WAIT_ output when Area 4 is select** | 0 |

**System Configuration Register (SYSCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 3 ~ 2 | Reserved. (read value always zero) | 0 |
| 1 ~ 0 | System Configuration Mode select (SMODE1, SMODE0)<br>**11: Reserved**<br>10: PCMCIA 0 with the external address / data buffer<br>Port A[7:4] / IrDA<br>Port A[3:2] / Timer 1, 0<br>Port A[1:0]<br>Port B / UART<br>Port C<br>Port D<br>AFE Interface<br>**LCDC with CRT**<br>01: **Reserved**<br>00: PCMCIA 0 with the external address / data buffer<br>PCMCIA 1 with the external address / data buffer<br>Port A[7:4] / IrDA<br>Port A[ 3:2] / Timer 1, 0<br>Port A[1:0]<br>Port B / UART<br>AFE Interface<br>LCDC with CRT | by pin |

*** Do not select UART and IrDA at the same time.**

**CPU Data Bus Control Register (SCPUCR)**

**Address: H'10000004, Access Size 16 bits**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | SPDSTOF | SPDSTIG | SPCSTOF | SPCSTIG | SPBSTOF | SPBSTIG | SPASTOF | SPASTIG |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**CPU Data Bus Control Register (SCPUCR) [cont'd]**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Bit Name** | SLCDSTIG | SCPU_CS56_EP | SCPU_CMD_EP | SCPU_ADDR_EP | SCPDPU | - | - | SCPU_A2319_EP |
| **Initial Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **R/W** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Description | Default |
|---|---|---|
| 15 | IO Port D Output Floating Control<br>0 - disable<br>1 - enable(floating) | 0 |
| 14 | IO Port D Input Gating Control<br>0 - disable<br>1 - enable(gating) | 0 |
| 13 | IO Port C Output Floating Control<br>0 - disable<br>1 - enable(floating) | 0 |
| 12 | IO Port C Input Gating Control<br>0 - disable<br>1 - enable(gating) | 0 |
| 11 | IO Port B Output Floating Control<br>0 - disable<br>1 - enable(floating) | 0 |
| 10 | IO Port B Input Gating Control<br>0 - disable<br>1 - enable(gating) | 0 |
| 9 | IO Port A Output Floating Control<br>0 - disable<br>1 - enable(floating) | 0 |
| 8 | IO Port A Input Gating Control<br>0 - disable<br>1 - enable(gating) | 0 |
| 7 | LCDC IO Input Gating on Standby Mode(SLCDSTIG)<br>0 - disable<br>1 - enable(gating) | 0 |
| 6 | CPU CS4_, CE1A_, CE2A_, CE1B_, CE2B_ Pull-up Control (SCPU_CS456_EP)<br>0 - enable(pull-up)<br>1 - disable | 0 |

**CPU Data Bus Control Register (SCPUCR) [cont'd]**

| Bit | Description | Default |
|---|---|---|
| 5 | CPU Command/Status Pull-up Control (SCPU_CMD_EP) (RD_, WE0_, WE1_, REWR_, A25, A24, ICIORD_, ICIOWR_)<br>0 - enable(pull-up)<br>1 - disable | 0 |
| 4 | CPU Address Bus **(A25, A24, A18-A0)** Pull-up Control (SCPU_ADDR_EP)<br>0 - enable(pull-up)<br>1 - disable | 0 |
| 3 | CPU data bus internal pull-up resister control<br>1: Internal pull-up resister enable<br>0: Internal pull-up resister disable | 0 |
| 2 ~ 1 | Reserved | 00 |
| 0 | CPU Address 23-19 Pull-up Control (SCPU_A2319_EP)<br>0 - disable<br>1 - enable(pull-up) | 0 |