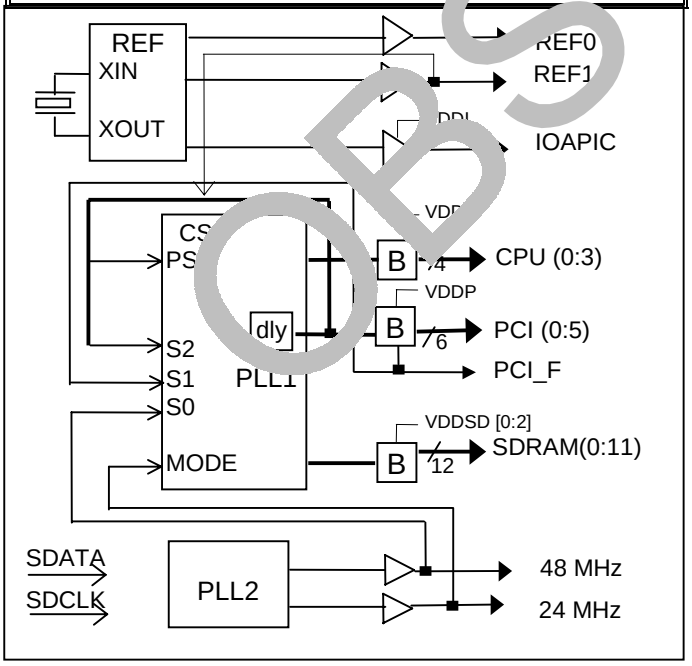
I²C Clock Generator for 3 DIMM, Pentium®, Pentium® II & Pro Boards.

Approved Product

PRODUCT FEATURES

- Supports Pentium®,Pentium® II, M2, & K6 CPUs.
- Designed to the 440LX specification
- Supports Synchronous and Asynchronous PCI.
- 4 CPU / AGP clocks
- Up to 12 SDRAM clocks for 3 DIMMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
  (VDD = VDDC = VDDP = VDDSD = VDDI = 3.3V)
  or (VDD = VDDC = VDDSD = VDDP = 3.3V, VDDI = VDDC = 2.5)
- < 250 pS skew among CPU or SDRAM clocks.
- < 250 pS skew among PCI clocks.
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - Jumperless frequency selection
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- Power Management Capability.
- IOAPIC clocks for multiprocessor support.
- 48 MHz for USB support
- Internal Crystal Load Capacitors.
- 48-pin SSOP package
- **Spread Spectrum Technology for EMI reduction**

BLOCK DIAGRAM

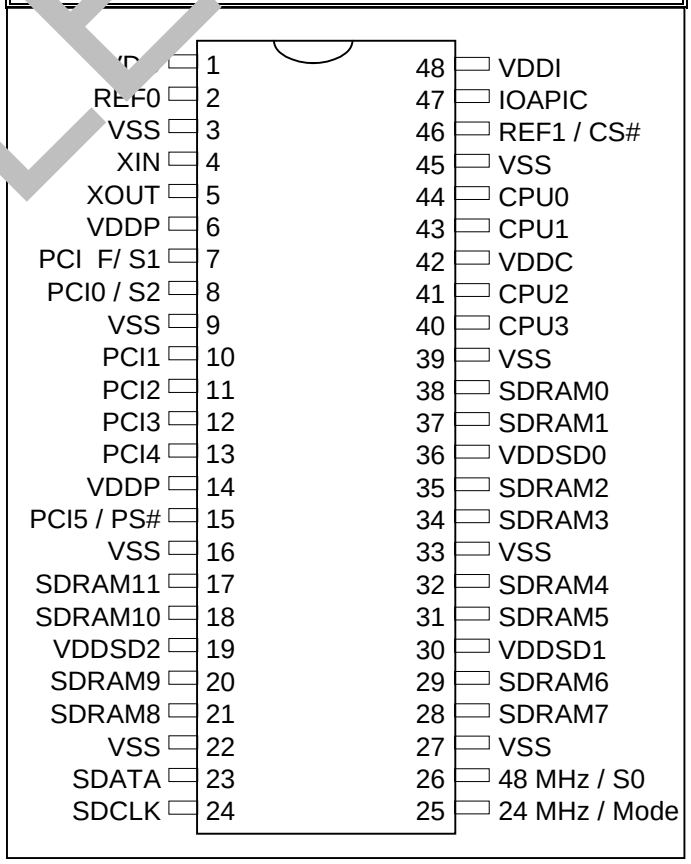


FREQUENCY TABLE (MHz)

S2	S1	S0	CPU	PCI
0	0	0	50.11	25.06
0	0	1	75.17	30.07
0	1	0	83.52	41.76
0	1	1	69.80	34.90
1	0	0	100.23	33.41
1	0	1	75.17	37.59
1	1	0	60.14	30.07
1	1	1	66.82*	33.41*

* Supports spread spectrum

CONNECTION DIAGRAM



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PIN DESCRIPTION

Pin Number	Pin Name	PWR	I/O	Description
4	**Xin**	VDD	I	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal. If the external input is used, Pin 5 is left unconnected.
5	**Xout**	VDD	O	
7	**PCI_F**	VDDP	O	This is a bi-directional pin. During power up, this pin is an input for frequency selection S1 control bit (see page 1, and app note on page 12) and sets the bit to its initial state. After a fixed period of time (see fig.1, page 3), this pin becomes a low skew PCI clock output that **does not** stop when PS# (pin 15 or I²C register bit) is asserted.
	S1	VDD	I *	
8	**PCI0**	VDDP	O	This is a bi-directional pin. During power up, this pin is an input for frequency selection S2 control bit (see page1,and app note on page 12) and sets the bit to its initial state. After a fixed period of time (see fig.1, page 3), this pin becomes a low skew PCI clock output that stops when PS# (pin 15 or its I²C register bit) is asserted.
	S2	VDD	I *	
10, 11, 12, 13	**PCI (1:4)**	VDDP	O	Low skew (<250 pS) clock outputs for PCI frequencies.
15	**PCI5**	VDDP	O	IF MODE=1 this pin becomes low skew (<250 pS) clock outputs for PCI frequencies.
	PS#	VDD	I *	If MODE=0 this pin controls whether the PCI clock outputs (except for PCI-F) are enabled (set to a logic 1) or disabled (set to a logic 0)
44, 43, 41, 40	**CPU(0:3)**	VDDC	O	Low skew (<250 pS) clock outputs for host frequencies such as CPU, MP, Chipset, Cache.
38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17	**SDRAM(0:11)**	VDDSD(0:2)	O	Synchronous DRAM DIM clocks.
47	**IOAPIC**	VDDI	O	Buffered copy of the crystal oscillator (nominally 14.31818 MHz).
46	**REF1**	VDD	O	IF MODE=1 this pin becomes a buffered copy of the internal crystal oscillator (nominally 14.31818 MHz)
	CS#	VDD	I	If MODE=0 then this pin controls whether the CPU clock outputs are enabled (set to a logic 1) or disabled (set to a logic 0).
2	**REF0**	VDD	O	This pin is a Buffered output of the crystal reference frequency.
26	**48 MHz**	VDD	I/O	This is a bi-directional pin. During power up, this pin is an input for frequency selection S0 control bit (see page1,and app note on page 12) and sets the bit to its initial state. After a fixed period of time (see fig.1, page 3), this pin becomes a 48 MHz frequency clock.
	S0	VDD	I *	
25	**24 MHz**	VDD	O	This is a bi-directional pin. During power up, this pin is an input that enables (0) or disables (1) the power management shared pins (46 and 15) (see app note on page 12) and sets the bit to its initial state. After a fixed period of time (see fig.1, page 3), this pin becomes a 24 MHz frequency clock.
	MODE	VDD	I *	

*A 10K ohm resistor to VDD or VSS is required to insure that the device's internal storage registers are correctly set at power up.

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PIN DESCRIPTION (Cont.)

Pin Number	Pin Name	PWR	I/O	Description
23	**SDATA**	VDD	I	Serial Data for I²C 2-wire control interface. Has internal pull-up.
24	**SDCLK**	VDD	I	Serial Clock of I²C 2-wire control interface. Has internal pull-up.
3, 9, 16, 22, 27, 33, 39, 45	**VSS**	-	P	Ground pins for the chip.
1	**VDD**	-	P	Power supply pins for analog circuit, core logic and reference clock buffers.
48	**VDDI**	-	P	Power supply pin for IOAPIC clock. May be either 3.3 or 2.5 Volts.
6, 14	**VDDP**	-	P	3.3 volt power for PCI clocks.
36, 30, 19	**VDDSD [0:2]**	-	P	3.3 volt power for SDRAM clocks
42	**VDDC**	-	P	Power supply pin for CPU clocks may be either 2.5 V or 3.3V

A bypass capacitor (0.1µF) should be placed as close as possible to each VDD, VDDSD, VDDI, and VDDP pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be canceled by the lead inductances of the traces.

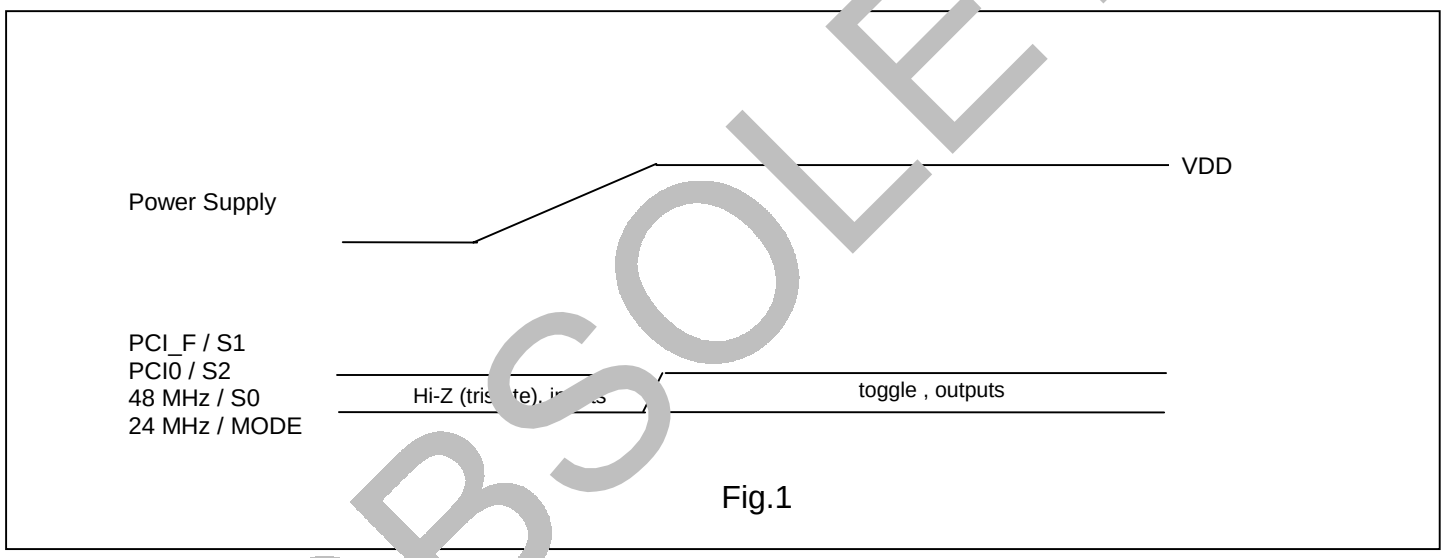

Fig.1

POWER MANAGEMENT FUNCTIONS

When MODE=0, pins 15 and 46 are inputs PS# (PCI_STOP#), and CS# (CPU_STOP#), respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The IMISG543 clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU/AGP and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPU	PCI	OTHER CLKs	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING

Please note that all clocks can be individually asynchronously enabled or stopped via the 2-wire I2C control interface. In this case all clocks are stopped in the low state.

POWER MANAGEMENT TIMING

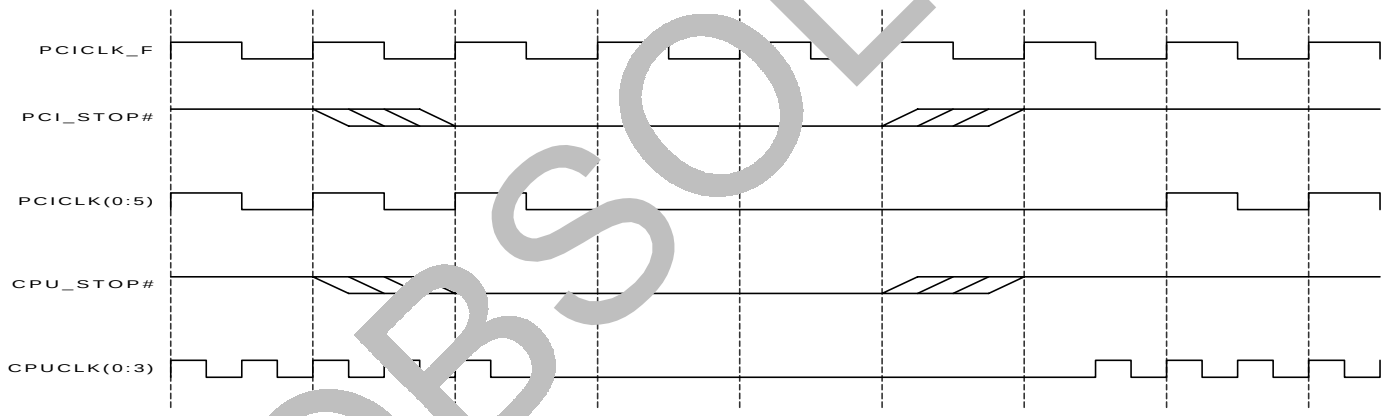

Fig. 2

2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISG543 cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The IMISG543 will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The IMISG543 will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7		*	Reserved
6	1		S2 (for frequency table selection by software via I2C)
5	1	*	S1 (for frequency table selection by software via I2C)
4	1	*	S0 (for frequency table selection by software via I2C)
3	0	*	enables freq. selection by hardware (set to 0) or software I²C (set to 1)
2	1	*	Reserved
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Spread-On Normal Operation 0 1 Test Mode 0 0 Spread-Off Normal Operation

SERIAL CONTROL REGISTERS (Cont.)

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Normal	see table	see table	CPU	14.318	14.318
Test Mode[1]	TCLK/2	TCLK/4	TCLK/2	TCLK	TCLK

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	48 MHz enable/Stopped
6	1	25	24 MHz enable/Stopped
5	1	-	0 = Reserved for IMI TEST. 1 = Normal operation.
4	x	-	Reserved
3	1	40	CPUCLK3 enable/Stopped
2	1	41	CPUCLK2 enable/Stopped
1	1	43	CPUCLK1 enable/Stopped
0	1	44	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	17	PCI_F enable/Stopped
5	1	15	PCI5 enable/Stopped
4	1	13	PCI4 enable/Stopped
3	1	12	PCI3 enable/Stopped
2	1	11	PCI2 enable/Stopped
1	1	10	PCI1 enable/Stopped
0	1	8	PCI0 enable/Stopped

SERIAL CONTROL REGISTERS (Cont.)

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28	SDRAM7 enable/Stopped
6	1	29	SDRAM6 enable/Stopped
5	1	31	SDRAM5 enable/Stopped
4	1	32	SDRAM4 enable/Stopped
3	1	34	SDRAM3 enable/Stopped
2	1	35	SDRAM2 enable/Stopped
1	1	37	SDRAM1 enable/Stopped
0	1	38	SDRAM0 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM11 enable/Stopped
2	1	18	SDRAM10 enable/Stopped
1	1	20	SDRAM9 enable/Stopped
0	1	21	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	47	IOAPIC enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	46	REF1 / CS# enable/Stopped
0	1	2	REF0 enable/Stopped

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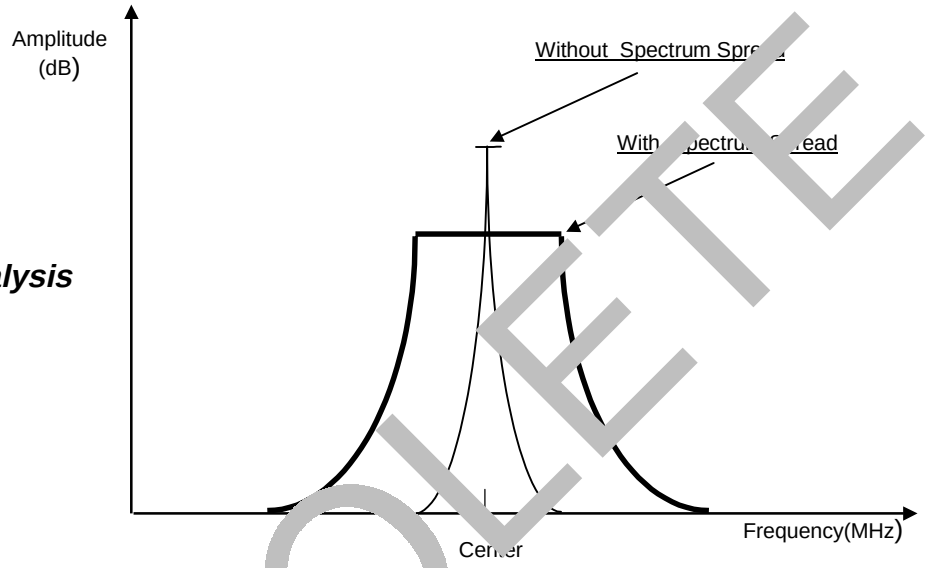
SPREAD SPECTRUM CLOCKING



Spectrum Analysis

SPECTRUM SPREADING SELECTION TABLE

Min (MHz)	Center (MHz)	Max (MHz)	CPU Frequency	% of Frequency Spreading	Mode
65.98	66.8	67.66	66 MHz	-/+ 1.25%	Center

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	220	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	35	mA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	tSKEW1	-		±250	pS	15 pf Load Measured at 1.5V
Skew (CPU-SDRAM)	tSKEW2	-	-	±500	pS	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	pS	-
Jitter Spectrum 20 dB Bandwidth from Center				500	KHz	
Overshoot/Undershoot Beyond Power Rails	V_{ove}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	note1
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

note 1: Ring Back must not enter this range.

JITTER CHARACTERISTICS		
Device	***Maximum***	***Conditions***
CPU, SDRAM	250 pS	15 pF
PCI	500 pS	30 pF

TB40AX_V TYPE BUFFER CHARACTERISTICS FOR CPU (0:3)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	22	-	31	mA	Vout = VDD -.5V
Pull-Up Current Max	IOH_{max}	37	-	56	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	30	-	41	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	109	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB40AX TYPE BUFFER CHARACTERISTICS FOR REF0 and SDRAM(0:11)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	39	-	39	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	30	-	40	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	103	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4	TRF_{max}		-	1.3	nS	30 pF Load
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

BT4LP112C TYPE BUFFER CHARACTERISTICS FOR PCICLK(0:5,F) AND REF1						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

TB4L1_V TYPE BUFFER CHARACTERISTICS FOR IOAPIC						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	20	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}				mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	18	-	23	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}			61	mA	Vout = 1.5V
Rise/Fall Time Max Between 0.4 V and 2.4 V		0.4	-	1.6	nS	20 pF Load
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

BT5LP1 TYPE BUFFER CHARACTERISTICS FOR 24M, 48M						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	13	-	17	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	30	-	44	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	13	-	19	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	32	-	44	mA	Vout = 1.5V
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF	-	-	2.0	nS	20 pF Load
VDD = VDDP = VDDSD(0:2) =3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (0 a -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO		--	8	pF	crystals internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Typical trace capacitance, (< 1 inch) is 4 pF, Load to the crystal is therefore = 2.0 pF
Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore = 18.0 pF
the total parasitic capacitance would therefore be = 20.0 pF.

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

APPLICATION NOTE FOR SELECTION ON BIDIRECTIONAL PINS

Pins 7, 8, 25 and 26 are Power up bidirectional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig1, page4), therefore, they are considered input select pins internal to the IC, these pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5mS settling time), then it is recommended to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see FIG.3A and Fig. 3B.

Fig 3A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.3A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig 3B represents a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, jumper is placed between leads 1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

If the system power supply is fast (less than 5mS settling time), then FIG3A only applies and Pull up Rup resistor is not necessary.

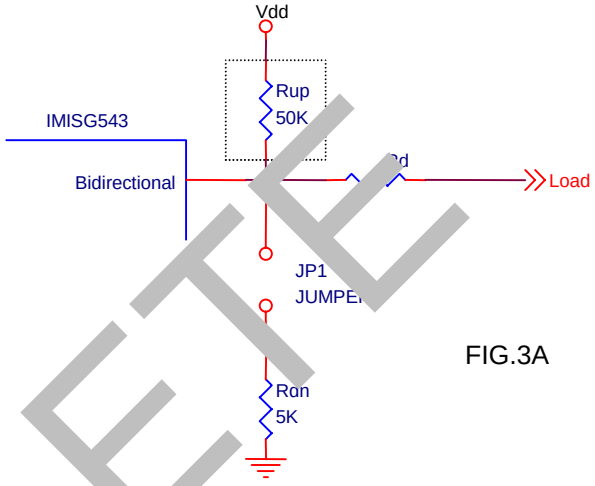

FIG.3A

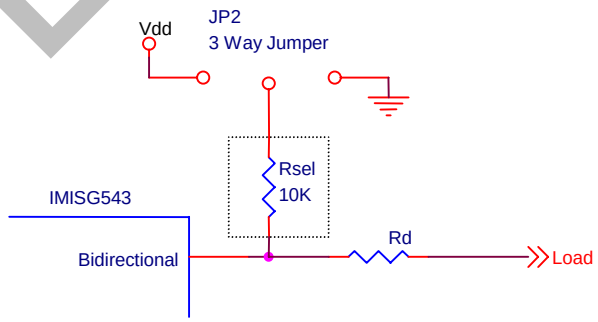

FIG.3B

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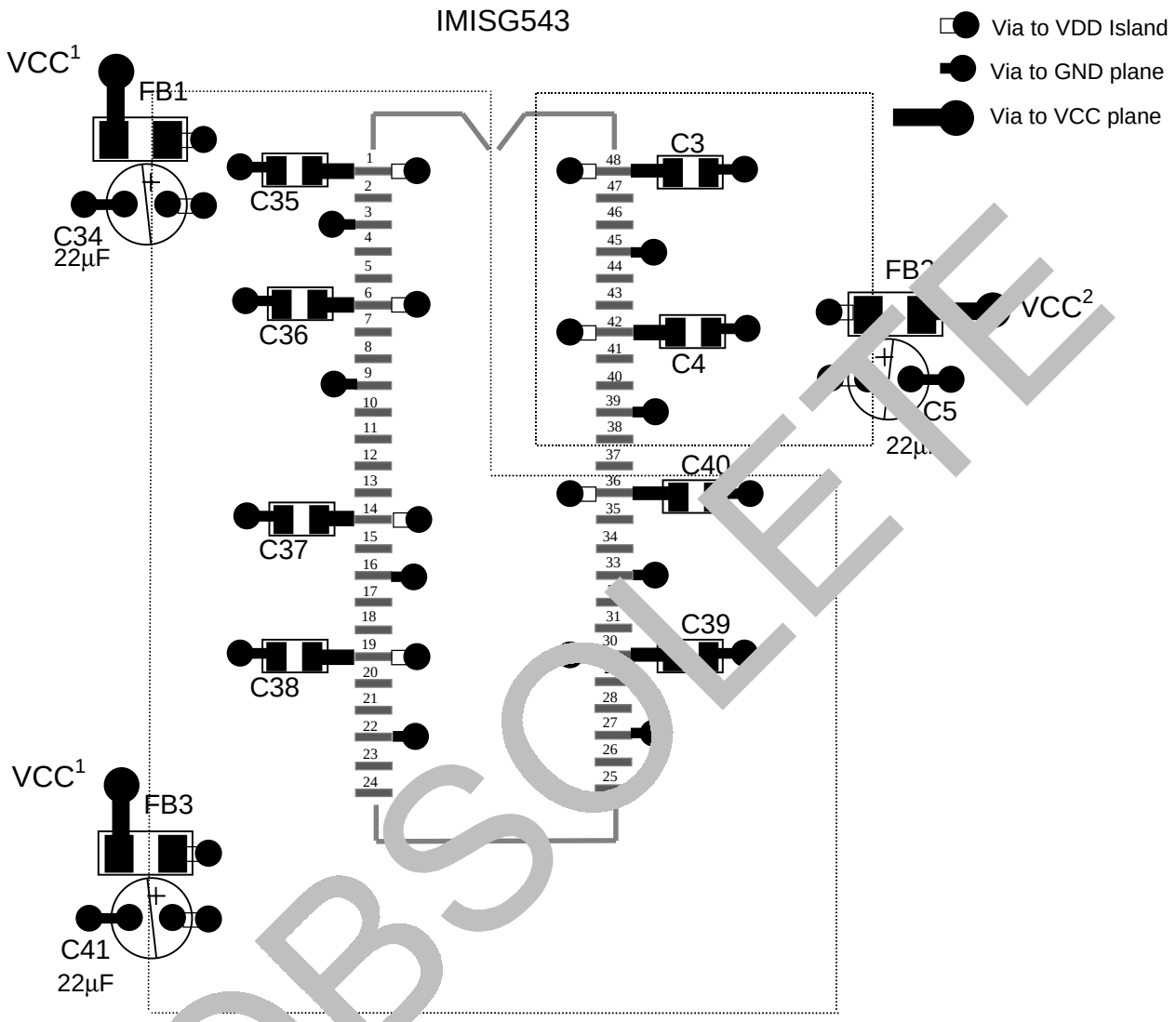
PCB LAYOUT SUGGESTION



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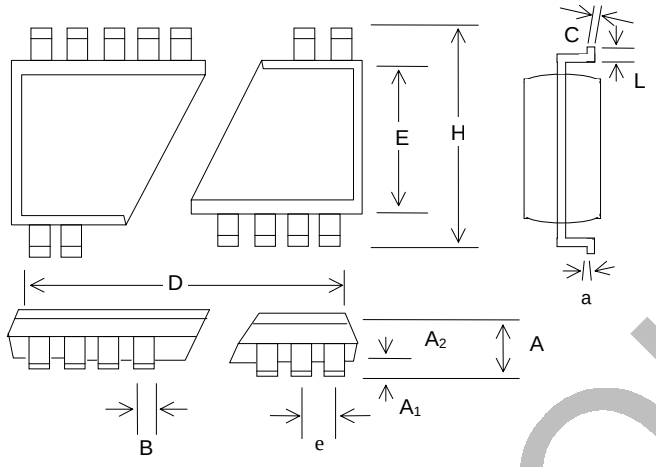
Approved Product

PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG543CYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG543CYB
Date Code, Lot #

IMISG543CYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number