

March 1996

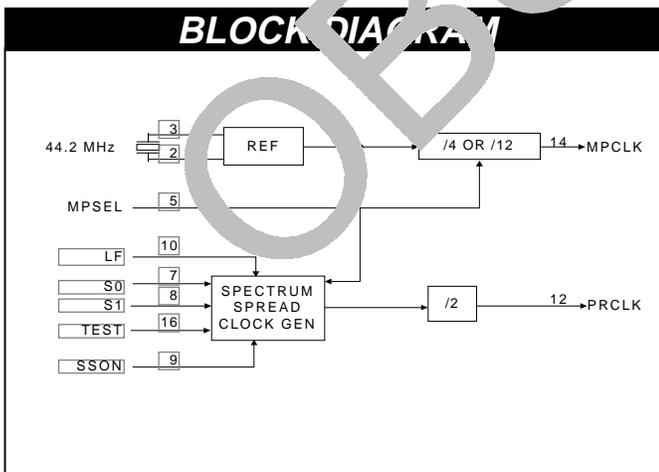
PATENT PENDING

REDUCED EMI CLOCK GENERATOR

PRODUCT FEATURES

- Generates CPU Clock Signals for Microprocessor Systems
- Reduces Measured EMI by 10 db nominal
- 4V to 7V Operating Supply Range
- Supports 80286-, 80386-, 80486-, Pentium™- and 29000-based designs
- Wide range of selectable output frequencies including 50, 25, 20 and 10 Mhz
- single, low cost crystal used as reference frequency
- Glitch-free switching
- 50% duty cycle
- Power down mode for low power consumption
- TTL or CMOS compatible outputs with 6mA drive capability
- Low, short- and long-term jitter
- 16 PDIP and 16 Pin SOIC (300 mil body) package options

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISG501 is a spectrum spread clock generator specially designed for personal computers, laser printers and other digital systems. IMISG501 uses a patent pending concept to generate popular clock frequencies that are intentionally broadbanded to reduce electromagnetic interference. IMISG501 attenuates the radiated emission amplitudes from products associated with either the clock harmonics or any signals derived from the clock signals nominally 10 db and could significantly reduce the cost of complying with the regulatory requirements.

PRCLK is the broadbanded output and can be programmed to generate 50, 25, 20 and 10 Mhz with S0 and S1 pins. A single, low cost external crystal is required as reference frequency for the synthesizer. Output modulation function can be turned off with the SSON pin. Several power down modes add the flexibility to operate the device in a completely static mode to reduce standby currents and simplify system design tests.

PDIP/SOIC CONNECTION DIAGRAM

VDD	1	16	TEST
OSCin	2	15	VDD
OSCout	3	14	MPCLK
VSS	4	13	VSS
MPSEL	5	12	PRCLK
AVDD	6	11	AVSS
S0	7	10	LF1
S1	8	9	SSON

APPLICATIONS

IMISG501 eliminates the need for multiple oscillators and generates the CPU clock signals for personal computers, laser printers and other digital systems. Supports 8086-, 80286-, 80386-, 80486-, Pentium™- and 29000-based designs. IMISG501 can be used with laptop or notebook computers to save power by running the system slower than normal CPU speeds or completely disabling the clocks in standby mode.

March 1996

REDUCED EMI CLOCK GENERATOR

PIN DESCRIPTION

OSCI_n, OSCO_ut - These pins form an on-chip reference oscillator when connected to terminals of an external 44.2 Mhz third overtone parallel resonant crystal. OSC_in may also serve as an input for an externally generated CMOS level or AC coupled reference signal.

S0, and S1 - Frequency select inputs. These inputs control the PRCLK frequency selection. S0-S1 inputs control the CPU clock frequencies. All these inputs have internal pull-downs.

Table 1 shows the output frequency selection conditions.

TEST - Controls power down and Test Mode selection. When high, S0-S1 and MPSEL controls the mode selection as shown on Table 1 and Table 2. When low, device operates in normal mode. This pin has an internal pull-down.

MPSEL - Controls MPCLK output frequency selection. Table 2 shows the selected frequencies for MPCLK. This input has an internal pull-up.

SSON - This pin controls the spectrum spread function. When low, PRCLK is modulated. When high, spectrum spread is turned off. This pin has an internal pull-up.

LF1 - This is the control output for the clock generator. It is a single-ended, tri-state output. Component connections are shown in Figure 1.

MPCLK - This is a nonmodulated output. This output can be programmed to be 3.7 Mhz or 11.06 mHz. The selection of these frequencies are controlled by the MPSEL pin shown in Table 1.

PRCLK - Output from the spectrum spread clock generator. Frequency selection is shown on Table 1. When the SSON pin is high, outputs are not modulated. When SSON is low, spectrum spread function is enabled.

VSS - Circuit ground

VDD - Positive power supply

AVSS - Analog circuit ground

AVDD - Analog positive power supply

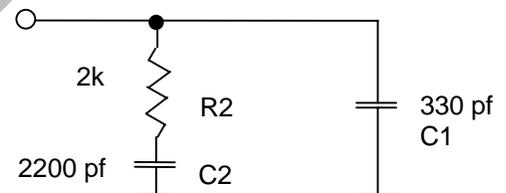


Figure 1

PRCLK FREQUENCY SELECTION			
Inputs			Output
TEST	S1	S0	PRCLK
0	0	0	9.96 Mhz
0	0	1	19.92 Mhz
0	1	0	24.9 Mhz
0	1	1	49.80 Mhz
1	0	0	0; Power Down
1	0	1	1; Power Down
1	1	0	TEST
1	1	1	Hi-Z

TABLE 1: When Power Down address is selected, the VCO is turned off and the device goes to standby mode. Phase detector is in tri-state mode.

MPCLK FREQUENCY SELECTION				
Inputs				Output
TEST	MPSEL	S1	S0	PRCLK
0	0	X	X	3.7 Mhz
0	1	X	X	11.06 MHz
1	X	0	0	0; Power Down
1	X	0	1	1; Power Down
1	X	1	0	TEST
1	X	1	1	Hi-Z

TABLE 2: When Power Down address is selected, the VCO is turned off and the device goes to standby mode. Phase detector is in tri-state mode.

March 1996

REDUCED EMI CLOCK GENERATOR

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65°C to 150°C
Ambient Temperature:	-0°C to 70°C
Recommend Operating Range:	4.5-5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$V_{SS} \leq (V_{in} \text{ or } V_{out}) < V_{DD}$$

All inputs are tied high or low internally.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	-	-	0.8	Vdc
Input High Voltage	V_{IH}	2.0	-	-	Vdc
Input Low Current with Pull-up/ Pull-down	I_{IL-H}	-	-	10/100	μ A
Output Low Voltage IOL = 6mA	V_{OL}	-	-	0.4	Vdc
Output High Voltage IOH=6mA	V_{OH}	2.5	-	-	Vdc
Tri-State leakage Current	I_{OZ}	-	-	10	μ A
Static Supply Current	I_{DD}	-	-	250	μ A
Dynamic Supply Current	I_{CC}	-	25	30	mA
Short Circuit Current	I_{SC}	25	-	-	mA

$V_{DD} = 5V \pm 10\%$, $T_A = 0^\circ\text{C to } 70^\circ\text{C}$

March 1996

REDUCED EMI CLOCK GENERATOR

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise and Fall Time Measured at 10% - 90% of VDD	t_{TLH}, t_{THL}	-	-	5	ns
Output Rise and Fall Time Measured at 0.8V - 2.0V	t_{TLH}, t_{THL}	-	-	3	ns
Output Duty Cycles	T_{symF1}	-	-	45/55	%
Jitter One Sigma	t_{j1s}	-	-	2	% of F_{out}
Cycle-to-Cycle Jitter with Normal Crystal	t_{jcc}	-	-	50	ps

VDD = 5V, TA = 0°C to 70°C, CL = 15 pF

OSCILLATOR CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	gm	20	80	180	Mhos	@ 44.2 Mhz
Output Impedance	Zo	-	200	800	ohms	@ 44.2 Mhz
Input Capacitance	Ci	8	13	18	pf	-
Output Capacitance	Co	5	6	7	pf	-
DC Bias Voltage	Vb	1.5	VDD	3.5	Volt	-
Start-up Time	ts	-	-	2	ms	@ VDD = 4.5V
Duty Cycle	T_{symF1}	-	-	45/55	%	-
Input Rise Time OSCin	CLKr	-	-	20	ns	-

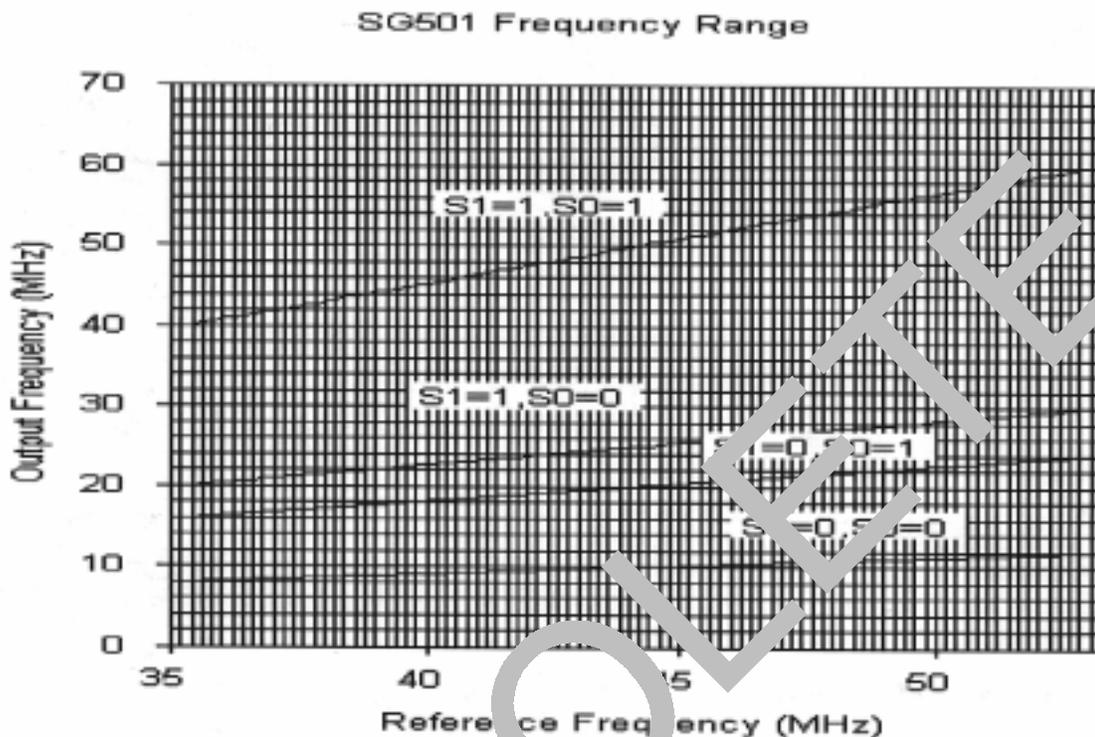
VCO CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
VCO Gain	Ko	35	55	65	MHz/Volt	$\Delta F/\Delta V$ Measured with VCO Control at 2V - 3V
Phase Detector Gain	Kd	100	145	200	$\mu A/rad$	

March 1996

REDUCED EMI CLOCK GENERATOR

CHARTS



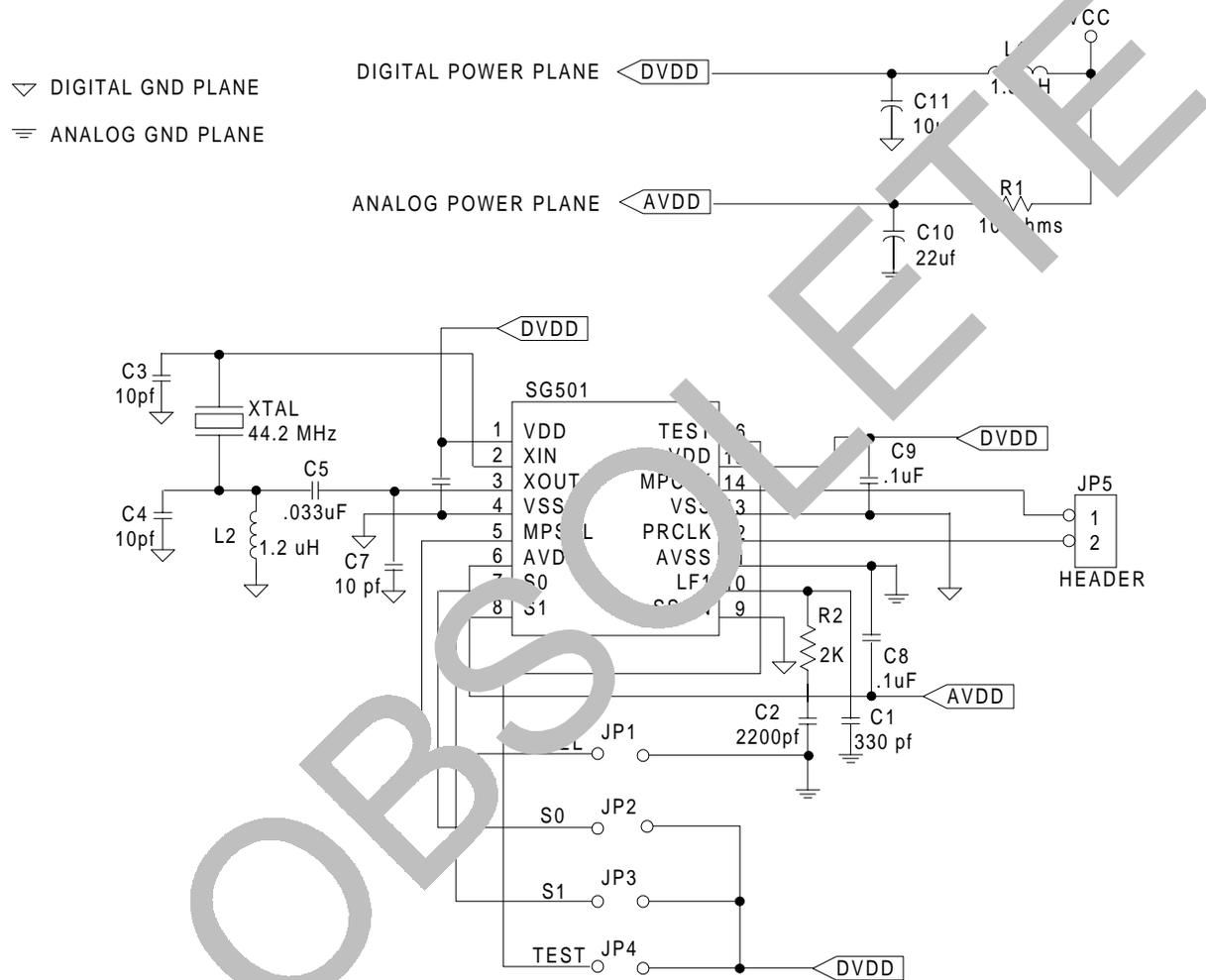
FREQUENCY SELECTION		
S0	S1	SCALING FACTOR ($\frac{\text{PRCLK}}{\text{REFERENCE}}$)
0	0	.225
0	1	.450
1	0	.562
1	1	1.25

Reference Range: 35 MHz_{MIN} to 55 MHz_{MAX}
Output Range: 8 MHz_{MIN} to 60 MHz_{MAX}

March 1996

REDUCED EMI CLOCK GENERATOR

EXTERNAL CONNECTIONS

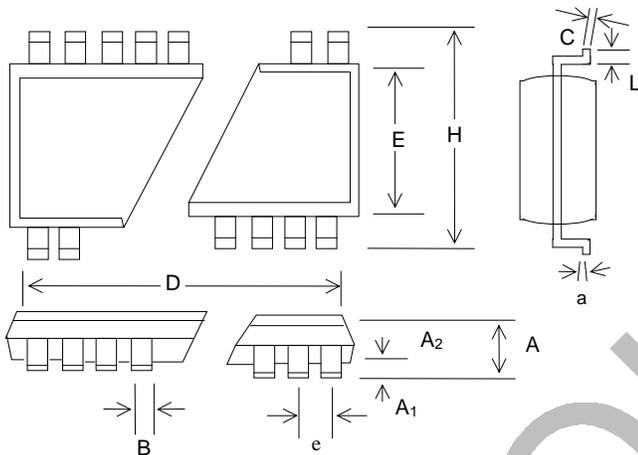


NOTE1: KEEP C3, C4, C5, C6 CLOSE TO THEIR PINS (4, 11, 13, 10, 9 RESPECTIVELY).

March 1996

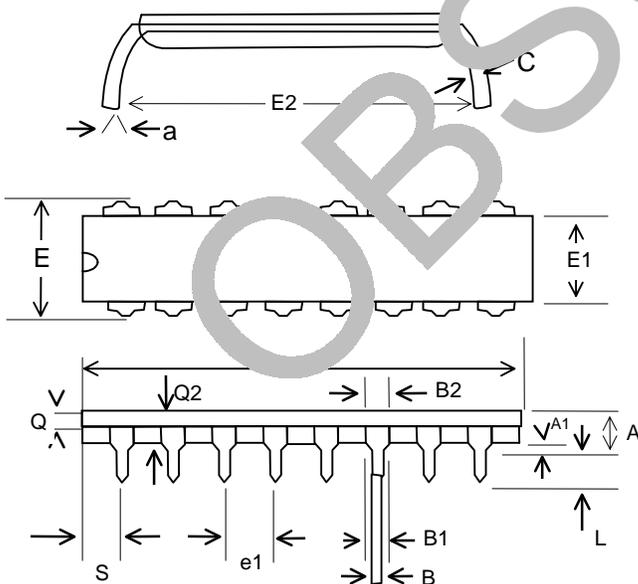
REDUCED EMI CLOCK GENERATOR

PACKAGE DRAWING AND DIMENSIONS



16 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.100	0.100	0.104	2.54	2.54	2.64
A ₁	0.0020	0.000	0.0075	0.051	0.000	0.190
A ₂	0.000	0.092	0.111	0.000	2.34	2.81
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	.399	.407	.412	10.13	10.34	10.46
E	.285	0.296	0.299	7.24	7.52	7.59
e	0.050 BSC			1.27 BSC		
F	0.400	0.406	0.410	10.16	10.31	10.41
a	0°	5°	10°	0°	5°	10°
L	0.024	0.032	0.040	0.61	0.81	1.02



16-PIN PLASTIC DIP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.150	0.160	0.170	3.81	4.06	4.318
A ₁	0.015	-	-	0.381	-	-
B	0.016	0.018	0.020	0.40	0.45	0.50
B ₁	0.056	0.059	0.062	1.47	1.52	1.57
B ₂	0.046	0.049	0.052	1.17	1.24	1.32
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.748	0.750	0.752	19.00	19.05	19.10
E	0.300	0.312	0.325	7.62	7.924	8.255
E ₁	0.240	0.252	0.260	6.096	6.49	6.604
E ₂	0.335	0.345	0.355	8.51	8.76	9.01
e ₁	0.100 BSC			2.54 BSC		
L	0.25	0.230	0.135	3.175	3.30	3.429
a	0°	7°	15°	0°	7°	15°
Q ₁	0.059	0.060	0.061	1.50	1.53	1.55
Q ₂	0.128	0.130	0.132	3.25	3.30	3.35
S	0.073	0.075	0.077	1.85	1.90	1.95

March 1996

REDUCED EMI CLOCK GENERATOR

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG501xPB	16 Pin Plastic Dip	Commercial, 0°C to + 70°C
IMISG501xB	16 Pin SOIC	Commercial, 0°C to + 70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SG501xPB
Date Code, Lot #

IMISG501xPB

