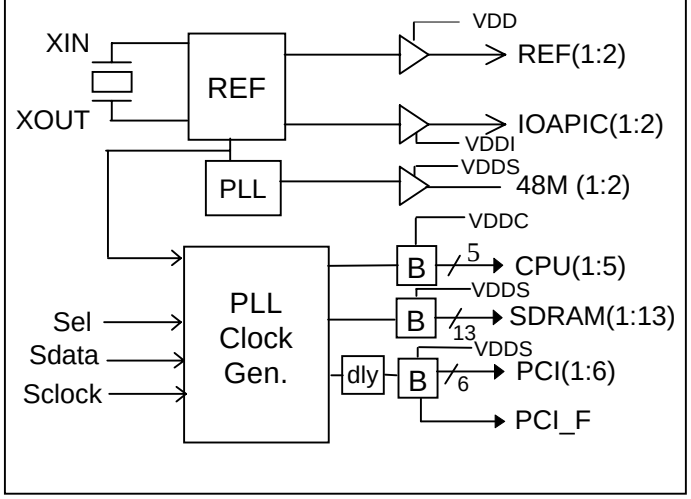
I²C Motherboard Clock Generator with 3 DIMM Support

Preliminary

PRODUCT FEATURES

- Designed to support Intel chipset Specification
- 5 CPU clocks
- 13 SDRAM clocks for DIMs.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (VDD = VDDS = VDDC =VDDI = 3.3V) or
- (VDD = VDDS = 3.3V, VDDC=VDDI = 2.5V)
- < 250ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- Controlled current output buffers
- I²C 2-Wire serial interface
- Programmable registers featuring:
  - enable/disable each output pin
  - mode as tri-state, test, or normal
- 2 IOAPIC clocks for multiprocessor support.
- 56-pin SSOP package

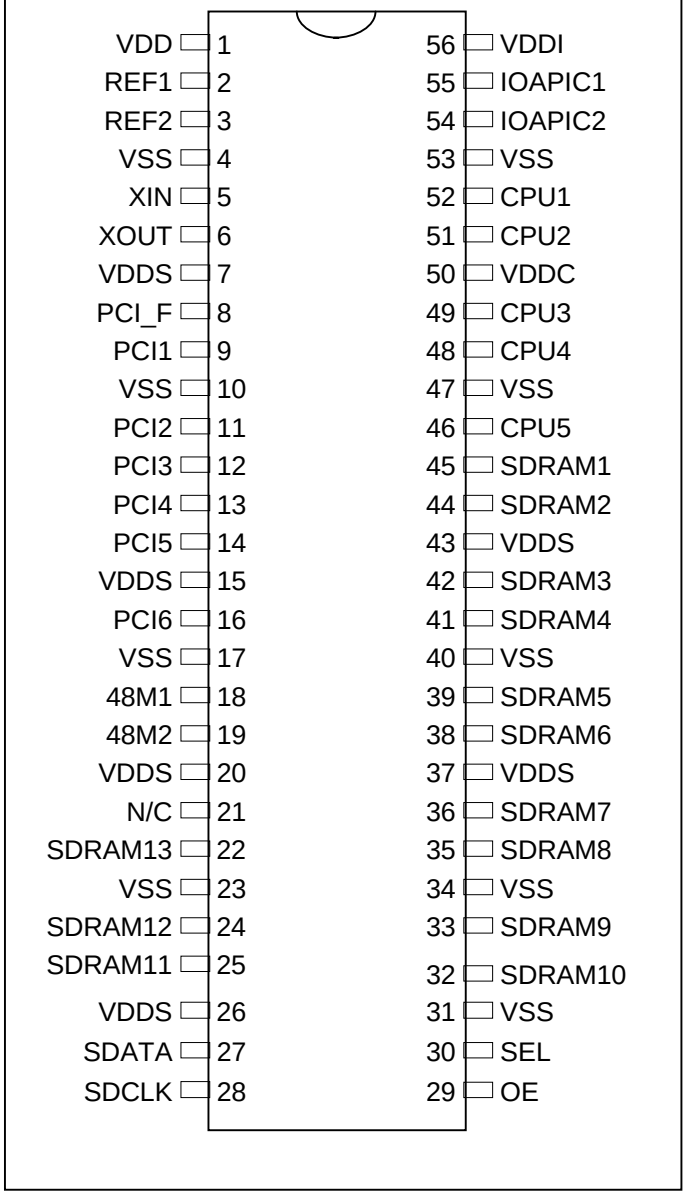
BLOCK DIAGRAM



FREQUENCY TABLE

SEL	CPU	PCI
0	60.0	30.0
1	66.6	33.3

CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
5	**Xin**	Vdd	I	OSC1	On-chip reference oscillator input pin. Requires either an external crystal (nominally 14.318 MHz) or external reference signal. Has internal 36 pF loading capacitor.
6	**Xout**	Vdd	O	OSC1	On chip reference oscillator output pin. Drives an external parallel resonant crystal, is left unconnected. Has internal 36 pF loading capacitor.
30	**SEL**	-	I	PADI4 PU	Frequency select input pins. See frequency select table on page 1.This pin has an internal pull-up
29	**OE**	-	I	PAD4 PU	Output Enable. when pulled to a logis 0 (LOW) Tri-states all clock outputs. This pin has an internal pull-up
52, 51, 49, 48, 46	**CPU(1:5)**	VDDC	O	BUF1	Clock outputs. See frequency select table on page 1.
8	**PCI_F**	VDDP	O	BUF5	Free running copy of the PCI bus output clocks. Powered by VDDP at 3.3 volts.
9, 11, 12, 13, 14, 16	**PCI(1:6)**	VDDS	O	BUF5	PCI bus output clocks. Powered by VDDP at 3.3 volts.
45, 44, 42, 41, 39, 38, 36, 35, 33, 32, 25, 24, 22	**SDRAM(1:13)**	VDDS	O	BUF4	SDRAM clock outputs. See frequency select table on page 1. See frequency select table on page 1.
18, 19	**48M(1:2)**	VDDS	O	BUF5	48 MHz Mhz fixed clock. Is 3.3 volt powered.
28	**SCLK**	-	O	PAD PU	serial clock of I²C 2-wire control interface. Has internal pull-up resistor.
27	**SDATA**	-	I/O	PAD PU	serial data of I²C 2-wire control interface. Has internal pull-up resistor.
55, 54	**IOAPIC(1:2)**	VDDI	O	BUF2	14.31818 Mhz clock. may be 3.3 or 2.5 volt powered.
2	**REF1**	VDD	O	BUF4	High Drive 14.31818 Mhz reference clock. Is 3.3 volt powered.
3	**REF2**	VDD	O	BUF5	14.31818 Mhz reference clock. Is 3.3 volt powered.
4, 10, 17, 23, 31, 40, 47, 53, 34	**VSS**	-	P	-	Ground pins for the device.
1	**VDD**	-	P	-	Power supply pin for 3.3V PCI, SDRAM and fixed clock buffer.
56	**VDDI**	-	P	-	Power supply pin for 2.5V/3.3V IOAPIC clock buffers.
50	**VDDC**	-	P	-	Power supply pin for 2.5V/3.3V CPU clock buffers.
43, 37, 26, 20, 15, 7	**VDDS**	-	P	-	Power supply pins for 3.3V PCI, SDRAM and fixed clock buffers.

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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceeding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below desrcibed sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

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SERIAL CONTROL REGISTERS (Cont.)

BYTE 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	*	Reserved, Don't set
6	0	*	Reserved, Don't set
5	0	*	Reserved, Don't set
4	0	*	Reserved, Don't set
3	x	n/a	Reserved, Don't set
2	x	n/a	Reserved, Don't set
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Reserved 0 1 Test Mode 0 0 Normal

IMPORTANT NOTE

Reserved bits are intended for possible future functions. It is important that they be set to logic 0 at all times otherwise data sheet specifications cannot be guaranteed.

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	Ref	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk
Normal SEL=1	66	CPU/2	CPU	14.318	14.318
Normal SEL=0	60	CPU/2	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

BYTE 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	n/a	Reserved
6	x	n/a	Reserved
5	x	-	Reserved
4	1	46	CPU5 enable/Stopped
3	1	48	CPU4 enable/Stopped
2	1	49	CPU3 enable/Stopped
1	1	51	CPU2 enable/Stopped
0	1	52	CPU1 enable/Stopped

SERIAL CONTROL REGISTERS (Continued)

BYTE 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	8	PCI_F enable/Stopped
5	1	16	PCI6 enable/Stopped
4	1	14	PCI5 enable/Stopped
3	1	13	PCI4 enable/Stopped
2	1	12	PCI3 enable/Stopped
1	1	11	PCI2 enable/Stopped
0	1	9	PCI1 enable/Stopped

BYTE 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	35	SDRAM8 enable/Stopped
6	1	36	SDRAM7 enable/Stopped
5	1	38	SDRAM6 enable/Stopped
4	1	39	SDRAM5 enable/Stopped
3	1	41	SDRAM4 enable/Stopped
2	1	42	SDRAM3 enable/Stopped
1	1	44	SDRAM2 enable/Stopped
0	1	45	SDRAM1 enable/Stopped

BYTE 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	22	SDRAM13 enable/Stopped
3	1	24	SDRAM12 enable/Stopped
2	1	25	SDRAM11 enable/Stopped
1	1	32	SDRAM10 enable/Stopped
0	1	33	SDRAM9 enable/Stopped

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SERIAL CONTROL REGISTERS(Continued)

BYTE 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	2	REF1 enable/Stopped
5	1	54	IOAPIC2 enable/Stopped
4	1	55	IOAPIC1 enable/Stopped
3	x	-	Reserved
2	1	19	48M2 enable/Stopped
1	1	18	48M1 enable/Stopped
0	1	3	REF2 enable/Stopped

BYTE 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	TBD	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	TBD	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDP=3.465V to ***3.135V , VDDC= VDDI = 2.375V to 2.9V, TA = 0ºC to +70ºC***						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
∆Period Adjacent Cycles	∆P	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Overshoot/Undershoot Beyond Power Rails	V_{over}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	note1
VDD = VDDP =3.30V +/- 5% , VDDC = VDDI = 2.5V +/- 5%, TA = 0ºC to +70ºC						

note 1: Ring Back must not enter this range.

TYPE 1 BUFFER CHARACTERISTICS FOR CPUCLK(1:5)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-27	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	TBD	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD = VDDP =3.30V +/- 5% , VDDC= VDDI = 2.5V +/- 5%, TA = 0ºC to +70ºC						

TYPE 2 BUFFER CHARACTERISTICS FOR IOAPIC(1:2)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	TBD	-	-	mA	Vout = 1.4 V
Pull-Up Current Max	IOH_{max}	-	-	-29	mA	Vout = 2.7 V
Pull-Down Current Min	IOL_{min}	TBD	-	-	mA	Vout = 1.0 V
Pull-Down Current Max	IOL_{max}	-	-	28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	0.4	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}	-	-	1.6	nS	20 pF Load
VDD =VDDF =3.30V +/- 5% , VDDC = VDDI = 2.5V +/- 5%, TA = 0ºC to +70ºC						

TYPE 4 BUFFER CHARACTERISTICS FOR REF1 and SDRAM(1:13)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	TBD	-	-	mA	Vout = 1.65 V
Pull-Up Current Max	IOH_{max}	-	-	-46	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	TBD	-	-	mA	Vout = 1.65 V
Pull-Down Current Max	IOL_{max}	-	-	53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	20 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.3	nS	30 pF Load
VDD = VDDP =3.30V +/- 5% , VDDC= VDDI = 2.5V +/- 5%, TA = 0ºC to +70ºC C						

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TYPE 5 BUFFER CHARACTERISTICS FOR REF2 AND PCI(1:6,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	15 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	30 pF Load
VDD = VDDP =3.30V +/- 5% , VDDC= VDDI = 2.5V +/- 5%, TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	the crystals rated load. note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)
For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. Budgeting Calculations Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF the total parasitic capacitance would therefore be = 20.0.0 pF.						

Note 1: It is recommended but not manditory that a crystal meets these specifications.

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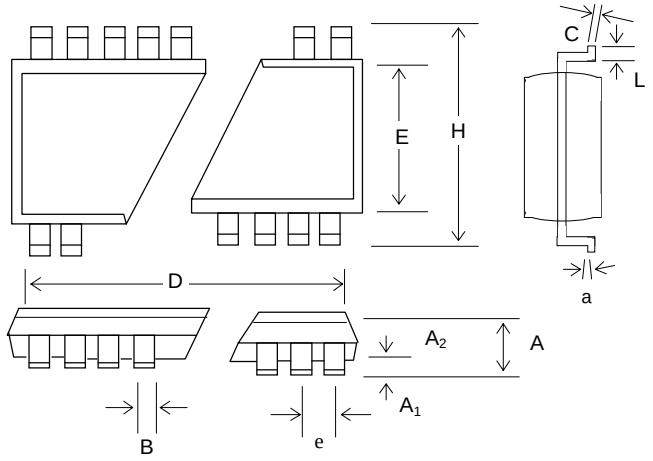
PACKAGE DRAWING AND DIMENSIONS



56 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D						
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC678AYB	56 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC678AYB
Date Code, Lot #

IMISC678AYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

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