System Clock Generator with Power Management

Preliminary

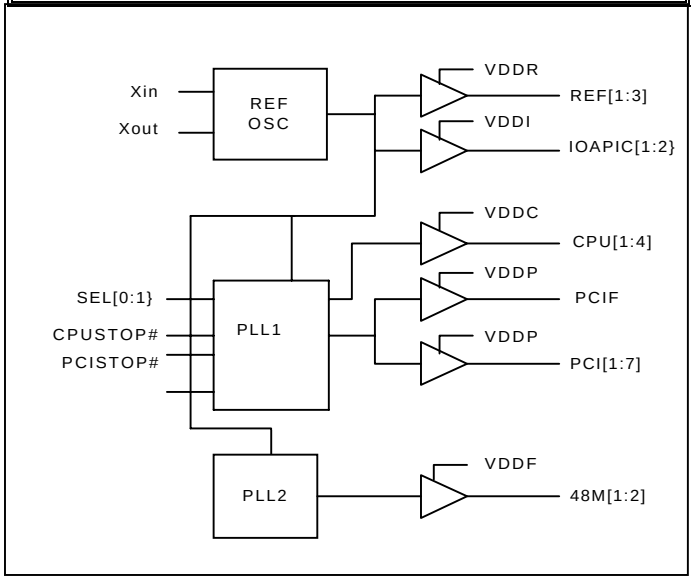
PRODUCT FEATURES

- Supports Pentium & Pro CPUs.
- 4 CPU and 8 PCI clocks
- 2 48 Mhz fixed clocks for USB and Super IO.
- Separate supply pins for mixed CPU, IOAPIC, and Fixed/PCI clocks
- < 175ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- Controlled current output buffers
- CPU clock stop
- PCI Stop Clock
  Power Down
- 2 IOAPIC clocks for multiprocessor support.
- 48-pin SSOP package

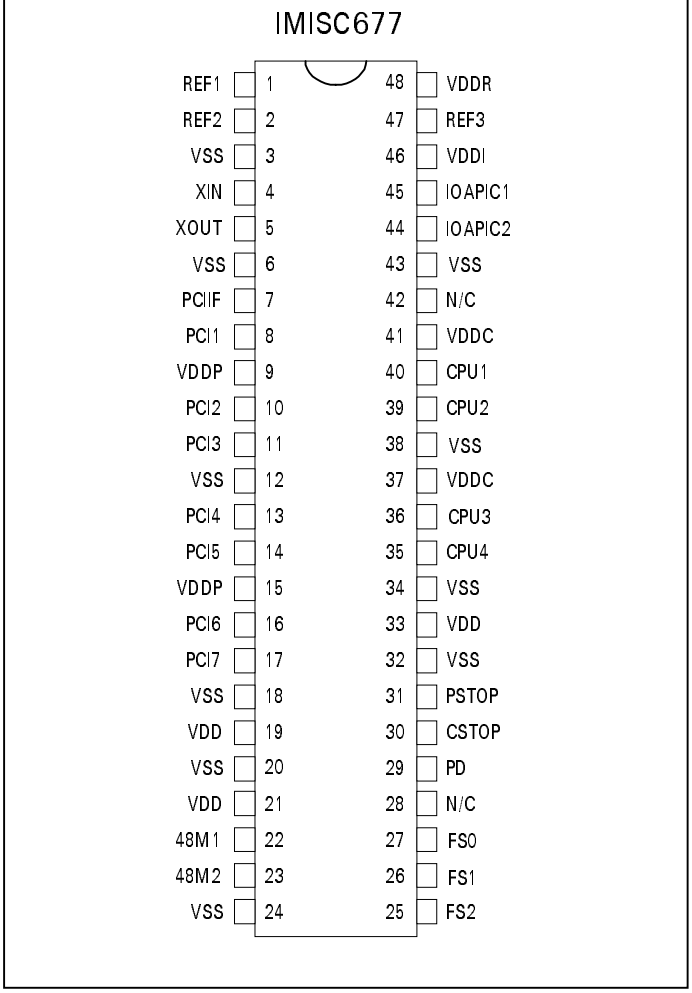
FREQUENCY TABLE

FS2	FS1	FS0	CPU	PCI
0	0	0	Tri-State	Tri-state
0	1	1	66.5	33.3
1	0	0	Ref/2	Ref/4
1	1	1	100 (99.7)	33.41

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	O-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
25, 26, 27	**FS(0:2)**	-	I	PADI4 PU	Frequency select input pins. See frequency select table on page 1.These pin has an internal pull-up
40, 39, 36, 35	**CPU(1:4)**	VDDC	O	BUF1	Clock outputs. CPU frequency table specified on page 1.
45, 44	**IOAPIC(1:2)**	VDDI	O	BUF2	IOAPIC clock for multi proscssor support. Fixed frequency at 14.31818 Mhz. (2.5 or 3.3 supply = VDDI)
8, 10, 11, 13, 14, 16, 17	**PCI(1:7)**	VDDP	O	BUF4	PCI bus clocks. See frequency select table on page 1.
7	**PCI_F**	VDDP	O	BUF4	PCI clock that ceases only when PD (pin 29) is ascerted. See frequency select table on page 1.
3, 6, 12, 18, 20, 24, 32, 34, 38, 43	**VSS**	-	P	-	Ground pins for the device.
46	**VDDI**	-	P	-	3.3 or 2.5 Volt power supply pins for IOAPIC clock output buffers.
9, 15	**VDDP**	-	P	-	3.3 Volt power supply pins for PCI and PCI_F clock output buffers.
21	**VDDF**	-	P	-	3.3 Volt power supply pins for 48 MHz clock output buffers.
48	**VDDR**	-	P		3.3 Volt power supply pins for reference clock output buffers.
37, 41	**VDDC**	-	P	-	3.3 or 2.5 Volt power supply pins for CPU clock output buffers.
19, 33	**VDD**				Power supply pins for analog circuits and core logic
1, 2, 47	**REF(1:3)**	VDDR	O	BUF3	Buffered outputs of on-chip reference oscillator.
22, 23	**48M(1:2)**	VDDF	O	BUF3	Fixed 48 Mhz frequency clock outputs.
31	**PSTOP**	-	I	PAD PU	When driven to a logic low level, this pin will synchronously stop all PCI clocks (except PCI_F) at a logic low level.
30	**CSTOP**	-	I	PAD PU	When driven to a logic low level, this pin will synchronously stop all CPU clocks at a logic low level.
29	**PD**	-	I	PAD PU	When this pin is driven to a logic low the IC will enter shutdown mode and **ALL** internal circuitry is turned off.

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	Outputs				
Descriptions	**CPU**	**PCI, PCIF**	**48 Mhz**	**REF1:3**	**IOAPIC**
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2	TCLK/4	TCLK/2	TCLK	TCLK

NOTE:
TCLK is a test clock that is driven into the XTAL_IN input during test mode.

POWER MANAGEMENT FUNCTIONS

All PCI (excluding PCI_F) and CPU clocks can be enabled or stopped via the PSTOP and CSTOP input pins. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, (after bring PD from a low to high state) the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CSTOP	PSTOP	PD	CPUCLK	PCICLK	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	RUNNING	RUNNING	RUNNING
1	0	1	RUNNING	LOW	RUNNING	RUNNING
1	1	1	RUNNING	RUNNING	RUNNING	RUNNING

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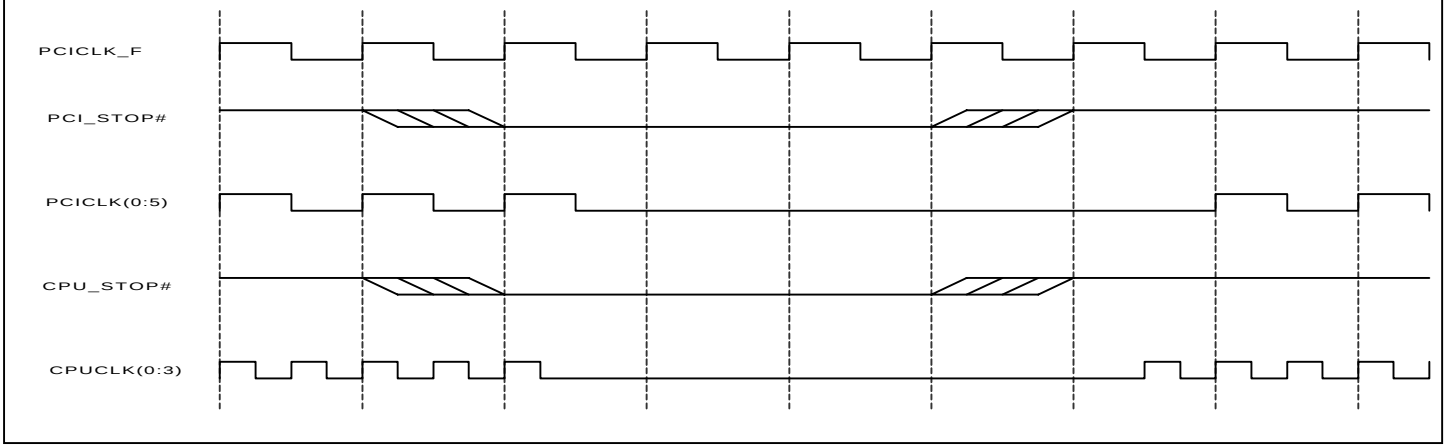
POWER MANAGEMENT TIMING



POWER MANAGEMENT TIMING		
Signal	**Signal State**	**Latency**
		No. of rising edges of free running PCICLK (PCIF)
CPU_Stop#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3 mS
	0 (power down)	2 max.

NOTES:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	140	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	70	mA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew All CPU Buffer Outputs	$tSKEW_1$	-	-	175	ps	20 pf Load Measured at 1.5V
Buffer out Skew All PCI Buffer Outputs	$tSKEW_2$	-	-	250	ps	30 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC						

BUFFER 1 CHARACTERISTICS FOR CPUCLK(1:4)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-27	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-27	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	27	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.3 V
Rise Time Between 0.4 V and 2.0 V	TR	0.4	-	1.6	nS	20 pF Load
Fall Time Between 0.4 V and 2.0 V	TF	0.5	-	1.6	nS	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC						

BUFFER 2 CHARACTERISTICS FOR IOAPIC (1:2)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	36	-	-	mA	Vout = 1.4 V
Pull-Up Current Max	IOH_{max}	-	-	-29	mA	Vout = 2.7 V
Pull-Down Current Min	IOL_{min}	36	-	-	mA	Vout = 1.0 V
Pull-Down Current Max	IOL_{max}	-	-	28	mA	Vout = 0.2 V
Rise Time Between 0.4 V and 2.0 V	TR	0.5	-	1.6	nS	20pF Load
Fall Time Between 0.4 V and 2.0V	TF	0.5	-	1.6	nS	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC						

BUFFER 3 CHARACTERISTICS FOR REF(1:3) and 48(1:2) MHz						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-29	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-23	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	29	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	20 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	20 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC						

BUFFER 4 CHARACTERISTICS FOR PCICLK(1:8,F)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	30 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	30 pF Load
VDD = VDDP=VDDF =VDDR =3.3V ±5%, VDDC, & VDDI = 2.5V ±5%,, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerence	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallell Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	
X1 and X2 Load	CL		17		pF	internal crystal loading gapacitors on each pin (to ground)

For maximum accuracy,the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0 pF.(matching CL)

Note 1: It is recommended but not manditory that a crystal meets these specifications.

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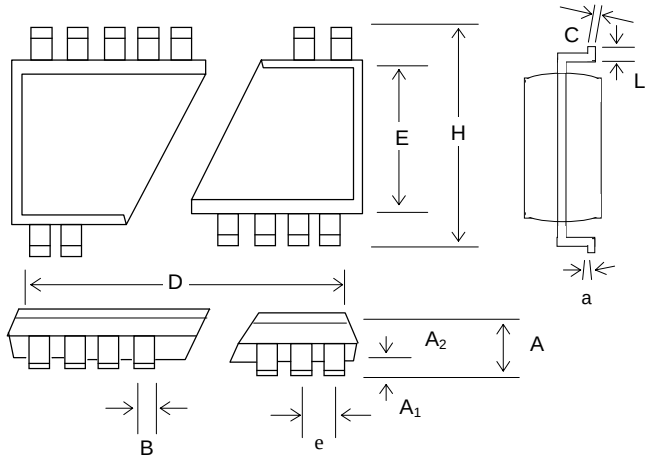
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC677CYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC677CYB
Date Code, Lot #

IMISC677CYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number