



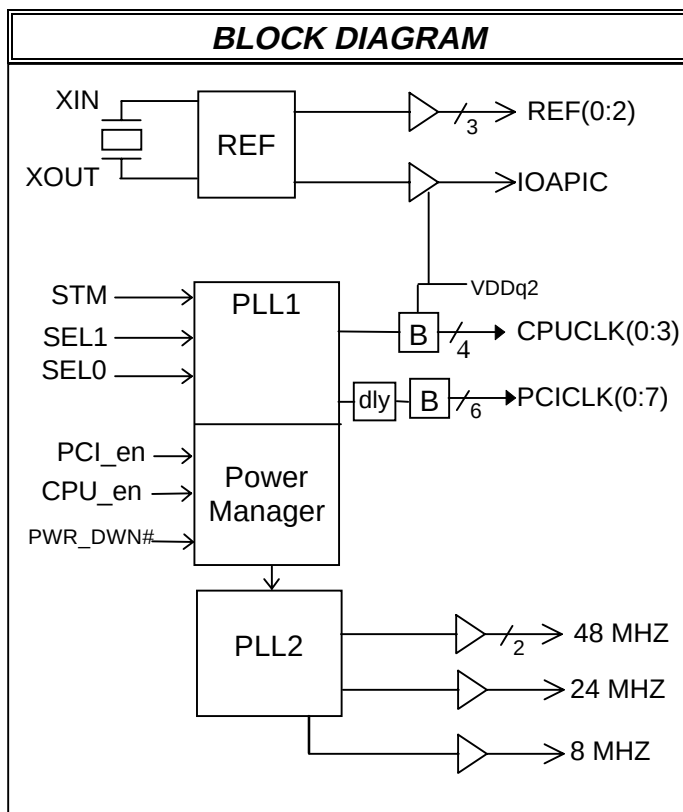
## Clock/Frequency Generator for 440FX w/Pentium II & Pro Systems

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### PRODUCT FEATURES

- Designed to the Intel spec. for supporting next generation Intel processor and Pentium-pro's with 2.5V clocking requirements with the Intel 440FX chipset.
- 4 host (CPU) clocks.
- IOAPIC for multiprocessing.
- Power management for Mobile applications.
- < 250 pS skew on CPU buffers
- < 250 pS skew on PCI buffers
- 48 Pin SSOP package for minimum board space

### BLOCK DIAGRAM

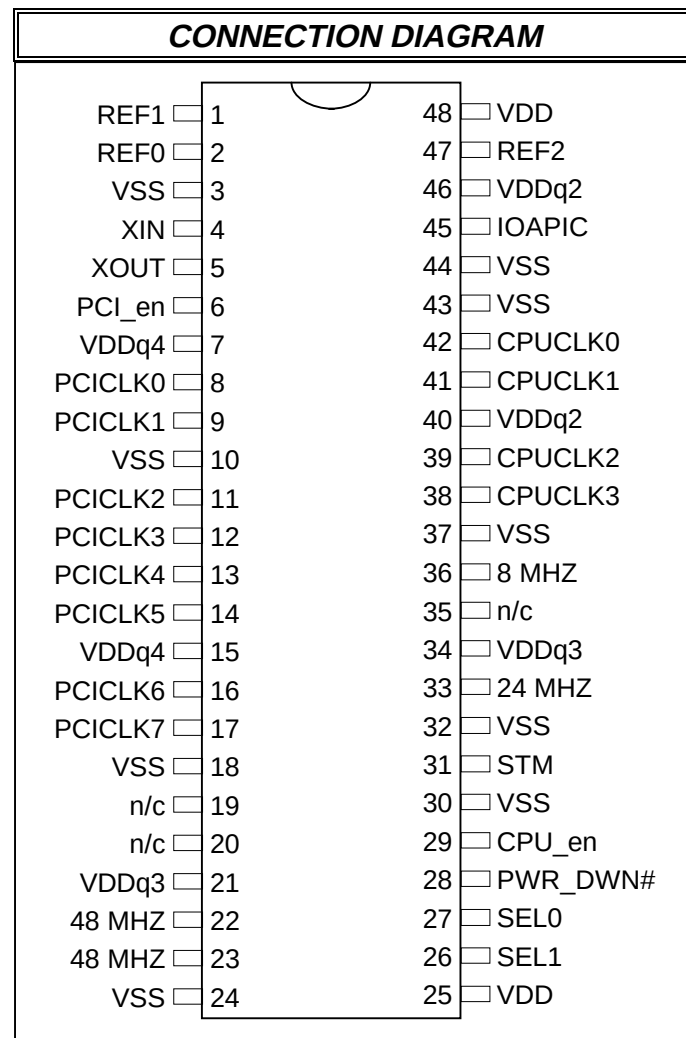


### FREQUENCY TABLE

| STM | SEL1 | SEL0 | CPU      | PCI      |
|-----|------|------|----------|----------|
| X   | 0    | 0    | Tristate | Tristate |
| 0   | 0    | 1    | 63.0     | 31.5     |
| 0   | 1    | 0    | 69.87    | 34.94    |
| X   | 1    | 1    | XIN/2    | XIN/4    |
| 1   | 0    | 1    | 60       | 30       |
| 1   | 1    | 0    | 66.44    | 33.22    |

X = Don't Care

### CONNECTION DIAGRAM





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### PIN DESCRIPTION

**XIN, XOUT** - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). XIN may also serve as input for an externally generated reference signal.

**SEL(0:1)** - Standard frequency select inputs. They have internal pull-ups.

**CPUCLK(0:3)** - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache. VDDq2 is the supply voltage for these outputs.

**PCICLK(0:7)** - Low skew (<250pS) clock outputs for PCI frequencies. They are synchronous to CPUCLK's.

**REF(0:2)** - Buffered outputs of reference 14.3 MHz.

**IOAPIC** - Buffered output of 14.3 MHz for multiprocessor support. It is powered by VDDq2.

**48 MHz** - Frequency output for USB.

**24 MHz** - Frequency output for super I/O.

**8 MHz** - 8 MHz output frequency.

**PWR\_DWN#** - Power down pin to turn the power of the whole chip down including the VCOs and the crystal buffer. It has an internal Pull-Up.

**CPU\_en** - Active low signal to stop the CPU clocks when low. It is high in normal operation and has an internal Pull-Up.

**PCI\_en** - Active low signal to stop the PCI clocks, when low. It is high in normal operation and has an internal Pull-Up.

**STM** - System test mode. Increased PCI and CPU clocks by 4.75% for system timing testing when low.

**VSS** - Ground pins for the chip.

**VDD** - Power supply pins for analog and core circuitry.

**VDDq4** - Power supply pins for 3.3V for PCI bus.

**VDDq3** - Power supply pins for 3.3V IO pins.

**VDDq2** - Power supply pins for 2.5V/3.3V IO pins.

**N/C** - No connection pins.

### FUNCTION TABLE

| SEL1 | SEL0 | CPU      | PCI      | REF(0:2)   | IOAPIC     | 24 MHz   | 48 MHz   | 8 MHz    |
|------|------|----------|----------|------------|------------|----------|----------|----------|
| 0    | 0    | Tristate | Tristate | Tristate   | Tristate   | Tristate | Tristate | Tristate |
| 0    | 1    | Note1    | Note1    | 14.318 MHz | 14.318 MHz | 24 MHz   | 48 MHz   | 8 MHz    |
| 1    | 0    | Note1    | Note1    | 14.318 MHz | 14.318 MHz | 24 MHz   | 48 MHz   | 8 MHz    |
| 1    | 1    | XIN/2    | XIN/4    | XIN        | XIN        | XIN/4    | XIN/2    | XIN/12   |

Note1: See Frequency Table, Page 1



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### POWER MANAGEMENT FUNCTIONS

The IMISC672 clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. On low to high transitions of PWR\_DWN#, external circuitry should allow 2-3 mS for the VCOs to stabilize prior to releasing PCI\_en or CPU\_en to a high level. The CPU and PCI clocks transition between running and stopped following the latency table below. CPU and PCI clocks are stopped after a complete period in their low state.

| CPU_en | PCI_en | PWR_DWN# | CPUCLK | PCICLK | OTHER CLKs | XTAL & VCOs |
|--------|--------|----------|--------|--------|------------|-------------|
| X      | X      | 0        | LOW    | LOW    | LOW        | OFF         |
| 0      | 0      | 1        | LOW    | LOW    | RUNNING    | RUNNING     |
| 0      | 1      | 1        | LOW    | Note2  | RUNNING    | RUNNING     |
| 1      | 0      | 1        | Note2  | LOW    | RUNNING    | RUNNING     |
| 1      | 1      | 1        | Note2  | Note2  | RUNNING    | RUNNING     |

Note2: See Frequency Table, Page 1

| Signal   | Signal State  | Min Pulse Width<br>(count by clocks) | Min Latency<br>(count by CPU clocks) | Max Latency<br>(count by CPU clocks) |
|----------|---------------|--------------------------------------|--------------------------------------|--------------------------------------|
| CPU_en   | 0 (disabled)  | 100 CPU                              | 1                                    | 4                                    |
|          | 1 (enabled)   | 10 CPU                               | 1                                    | 4                                    |
| PCI_en   | 0 (disabled)  | 10 PCI                               | 2                                    | 4                                    |
|          | 1 (enabled)   | 10 PCI                               | 2                                    | 4                                    |
| PWR_DWN# | 0 (power off) | 3mS                                  | 1                                    | 4                                    |
|          | 1 (normal)    | 3mS                                  | 2 mS                                 | 3 mS                                 |

### MAXIMUM RATINGS

|                          |                  |
|--------------------------|------------------|
| Voltage Relative to VSS: | -0.3V            |
| Voltage Relative to VDD: | 0.3V             |
| Storage Temperature:     | -65°C to + 150°C |
| Operating Temperature:   | -0°C to + 70°C   |
| Maximum Power Supply:    | 7V               |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).



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### ELECTRICAL CHARACTERISTICS

| Characteristic                     | Symbol | Min | Typ | Max | Units | Conditions                                              |
|------------------------------------|--------|-----|-----|-----|-------|---------------------------------------------------------|
| Input Low Voltage                  | VIL    | -   | -   | 0.8 | Vdc   | -                                                       |
| Input High Voltage                 | VIH    | 2.0 | -   | -   | Vdc   | -                                                       |
| Input Low Current                  | IIL    |     |     | -66 | μA    |                                                         |
| Input High Current                 | IIH    |     |     | 5   | μA    |                                                         |
| Output Low Voltage<br>IOL = 12 mA  | VOL    | -   | -   | 0.4 | Vdc   | All Outputs (see switching spec)                        |
| Output High Voltage<br>IOH = 12 mA | VOH    | 2.4 | -   | -   | Vdc   | All Outputs (see switching spec)                        |
| Tri-State leakage Current          | Ioz    | -   | -   | 10  | μA    |                                                         |
| Dynamic Supply Current             | IDD    | -   | 40  | 90  | mA    | CPU = 66.6 MHZ, No Load                                 |
| Static Supply Current              | IDD    | -   | 20  | 30  | mA    | CPU = 66.6 MHZ, No Load<br>CPU_en = Low<br>PCI_en = Low |
| Short Circuit Current              | ISC    | 25  | -   | -   | mA    | 1 output at a time - 30 seconds                         |

**VDD = VDDq2 = VDDq3 = VDDq4 = 3.3V±5%, TA = 0°C to +70°C**

### SWITCHING CHARACTERISTICS

| Characteristic                                    | Symbol            | Min | Typ | Max  | Units | Conditions                                            |
|---------------------------------------------------|-------------------|-----|-----|------|-------|-------------------------------------------------------|
| Output Duty Cycle                                 | -                 | 45  | 50  | 55   | %     | See note 3                                            |
| CPUCLK(0:3) High Time                             | tHKH              | 5.2 | -   | -    | nS    | @ 66.6 MHZ, Measured at 2.0V                          |
| CPUCLK(0:3) Low Time                              | tHKL              | 5.0 | -   | -    | nS    | @ 66.6 MHZ, Measured at 0.4V                          |
| CPUCLK(0:3) High Time                             | tHKH              | 6.0 | -   | -    | nS    | @ 60 MHZ, Measured at 2.0V                            |
| CPUCLK(0:3) Low Time                              | tHKL              | 5.8 | -   | -    | nS    | @ 60 MHZ, Measured at 0.4V                            |
| CPU to PCI Offset                                 | tOFF              | 1   | -   | 4    | nS    | See Note 3                                            |
| Buffer out Skew All CPU<br>and PCI Buffer Outputs | tSKEW             | -   | -   | 250  | pS    | See Note 3                                            |
| ΔPeriod Adjacent Cycles                           | ΔP                | -   | -   | ±250 | pS    | -                                                     |
| Jitter Absolute, CPU                              | tjab              |     |     | 500  | pS    | (long term jitter measured over a 3<br>minute period) |
| Overshoot/Undershoot<br>Beyond Power Rails        | V <sub>over</sub> | -   | -   | 1.5  | V     | 22 ohms @ source of 8 inch PCB run<br>to 15 pf load   |
| Ring Back Exclusion                               | V <sub>RBE</sub>  | 0.7 |     | 2.1  | V     | See Note 4                                            |

**VDD = VDDq3 = VDDq4 = 3.3V ±5%, VDDq2 = 2.375V to 2.9V, TA = 0°C to +70°C**

Note 3: CPUCLK(0:3) are measured at 1.25 V. All other signals are measured at 1.5V.

Note 4: Ring Back must not enter this range.



## Clock/Frequency Generator for 440FX w/Pentium II & Pro Systems

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### TYPE TB4L BUFFER CHARACTERISTICS FOR CPUCLK(0:3) and IOAPIC

| Characteristic                                | Symbol             | Min | Typ | Max | Units | Conditions          |
|-----------------------------------------------|--------------------|-----|-----|-----|-------|---------------------|
| Pull-Up Current Min                           | IOH <sub>min</sub> | 22  | -   | -   | mA    | Vout = 1.25 V       |
| Pull-Up Current Max                           | IOH <sub>max</sub> | 13  | -   | -   | mA    | Vout = Vddq2 - 0.5V |
| Pull-Down Current Min                         | IOL <sub>min</sub> | 50  | -   | -   | mA    | Vout = 1.5 V        |
| Pull-Down Current Max                         | IOL <sub>max</sub> | 18  | -   | -   | mA    | Vout = 0.4 V        |
| Rise/Fall Time Min<br>Between 0.4 V and 2.0 V | TRF                | 0.4 | -   | 1.8 | nS    | 20 pF Load          |
| Rise/Fall Time Max<br>Between 0.4 V and 2.0 V | TRF <sub>max</sub> | -   | -   | 2.3 | nS    | 20 pF Load          |

$VDD = VDDq3 = VDDq4 = 3.3V \pm 5\%$ ,  $VDDq2 = 2.375V$  to  $2.9V$ ,  $TA = 0^{\circ}C$  to  $+70^{\circ}C$

### TYPE TB5L BUFFER CHARACTERISTICS FOR REF(1:2) and 48/24 MHZ

| Characteristic                                | Symbol             | Min | Typ | Max | Units | Conditions      |
|-----------------------------------------------|--------------------|-----|-----|-----|-------|-----------------|
| Pull-Up Current Min                           | IOH <sub>min</sub> | 30  | -   | -   | mA    | Vout = 1.5 V    |
| Pull-Up Current Max                           | IOH <sub>max</sub> | 13  | -   | -   | mA    | Vout = Vdd-0.5V |
| Pull-Down Current Min                         | IOL <sub>min</sub> | 32  | -   | -   | mA    | Vout = 1.5 V    |
| Pull-Down Current Max                         | IOL <sub>max</sub> | 13  | -   | 29  | mA    | Vout = 0.4 V    |
| Rise/Fall Time Min<br>Between 0.4 V and 2.4 V | TRF <sub>min</sub> | 1.0 | -   | -   | nS    | 20 pF Load      |
| Rise/Fall Time Max<br>Between 0.4 V and 2.4 V | TRF <sub>max</sub> | -   | -   | 4.0 | nS    | 20 pF Load      |

$VDD = VDDq3 = VDDq4 = 3.3V \pm 5\%$ ,  $VDDQ2 = 2.375V$  to  $2.9V$ ,  $TA = 0^{\circ}C$  to  $+70^{\circ}C$

### TYPE TB4L BUFFER CHARACTERISTICS FOR REF0 and PCI

| Characteristic                                | Symbol             | Min | Typ | Max | Units | Conditions      |
|-----------------------------------------------|--------------------|-----|-----|-----|-------|-----------------|
| Pull-Up Current Min                           | IOH <sub>min</sub> | 44  | -   | -   | mA    | Vout = 1.5 V    |
| Pull-Up Current Max                           | IOH <sub>max</sub> | 18  | -   | -   | mA    | Vout = Vdd-0.5V |
| Pull-Down Current Min                         | IOL <sub>min</sub> | 50  | -   | -   | mA    | Vout = 1.5 V    |
| Pull-Down Current Max                         | IOL <sub>max</sub> | 18  | -   | -   | mA    | Vout = 0.4 V    |
| Rise/Fall Time Min<br>Between 0.4 V and 2.4 V | TRF <sub>min</sub> | 0.5 | -   | 1.4 | nS    | 30 pF Load      |
| Rise/Fall Time Max<br>Between 0.4 V and 2.4 V | TRF <sub>max</sub> | -   | -   | 2.4 | nS    | 30 pF Load      |

$VDD = VDDq3 = VDDq4 = 3.3V \pm 5\%$ ,  $VDDq2 = 2.375V$  to  $2.9V$ ,  $TA = 0^{\circ}C$  to  $+70^{\circ}C$

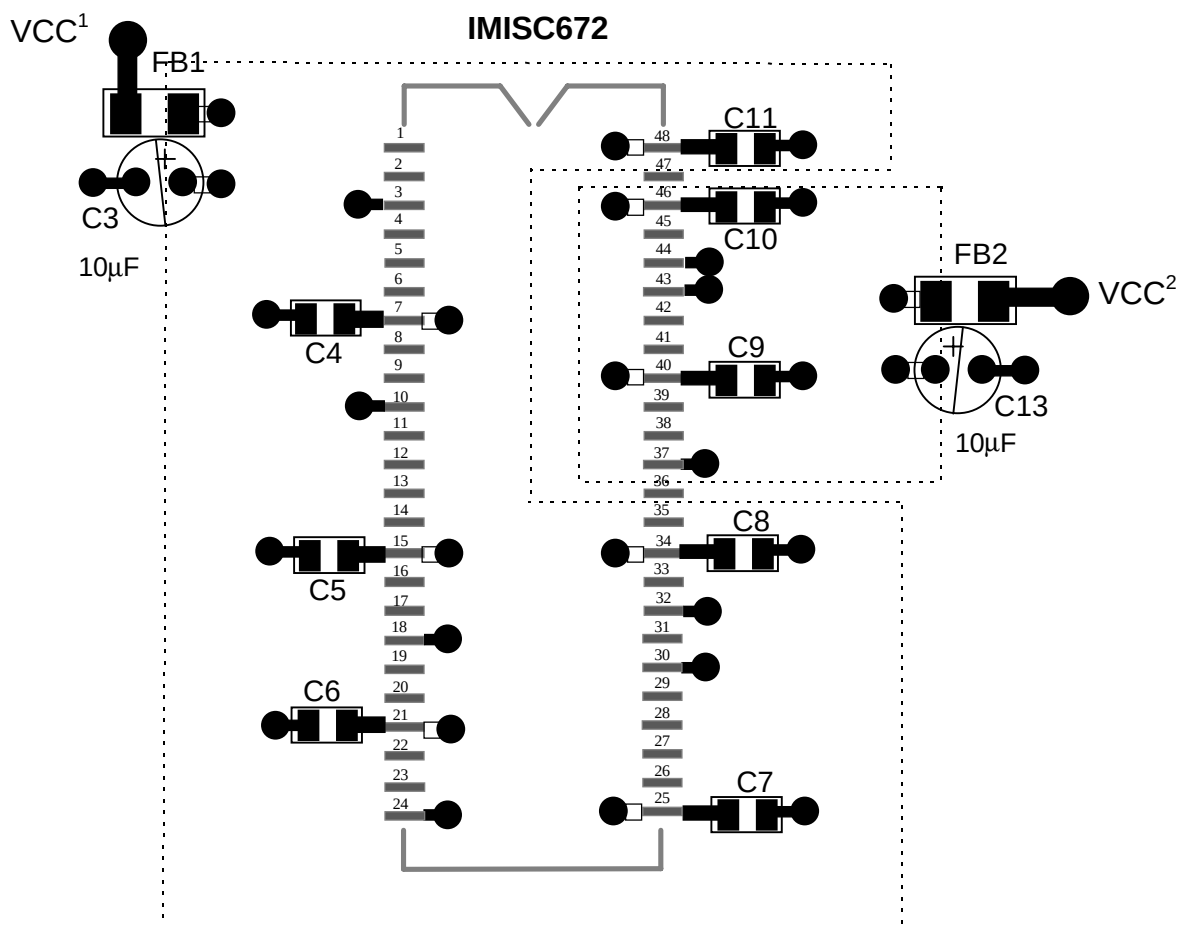


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### PCB LAYOUT RECOMMENDATION

-  Via to VDD Island
-  Via to GND plane
-  Via to VCC plane



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C4, C5, C6, C7, C8, C9, C10, and C11 (all are 0.1μf) should always be used and placed close to their VDD pins.

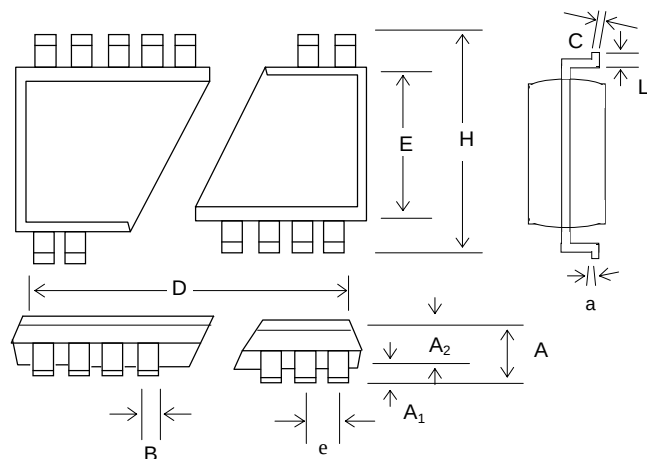


# SC672A

## Clock/Frequency Generator for 440FX w/Pentium II & Pro Systems

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### PACKAGE DRAWING AND DIMENSIONS



#### 48 PIN SSOP OUTLINE DIMENSIONS

| SYMBOL         | INCHES    |       |        | MILLIMETERS |       |       |
|----------------|-----------|-------|--------|-------------|-------|-------|
|                | MIN       | NOM   | MAX    | MIN         | NOM   | MAX   |
| A              | 0.095     | 0.102 | 0.110  | 2.41        | 2.59  | 2.79  |
| A <sub>1</sub> | 0.008     | 0.012 | 0.016  | 0.20        | 0.31  | 0.41  |
| A <sub>2</sub> | 0.088     | 0.090 | 0.092  | 2.24        | 2.29  | 2.34  |
| B              | 0.008     | 0.010 | 0.0135 | 0.203       | 0.254 | 0.343 |
| C              | 0.005     | -     | 0.010  | 0.127       | -     | 0.254 |
| D              | 0.620     | 0.625 | 0.630  | 15.75       | 15.88 | 16.00 |
| E              | 0.292     | 0.296 | 0.299  | 7.42        | 7.52  | 7.59  |
| e              | 0.025 BSC |       |        | 0.635 BSC   |       |       |
| H              | 0.400     | 0.406 | 0.410  | 10.16       | 10.31 | 10.41 |
| a              | 0.10      | 0.013 | 0.016  | 0.25        | 0.33  | 0.41  |
| L              | 0.024     | 0.032 | 0.040  | 0.61        | 0.81  | 1.02  |
| X              | 0.085     | 0.093 | 0.100  | 2.16        | 2.36  | 2.54  |

### ORDERING INFORMATION

| Part Number | Package Type | Production Flow          |
|-------------|--------------|--------------------------|
| IMISC672AYB | 48 PIN SSOP  | Commercial, 0°C to +70°C |

**Note:** The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: IMI  
SC672AYB  
Date Code, Lot #

IMISC672AYB

- Flow  
B = Commercial, 0°C to + 70°C
- Package  
Y = SSOP
- Revision
- IMI Device Number