Low Cost Clock Generator for Pentium™ Based Designs (3 DIMM)

Preliminary

PRODUCT FEATURES

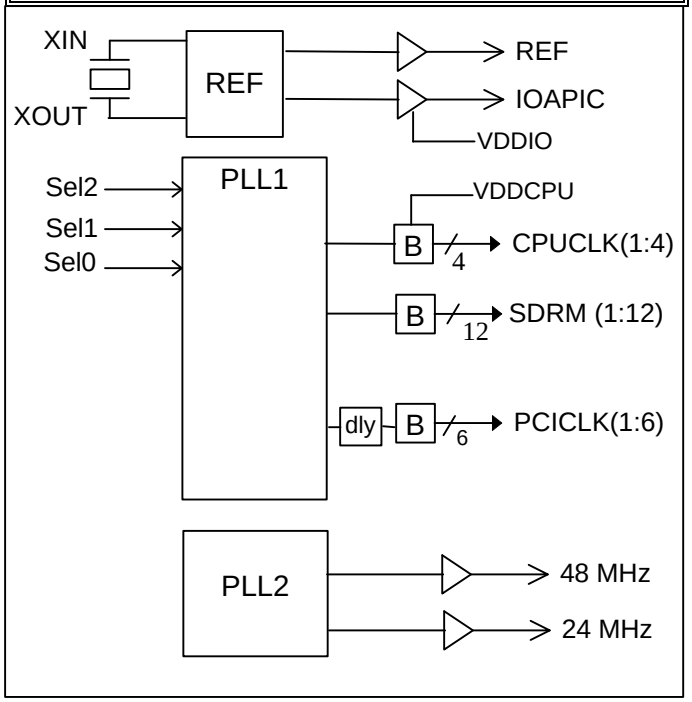
- Designed to the Intel spec. for supporting three Synchronous DRAM with the Intel chipset .
- 4 host (CPU) clocks.
- 12 SDRAM Clocks for 3 DIMM support.
- 6 PCI clocks
- < 250 pS skew on CPU, and PCI buffers
- 48 Pin SSOP package for minimum board space

FREQUENCY TABLE

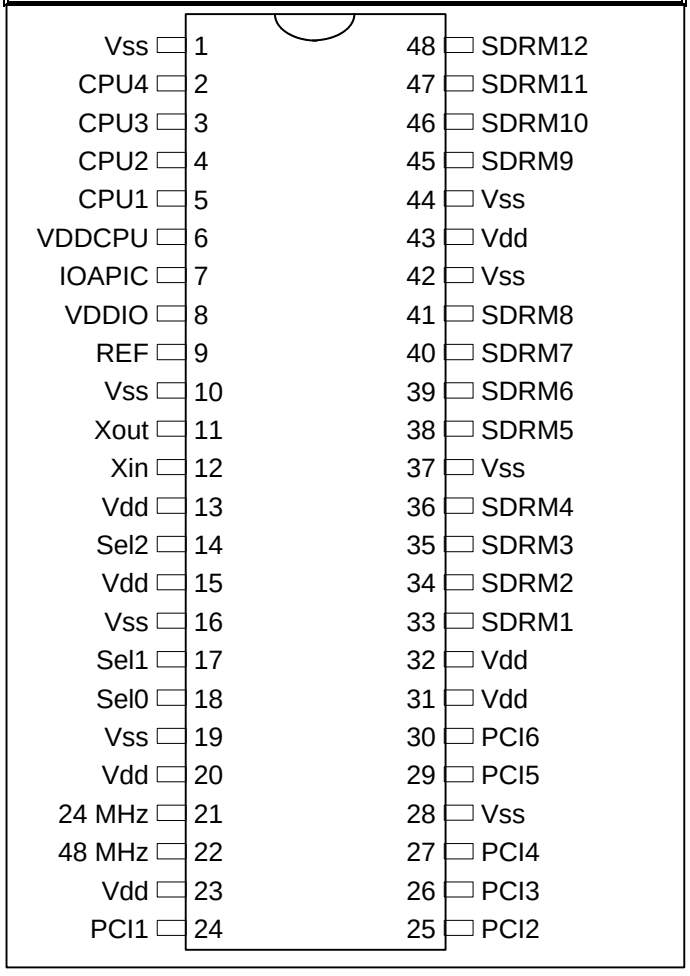
Sel2	Sel1	Sel0	CPU	PCI
0	0	0	tristate	tristate
0	0	1	75	a.32
0	1	0	55	27.5
0	1	1	75	37.5
1	0	0	50	25
1	0	1	60	30
1	1	0	66.6	33.3
1	1	1	test	test

a.32 = Asynchronous PCI.

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	I/O	TYPE	Description
11,12	**Xin, Xout**			These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.
17, 18	**SEL(0:2)**			Standard frequency select inputs. They have internal pull-ups. (See table, Page 1)
2,3,4,5	**CPU (1:4)**			Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache. VDDCPU is the supply voltage for these outputs.
33,34,35, 36,38,39, 40,41,45, 46,47,48	**SDRM(1:12)**			Low skew (<250 pS) clock outputs for supporting up to 3 SDRAM modules.
24,25,26, 27,29,30	**PCI (1:6)**			Low skew (<250pS) clock outputs for PCI frequencies. They are synchronous to CPU Clocks.
9	**REF**			Buffered output of the crystal reference.
7	**IOAPIC**			Buffered output of crystal reference. This pin is independently powered up by VDDIO.
22	**48MHz**			Frequency output for USB.
21	**24MHz**			Frequency output for super I/O.
1,10,16, 19,28,37, 42,44	**Vss**			Circuit Ground.
13,15,20, 23,31,32, 43	**Vdd**			Power supply.(3.3Volts)
6	**VDDCPU**			Indepedent power supply for CPU clocks. Can be connected to 3.3V or to 2.5V.
8	**VDDIO**			Indepedent power supply for IOAPIC clock Can be connectec to 3.3V or to 2.5V

A bypass capacitor (0.1mF) should be placed as close as possible to each VDD, VDDCPU, and VDDIO pins. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	-55ºC to +125ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input High Current, Pull- up	IIH	-	-	50	µA	S0-S2 Inputs
Output Low Voltage	VOL	-	-	0.4	Vdc	All Outputs, IOL = 12mA
Output High Voltage	VOH	2.4	-	-	Vdc	All Outputs, IOH = 12mA
Tri-State leakage Current	Ioz	-	-	10	µA	All Outputs
Dynamic Supply Current	Icc	-	67	-	mA	CPU = 66.6 MHz, PCI = 33.3 Mhz, No load
Static Supply Current	Icc (PD)	-	200	-	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = 3.3V±5%, TA = 0ºC to +70ºC

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.4V - 2.0V) and Fall (2.0V-0.4V) time	tTLH, tTHL	-	-	1.6	ns	All clock outputs, 30 pf load
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	Measured at 1.5V
Skew,CPU, PCI, SDRAM	tSKEW	-	-	250	ps	Measured at 1.5V
ΔPeriod Cycles, CPU	ΔP	-	-	±250	ps	-
Jitter Absolute, CPU	tjab	-	-	500	ps	-

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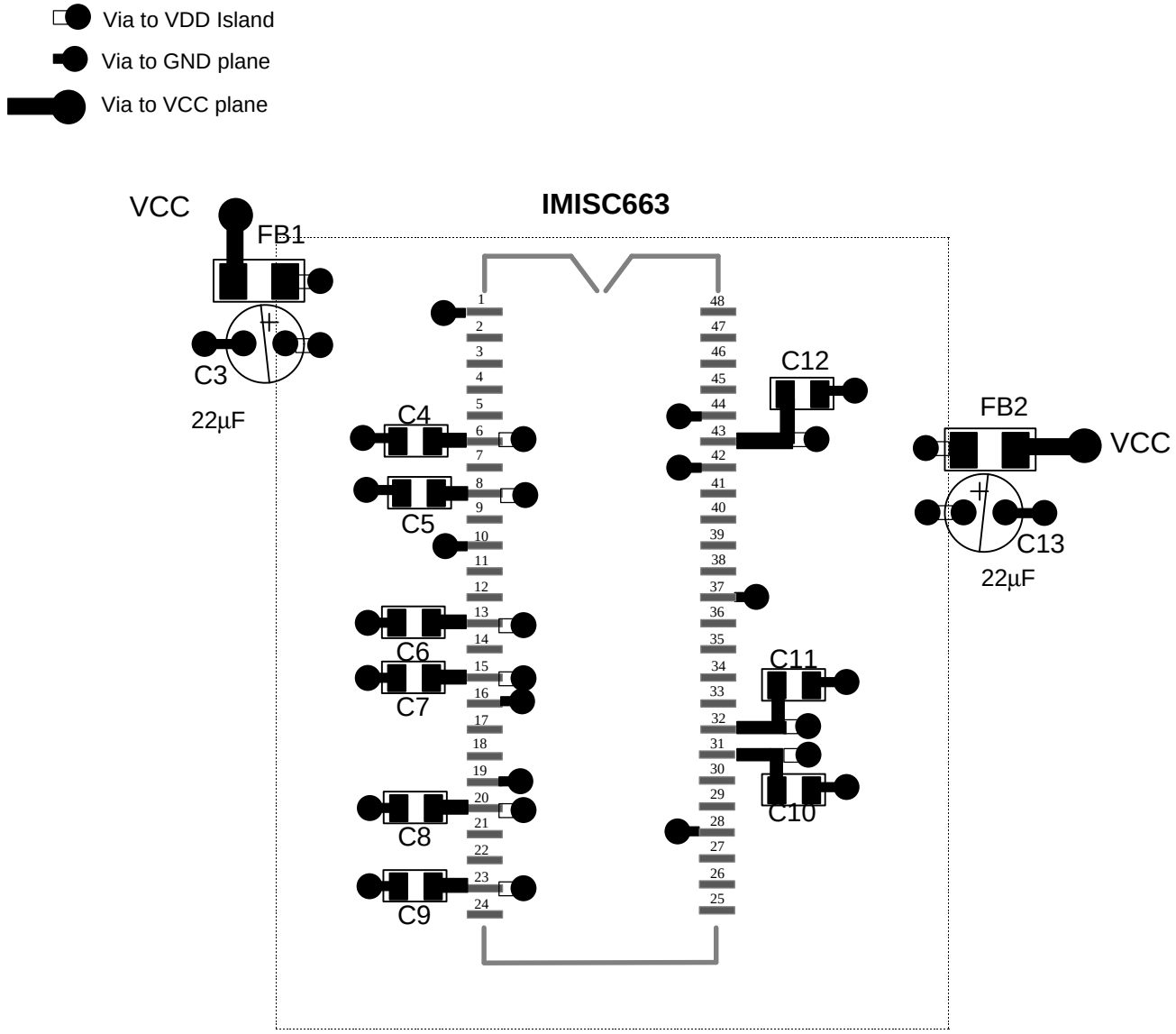
PCB LAYOUT RECOMMENDATION



N1 : This is only a layout recommendation for best performance and lower EMI. The designer may choose a differnent approach but C4, C5, C6, C7, C8, C9, C10, C11, and C12 (all are 0.1µf) should always be used and placed close to their VDD pins.

N2 : If the Clock Gen. is placed in a noisy enviroment, the designer may choose to place all vias to VDD island on the outer side (between Pin and Cap) as on pins 31 and 32. In any case, the trace between Pin and Cap must always be as short as possible.

N3 : For improved current ground return paths, the designer may choose to place 2 vias per Vss pin. This will lower the bounce on the ground return and improves EMI.

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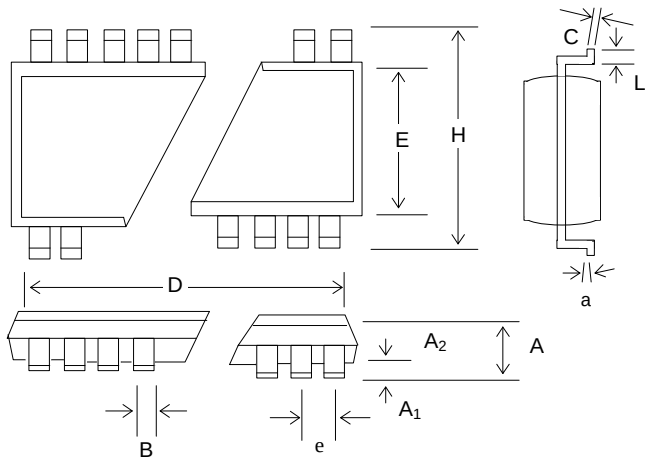
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC663BYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC663BYB
Date Code, Lot #

IMISC663BYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number