I²C System Clock Buffer for Mobile Applications

Approved Product

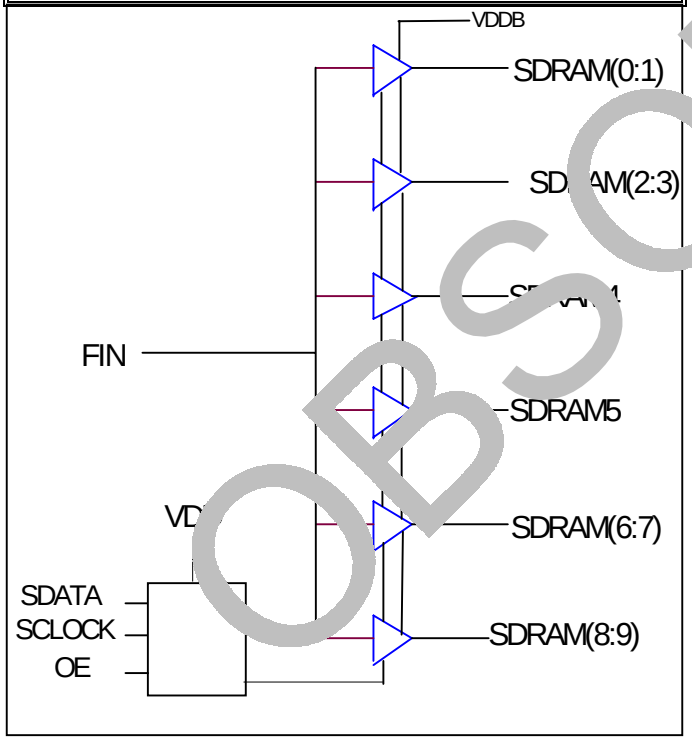
PRODUCT FEATURES

- 10 output buffers for high clock fanout applications
- Each output can be internally disabled for EMI and power consumption reduction.
- Separate power supply for each group of 2 clock outputs for mixed voltage application.
- < 250ps skew between output clocks.
- 28-pin SSOP package for minimum boad space
- Single output Tristate pin for testability

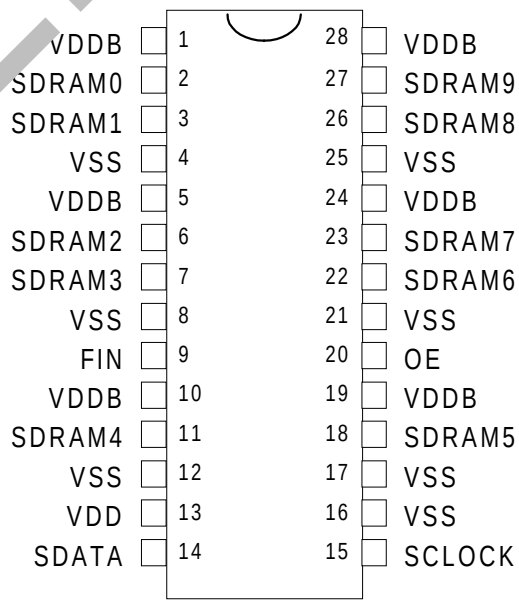
PRODUCT DESCRIPTION

The device is a high fanout system clock distributor. Its primary application is to create the large quantity of clocks needed to support a wide range of clock loads that are referenced to a single existing clock. Loads of up to 30 pF are supported. Primary application of this component is where long traces are used to transport clocks from their generating devices to their loads. The creation of EMI and the degradation of waveform rise and fall times is greatly reduced by running a single reference clock trace to the device and then using it to regenerate the clock that drives shorter traces by using the IMISC660 to generate the clocks at the target device. EMI is therefore minimized and board real estate is saved.

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
9	**FIN**	-	I	PAD	This pin is connected to the input reference clock. This clock must be in the range of 10.0 to 100.0 Mhz.
2,3,6,7,11,18,22,23,26,27	**SDRAM(0:9)**	VDDB	O	BUF1	Low skew output clocks.
20	**OE**	-	I	PAD	Buffer Output Enable pin. This pin is low it is used to place all output clocks (CLK1:10) in a tri state condition. This feature facilitates in production board level testing to be easily implemented for the clocks that this device produces. Has internal pull-up resistor.
14	**SDATA**	VDD	I/O	PAD	Serial Data for I2C control interface. This pin receives data streeams from the I2C bus and outputs an acknowledge for valid data.
15	**SCLOCK**	VDD	I	PAD	Serial Clock for I2C control interface.
4, 8, 12, 16, 17, 21, 25	**VSS**		PWR	-	Ground pins for clock output buffers. These pins must be returned to the same potential to reduce output clock skew.
1, 5, 10, 19, 24, 28	**VDDB**	-	PWR	-	Power for output clock buffers.
13	**VDD**	-	PWR	-	Power for device core logic.

MAXIMUM RATINGS

Voltage Relative to VSS: -0.3

Voltage Relative to VDD: 0.5V

Storage Temperature: -65 to + 150ºC

Operating Temperature: -40 to +85ºC

Maximum Power Supply 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceeding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below desrcibed sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	reserved
6	1	-	reserved
5	1	-	reserved
4	1	-	reserved
3	1	7	SDRAM3 (Active = 1, Forced low = 0)
2	1	6	SDRAM2 (Active = 1, Forced low = 0)
1	1	3	SDRAM1 (Active = 1, Forced low = 0)
0	1	2	SDRAM0 (Active = 1, Forced low = 0)

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SERIAL CONTROL REGISTERS (Cont.)

Byte 1: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	27	SDRAM9 (Active = 1, Forced low = 0)
6	1	26	SDRAM8 (Active = 1, Forced low = 0)
5	1	23	SDRAM7 (Active = 1, Forced low = 0)
4	1	22	SDRAM6 (Active = 1, Forced low = 0)
3	1	-	reserved
2	1	-	reserved
1	1	-	reserved
0	1	-	reserved

Byte 4: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	18	SDRAM (Active = 1, Forced low = 0)
6	0	11	SDRAM (Active = 1, Forced low = 0)
5	0	-	Not Used
4	0	-	Not Used
3	0	-	Not Used
2	0	-	Not Used
1	1	-	Not Used
0	1	-	Not Used

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL	-66			µA	
Input High Current	IIH			66	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd_{66}	-	-	160	mA	Input frequency = 66 Mhz - All outputs on and at 30 pF load
	Idd_{100}	-		220	mA	Input frequency 100 Mhz - All outputs on and at 30 pF load
Static Supply Current	Isdd	-	-		mA	All outputs disabled no input clock
Short Circuit Current	ISC	25	-		mA	1 output at a time - 30 seconds
Input Rise Time	TIR	2.4		-	nS	.8 to 2.4 volts
VDD = VDD1 thru VDD5 =3.3V ±5%, , TA = -40ºC to +85ºC						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle		45	50	55	%	Measured at 1.5V (50/50 in)
Buffer out/out Skew All Buffer Outputs	tSKEW	-	-	250	pS	35 pF Load Measured at 1.5V
Buffer input to output Skew	tSKEW	2.0	4.0	5.0	nS	
Jitter Cycle to Cycle*	TJCC			50	pS	@ 35 pF loading
Jitter Absolute (Peak to Peak)*	TJabs			150	pS	@ 35 pF loading
VDD = VDD1 thru VDD5 = 3.3V ±5%, , TA = -40ºC to +85ºC						

*This jitter is additive to the input clock's jitter.

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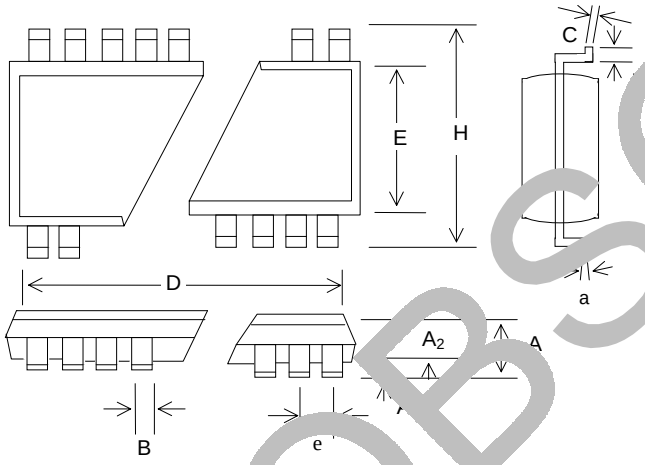
TYPE 1 BUFFER CHARACTERISTICS (ALL CLOCK OUTPUTS)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	30	-	39	mA	Vout =VDD - .5V
Pull-Up Current Max	IOH_{max}	75	-	109	mA	Vout 1.5V
Pull-Down Current Min	IOL_{min}	30	-	40	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	103	mA	Vout = 2.V
Dynamic Output Impedance	Z_O	8	-	15	0hms	6 100 Mhz
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	-	-	1.33	nS	30 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.33	nS	pF Loa
VDD = VDD1 thru VDD5 =3.3V ±5%, , TA = -40°C to +8 C						

PACKAGE DRAWING AND DI EN IONS



28 PIN SOP OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMB	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC660CYB	28 PIN SSOP	Commercial, -40ºC to +85ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC660CYB
Date Code, Lot #

IMISC660CYB

- Flow
  B = Commercial, -40ºC to + 85ºC
- Package
  Y = SSOP
  T = TSSOP
- Revision
- IMI Device Number

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