Clock Generator for 3 DIMM, Pentium Boards

Preliminary Product Information

PRODUCT FEATURES

- Individual I^2C clock stop controls for low power mobile applications and EMI reduction
- Designed to meet Intel[tm] specifications
- Integrated crystal loading capacitors
- Supports Intel Pentium, Pentium Pro, Pentium II, Cyrix and AMD CPU's
- 7 PCI BUS clocks (synchronous or asynchronous)
- <250 pS skew on all CPU/SDRAM clocks
- <500 pS between CPU and PCI clocks
- 2 Ref. Clocks @ 14.31818 MHz, one at VDDC (IOAPIC)
- Separate V_{DDC} for CPUL (1:3) clock buffers and IOAPIC
- Programmable registers for jumperless frequency selection
- 48 Pin SSOP Package

PRODUCT DESCRIPTION

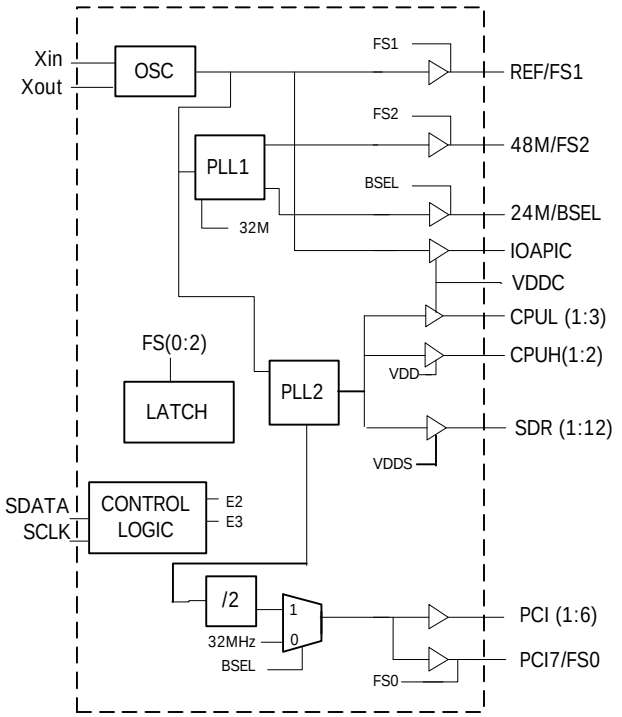
The device is a high fanout EMI reducing system clock generator that provides the large quantity of clocks needed to support the motherboard. Bi-directional I/O pins are provided to maximize the functionality of the device and provide the input control features required for user flexibility.

FREQUENCY TABLE (MHz)

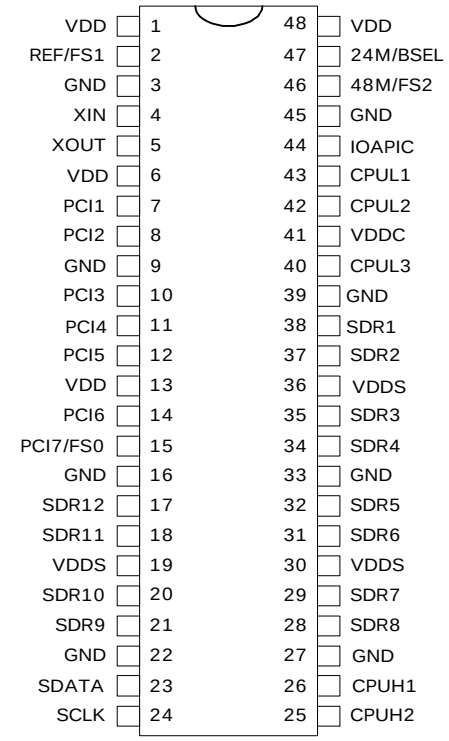
(Functionality with 14.31818 MHz input)

Frequency Select			CPUs	PCI (1:6)	
FS2	FS1	FS0	MHz	BSEL = 1	BSEL = 0
0	0	0	60.0	30.0	32.0.
0	0	1	66.8	33.4	32.0
0	`1	0	50	25.0	32.0
0	1	1	55	27.5	32.0
1	0	0	75	37.5	32.0
1	0	1	68.7	34.4	32.0
1	1	0	83.3	41.7	32.0
1	1	1	Tri-state	Tri-state	Tri-state

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	POWER	I/O	TYPE	Description
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal. Has internal 18 pF crystal loading capacitor.
5	**Xout**	VDD	O	OSC1	On-chip reference oscillator output pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used, this pin is left unconnected. Has internal 18 pF crystal loading capacitor.
40, 42, 43	**CPUL[1:3]**	VDDC	O	BUF1	Clock output. CPU frequency table specified. Power is applied by VddC
38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17	**SDR [1:12]**	VDDS	O	BUF2	Clock output. Low skew copy of the CPU clock used to drive SDRAM clock pins.
25, 26	**CPUH(1:2)**	VDD	O	BUF1	Clock output. Low skew copy of the CPU clock used to drive SDRAM clock pins. Powered is applied by Vdd
7, 8, 10, 11, 12, 14	**PCI [1:6]**	VDD	O	BUF1	Clock output. PCI Bus frequency table specified. Power is applied by VDD Pins.
46	**48M/FS2**	VDD	I/O	BUF 2 PU	Bi-directional pin. During powerup sets the FS2 bit. Afterwards, it is a 48.0 MHz output clock. Has internal pullup.
2	**REF/FS1**	VDD	I/O	BUF4 PU	Bi-directional pin. During powerup sets the FS1 bit. Afterwards, it is a 14.31818 MHz reference output clock. has internal pullup
47	**24M/BSEL**	VDD	I/O	BUF 2 PU	Bi-directional pin. During powerup sets the bus mode (BSEL) bit. Afterwards, it is a 24.0 MHz reference output clock.
15	**PCI7/FS0**	VDD	I/O	BUF3 PU	Bi-directional pin during power up. Its logic level is latched and defines the selection of the frequency table. as FS0. After power up it acts as a PCI clock output as defined by the PCI [1:6] pins.
23	**SDATA**		I	PAD PU	I^2C data input pin Has internal pullup.
24	**SCLK**		I	PAD PU	I^2C clock input pin. Has internal pullup.
1,6, 13, 48	**VDD**		PWR	---	3.3 volt core, PCI clock and fixed clock power.
41	**VDDC**		PWR	---	3.3 or 2.5 volt CPU clock power
19, 30, 36	**VDDS**		PWR	---	3.3 volt power for SDRAM and CPUH buffers
3, 9,16,22, 27,33,39, 45	**GND**		PWR	---	Device ground
44	**IOAPIC**	VDDC	O	BUF4	This is a 14.31818 MHz clock. Its output buffers is supplied by the VDDC and may be as 2.5 volts.

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Selection on Bi-directional Pins

Bi-directional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode and therefore, they are considered input select pins. Internal to the IC, these pins have a large value pull-up each (100KΩ), therefore, a selection "1" is the default. If a selection "0" is desired, then a direct connection to ground through a 10KΩ resistor should be implemented as shown in Fig.3. Please note the selection resistor (10KΩ) is placed before the Damping resistor (Rd) and close to the devices pin.

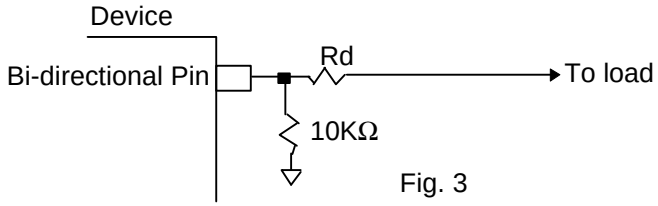

Fig. 3

2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

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SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2, ...) will be valid and acknowledged.

Byte 0: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	*	BSEL (frequency Table Selection via I^2C)
6	1	*	FS2 (frequency Table Selection via I^2C)
5	1	*	FS1 (frequency Table Selection via I^2C)
4	1	*	FS0 (frequency Table Selection via I^2C)
3	0	*	enable frequency selection by hardware (set to 0) or software I^2C (set to 1)
2	x	n/a	Reserved for future Spread Spectrum function
1 0	0 0	* *	Bit 1 Bit 0 1 1 Tri-State 1 0 Reserved for IMI testing function 0 1 Test Mode 0 0 Normal

Function Table

Function Description	Outputs				
	CPU	PCI	SDRAM	REF	IOAPIC
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test (BSEL=1)	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk
Test (BSEL=0)	Tclk/2	Tclk/3	Tclk/2	Tclk	Tclk
Normal	see table	see table	CPU	14.318	14.318

Notes:
1. Tclk is a test clock over driven on the Xin input during test mode.

SERIAL CONTROL REGISTERS (Cont.)

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	46	48 MHz enable/Stopped
6	1	47	24 MHz enable/Stopped
5	x	-	Reserved
4	1	25	CPUH2 enable/Stopped
3	1	26	CPUH1 enable/Stopped
2	1	40	CPUL3 enable/Stopped
1	1	42	CPUL2 enable/Stopped
0	1	43	CPUL1 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	15	PCI7 / FS0 enable/Stopped
5	1	14	PCI6 enable/Stopped
4	1	12	PCI5 enable/Stopped
3	1	11	PCI4 enable/Stopped
2	1	10	PCI3 enable/Stopped
1	1	8	PCI2 enable/Stopped
0	1	7	PCI1 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28	SDRAM8 enable/Stopped
6	1	29	SDRAM7 enable/Stopped
5	1	31	SDRAM6 enable/Stopped
4	1	32	SDRAM5 enable/Stopped
3	1	34	SDRAM4 enable/Stopped
2	1	35	SDRAM3 enable/Stopped
1	1	37	SDRAM2 enable/Stopped
0	1	38	SDRAM1 enable/Stopped

SERIAL CONTROL REGISTERS (Cont.)

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	1	17	SDRAM12 enable/Stopped
2	1	18	SDRAM11 enable/Stopped
1	1	20	SDRAM10 enable/Stopped
0	1	21	SDRAM9 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	1	44	IOAPIC enable/Stopped
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	1	2	REF1/FS1 enable/Stopped

Byte 6: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

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MAXIMUM RATINGS

Maximum Power Supply: 7 V
Vin Relative to VSS: -0.3V to VDD+0.3
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: -55ºC to +125ºC
Maximum Power Dissipation: W
ESD: 12Kv(inputs), 2Kv (outputs)

Note. All Vdd and Vss pins must be connected to their required potentials to avoid device damage

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	All logic inputs
Input High Voltage	VIH	2.0	-	-	Vdc	All logic inputs
Input Low Current	IIL			-66	µA	All logic inputs
Input High Current	IIH			5	µA	All logic inputs
Tri-State leakage Current	Ioz	-	-	10	µA	All logic outputs
Static Supply Current	Isdd			22	mA	CPU = 66.6 Mhz, no clocks loaded
Dynamic Supply Current	Idd	-	-	84	mA	CPU = 66.6 Mhz, all clocks at specified max capacitance
Powered down Supply Current	Ipd		-	128	µA	PD pin at Vss level
Input Capacitance Logic Gates	Cli	3	-	5	pF	All logic input pins
Input Capacitance Xin andXout pins	Cioi, Cioo	5	-	8	pF	Reference Oscillator pins. Effective load to crystal is half this value.

VDD = VDD =3.3 +/- 5%, VDDC = 2.5V +/- 5%, TA = 0ºC to +70ºC

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TIMING CHARACTERISTICS						
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
CPU to CPU Skew	Tskw1	-	-	250	pS	20 pF Load, Measured @ 1.25V
SDRAM to SDRAM Skew	Tskw2	-	-	250	pS	30 pF Load, Measured @ 1.5V
CPU to SDRAM Skew	Tskw3	-	-	500	pS	CPU: 20 pF Load, Measured @ 1.25V SDRAM: 30 pF Load, Measured @ 1.5V
PCI to PCI Skew	Tskw4	-	-	500	pS	30 pF Load, Measured @ 1.5V
CPU to PCI Offset	Toff	1	-	4	nS	CPU: 20 pF Load, Measured @ 1.25V PCI: 30 pF Load, Measured @ 1.5V
Output Duty Cycle	Tdty	45	50	55	%	CPU, IOAPIC: 20 pF Load, Meas. @ 1.25V
Cycle to Cycle Jitter	Tccj	250	-	250	pS	PCI, SDRAM, REF, 48MHz, 24MHz : 30 pF
Long Term Jitter	Tj	-	-	500	pS	Load, Measured @ 1.5V
VDD = VDD =3.3V +/- 5%, VDDC = 2.5V +/- 5%, TA = 0ºC to +70ºC						

BUF1 (CPU clocks)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
pull-up Current	IOH	-27	-	-27	mA	VOH_{min} = 1.0V, VOH_{max} = 2.6
Pull-Down Current	IOL	27	-	27	mA	VOL_{min} = 1.2v, VOL_{max} = 0.3V
Rise/Fall times	Tr, Tf	0.4	-	1.6	nS	20 pF Load, Measured @ 0.4V to 2.0V
Clock High Time	Thi	5	-	-	nS	20 pF Load, Measured @ 2V
Clock Low Time	Tlo	5	-	-	nS	20 pF Load, Measured @ 0.4V
VDD = VDD3 =3.3V +/- 5%, VDDC = 2.5V +/- 5%, TA = 0ºC to +70ºC						

BUF2 (REF and SDRAM clocks)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-46	-	-46	mA	VOH_{min} = 1.0V, VOH_{max} = 2.6
Pull-Down Current	IOL	53	-	53	mA	VOL_{min} = 1.2v, VOL_{max} = 0.3V
Rise/Fall times	Tr, Tf	0.5	-	1.3	nS	35 pF Load, Measured @ 0.4V to 2.0V
Clock High Time	Thi	5	-	-	nS	35 pF Load, Measured @ 2V
Clock Low Time	Tlo	5	-	-	nS	35 pF Load, Measured @ 0.4V
VDD = VDD =3.3V +/- 5%, VDDC = 2.5V +/- 5%, TA = 0ºC to +70ºC						

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BUF3 (PCI clocks)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-33	-	-33	mA	VOH_{min} = 1.0V, VOH_{max} = 2.6
Pull-Down Current	IOL	30	-	38	mA	VOL_{min} = 1.2v, VOL_{max} = 0.3V
Rise/Fall times	Tr, Tf	0.4	-	2.0	nS	20 pF Load, Measured @ 0.4V to 2.0V
Clock High Time	Thi	5	-	-	nS	20 pF Load, Measured @ 2V
Clock Low Time	Tlo	5	-	-	nS	20 pF Load, Measured @ 0.4V
VDD = VDD =3.3V +/- 5%, VDDC = 2.5V +/- 5%, TA = 0ºC to +70ºC						

BUF4 (IOAPIC and fixed clocks)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	-29	-	-29	mA	VOH_{min} = 1.0V, VOH_{max} = 2.6
Pull-Down Current	IOL	28	-	28	mA	VOL_{min} = 1.2v, VOL_{max} = 0.3V
Rise/Fall times	Tr, Tf	0.4	-	1.6	nS	20 pF Load, Measured @ 0.4V to 2.0V
Clock High Time	Thi	5	-	-	nS	20 pF Load, Measured @ 2V
Clock Low Time	Tlo	5	-	-	nS	20 pF Load, Measured @ 0.4V
VDD = VDD =3.3V +/- 5%, VDDC = 2.5V+/- 5%, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	18	-	pF	note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. Typical trace capacitance, for traces less than a inch are 4 pF. with an internal pin capacitance of 5 pF the total parasitic capacitance would be 9 pF. It this instance a27 pF capacitor added to both legs (pins) of the crystal would bring its total load the recommended 18 pF CL pF each leg) .

Note 1: It is recommended but not mandatory chooses a crystal that meets these specifications.

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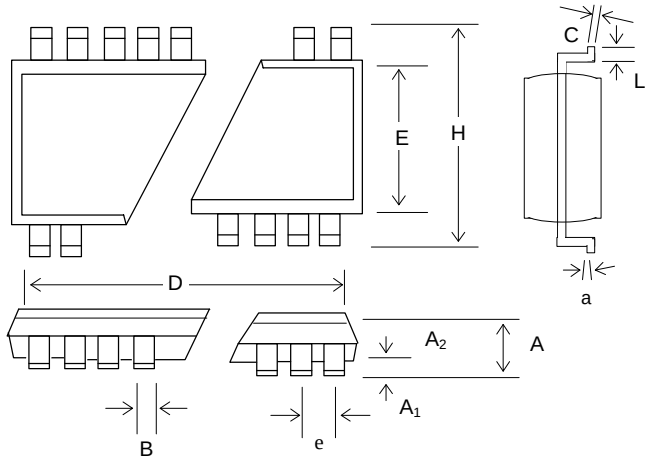
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0º	5º	8º	0º	5º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG654AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening.

Note: Purchase of I^2C components of International Microcircuits, Inc. or one of its sublicensed Associated Companies conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.