

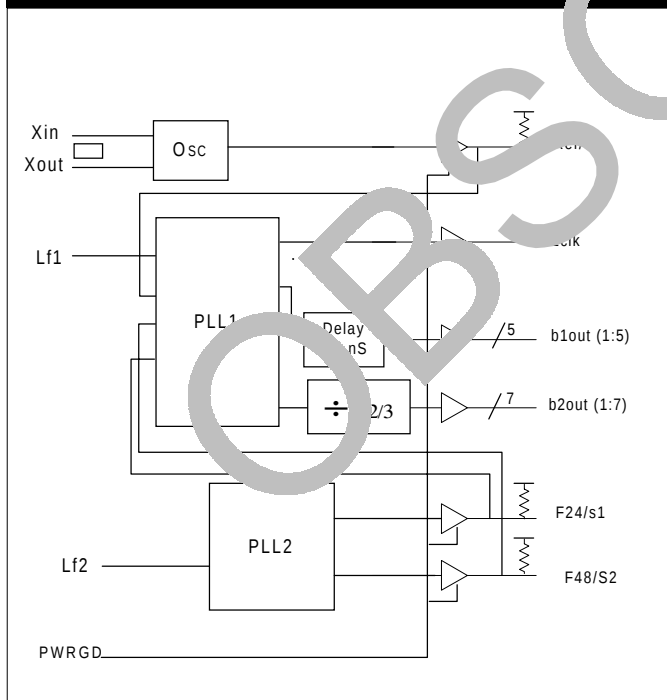
May 1996

PLL FREQUENCY SYNTHESIZER
CMOS LSI

PRODUCT FEATURES

- Supports PCI system board designs P54, P55, and P6
- Integrates system clocks and distribution buffers
- An early host clock, 5 host clocks and 7 PCI clocks
- Supports 5V or 3.3V on ECLK and B1out*
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISC617 provides the clocks and the low skew distribution buffers required to drive the Pentium™ CPU and PCI busses. Selectable delay between ECLK and B1out*. Mixed supply option for P55/54 applications. Fixed 24 and 48 MHz for floppy and U.S.B.

FREQUENCY TABLE

SELECT			OUTPUTS (MHz)	
F24/S2	F24/S1	Ref/S0	ECLK*	B2out*
0	0	0	40	20
0	0	1	75	37.5
0	1	0	40	40
0	1	1	reserved	reserved
1	0	0	50	33.3
1	0	1	50	25
1	1	0	60	30
1	1	1	66.6	33.3

* ECLK = B1out*

APPLICATIONS

60 mA of switching current is provided on all outputs at B1VDD = VDD = 5V.

3.3V operating modes support new low voltage components on the CPU bus. Operating the B1 buffer at 3.3V (B1VDD) and routing the CPU clock through B1 distributes a 3.3V signal to the CPU bus. The outputs provide 30 mA switching current.

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Xin Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

ECLK - Early clock output. This output is synchronous to B1out* clocks and leads by 5 ns typically.

B1out* - Delayed buffered outputs of ECLK.

B2out* - Buffered outputs for PCI bus. Synchronous to ECLK.

F24/S1 - When PWRGD is low this pin is used as an input select line, S1. When PWRGD is high this pin is 24 MHz output. This pin has an internal pull-up.

F48/S2 - When PWRGD is low this pin is used as an input select line, S2. When PWRGD is high this pin is 48 MHz output. This pin has an internal pull-up.

PWRGD - Logic low on this input tristates all outputs. When logic transitions to high, it causes the select data to be latched and the outputs are enabled. This is a Schmitt input with an internal pull-up.

Ref/S0 - When PWRGD is low this pin is used as an input select line, S0. When PWRGD is high this pin is a reference output of the crystal input. This pin has an internal pull-up.

LF1 and LF2 - These are the loop filter pins for the clock generators. A 0.1 μ F capacitor should be connected from each pin to AVSS. Grounding LF puts PLL in low power mode.

VSS - Circuit ground.

VDD - Positive power supply.

AVSS - Analog circuit ground.

AVDD - Analog positive power supply.

B1VDD - 3V/5V logic level control for ECLK and B1out* outputs.

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Voltage Relative to VSS: -0.3V
 Voltage Relative to VDD: 0.3V
 Storage Temperature: -65°C to 150°C
 Ambient Temperature: -55°C to +125°C
 Maximum Operating Supply: 6V

application of any voltage higher than the maximum rated voltages to its circuit. For proper operation, Vin and Vout should be constrained to the range:

$$V_{ss} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid

Unused inputs must always be tied to an appropriate logic voltage level (either Vss or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V _{IL}	-	-	0.8	V _{dc}	PWRGD, F12/S2, F24/S1, Ref/S0
Input High Voltage	V _{IH}	2.0	-	-	V _{dc}	
Input Low Current with Pull-up or Pull-down	I _{IL} , I _{IH}	-	-	50	μA	
Output Low Voltage I _{OL} = 6mA	V _{OL}	-	-	0.4	V _{dc}	ECLK and B1out*
Output High Voltage I _{OH} = 6mA	V _{OH}	2.4	-	-	V _{dc}	
Output Low Voltage I _{OL} = 12mA	V _{OL}	-	-	0.4	V _{dc}	All other outputs
Output High Voltage I _{OH} = 12mA	V _{OH}	2.4	-	-	V _{dc}	
Tri-State leakage Current	I _{OZ}	-	-	10	μA	LF1, LF2, and tristate outputs
Dynamic Supply Current	I _{DD}	-	-	95	mA	ECLK = 50 MHz
Static Supply Current	I _{DD}	-	300	-	μA	LF1 = LF2 = 0, Xin = 1
Short Circuit Current	I _{OS}	25	-	-	mA	1 output at a time - max 30 sec.

VDD=AVDD= 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0°C to 70°C

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SWITCHING CHARACTERISTICS

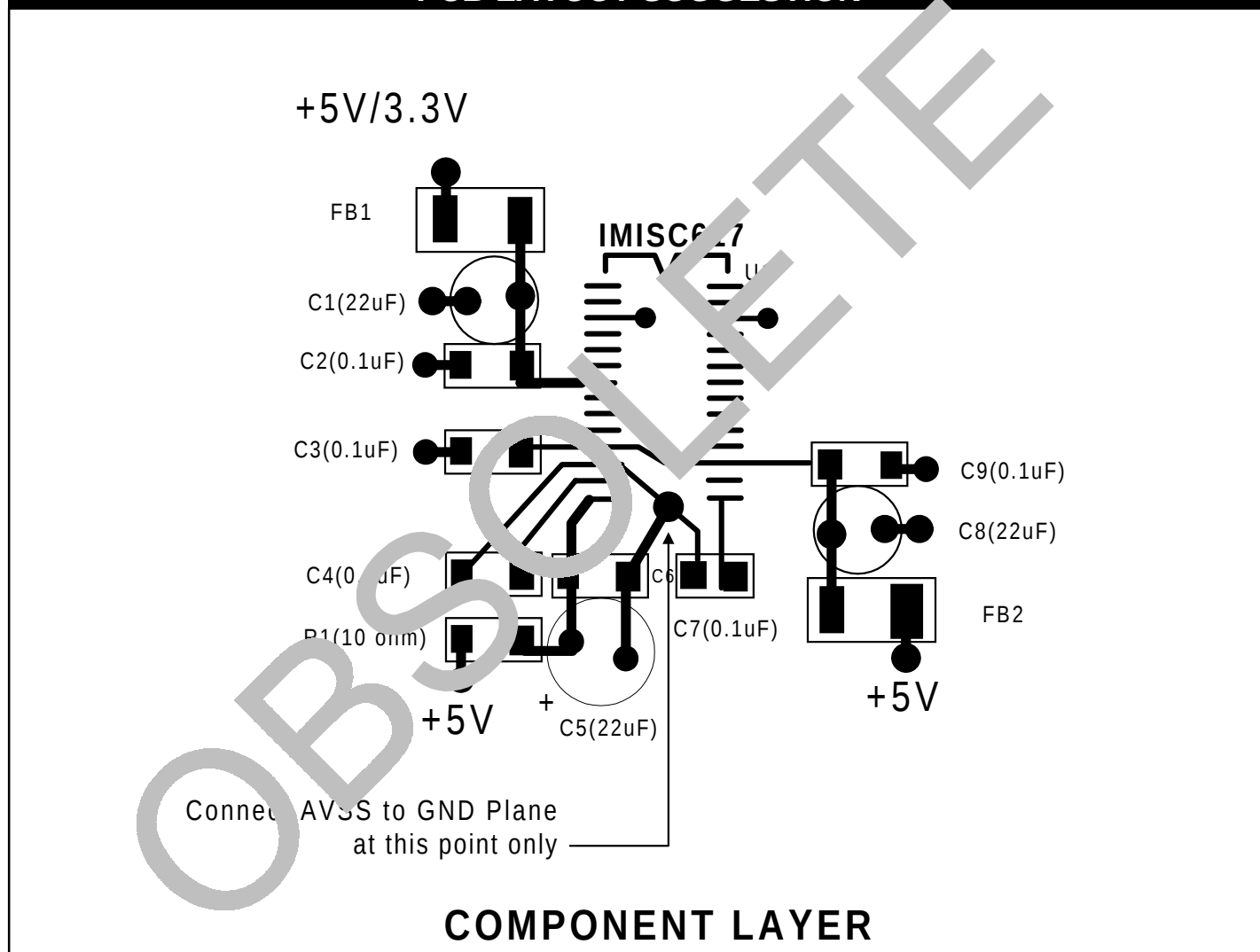
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time	tTLH,	-	-	1.5	nS	15 pF load. B1out* + ECLK
	tTHL	-	-	1.5	nS	15pF load. All other outputs
Output duty cycle		45	50	55	%	Measured at 1.5V, 15 pF load
B1out*-Skew	t1SKW	-	-	250	pS	Measured at 1.5V
B2out*-Skew	t2SKW	-	-	500	pS	Measured at 1.5V
B1out* - B2out*		1	-	4	nS	Measured at 1.5V
ECLK to B1out* Offset2	tOFF	4	5.5	6.2		Measured at 1.5V.
ΔPeriod Adjacent Cycles	ΔP	-	-	200	nS	Measured at 1.5V on ECLK
Jitter Absolute	tjab	-	± 100	-	pS	Measured at 1.5V on ECLK
VDD=AVDD = 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0°C to 70°C						

*See Application Note for implementation

CONNECTION DIAGRAMS

Xin	☐ 1	28	☐ Ref/S0
Out	☐ 2	27	☐ F24/S1
VSS	☐ 3	26	☐ VSS
ECLK	☐ 4	25	☐ B2out1
B1out1	☐ 5	24	☐ B2out2
B1out2	☐ 6	23	☐ B2out3
B1vdd	☐ 7	22	☐ F48/S2
B1out3	☐ 8	21	☐ B2out4
B1out4	☐ 9	20	☐ B2out5
B1out5	☐ 10	19	☐ B2out6
VDD	☐ 11	18	☐ B2out7
AVSS	☐ 12	17	☐ VDD
Lf1	☐ 13	16	☐ PWRGD
AVDD	☐ 14	15	☐ Lf2

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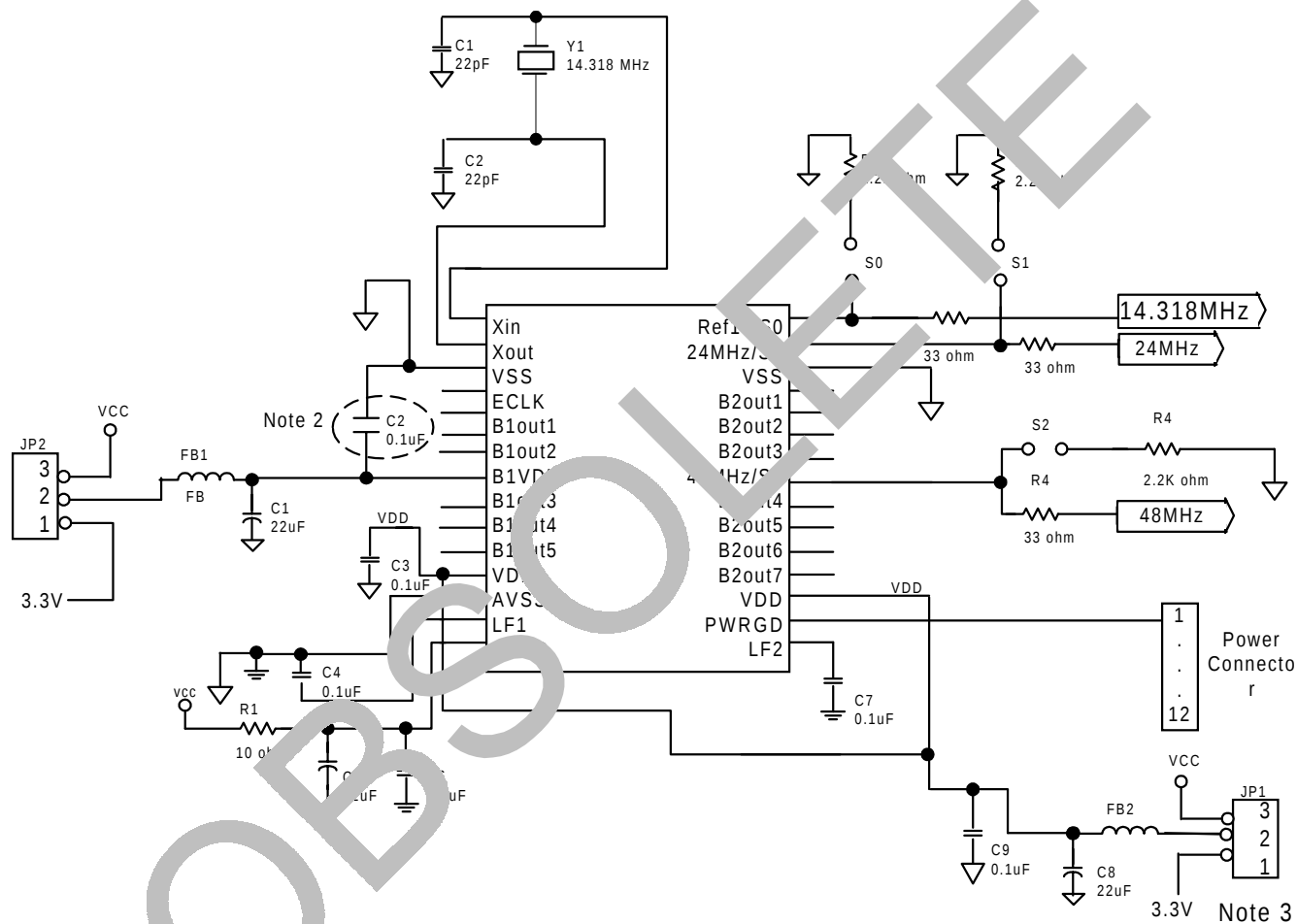
PLL FREQUENCY SYNTHESIZER
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1. Power supply bypass caps (0.1μF and 22 μF) must be positioned close to VDD pins to be effective.
2. LF caps must be low leakage, such as multilayer ceramic Z5U or X7R material.

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APPLICATION SUGGESTION (Update)

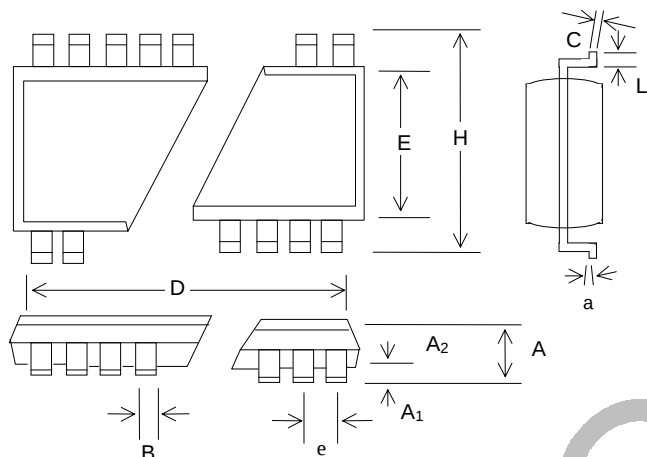


1. All Bypass caps must be as close as possible to their VDD, AVDD, and B1VDD pins.

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PACKAGE DRAWING AND DIMENSIONS



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.060	0.073	0.085	1.73	1.86	1.99
A ₁	0.002	0.005	0.008	0.05	0.13	0.21
A ₂	0.066	0.069	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC617AYB	28 PIN SSOP	Commercial, 0°C to 70°C

Marking: IMI

SC617AYB

Date Code Lot #

IMISC617AYB

Flow

B = Commercial, 0°C to 70°C

Package

SSOP

Revision

IMI Device Number