T1 / E1 / J1 OCTAL FRAMER

PRELIMINARY
BRIEF DATA SHEET
IDT82V2108

FEATURES

- Eight framers in a single chip supporting T1, E1, J1 or unframed data receive and transmit.
- System interface compatible with Mitel ST bus, AT&T CHI bus and MVIP PCM bus. Supports data rates of 1.544 /2.048/8.192 Mb/s on system side. Up to four links can be byte interleaved on one system bus in both transmit and receive direction.
- Provides three duplex HDLC controllers for each framer in E1 mode and two duplex HDLC controllers for each framer in T1/J1 ESF mode. Supports the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces as per ITUT standards. Each HDLC controller has a 128 byte deep FIFO in both the transmit and receive direction.
- Provides jitter attenuation in both transmit and receive paths for each framer.
- Provides per channel/timeslot payload loop-back, per link diagnostic loop-back and per line loop-back.
- Provides a programmable pattern generator/detector to generate/detect common pseudo-random (as ITUT-T O.151) or repetitive sequences in the entire frame (T1, E1 or J1) or on a fractional T1/E1/J1 basis in both the transmit and receive directions. The pattern can also be inserted/detected in only the 7 most significant bits to support Nx56 kbs T1 mode. One programmable generator/detector is shared by all eight framers.
- Provides signaling insertion / extraction for CCS / CAS and RBS signaling system.
- Provides programmable idle code substitution, data and sign inversion, and A-law/μ-law digital milli-watt code insertion on per channel/timeslot basis.
- Detects and integrates Red Alarm, Yellow Alarm and AIS.
- Transmit Yellow Alarm signal or AIS automatically or manually.
- Provides performance monitoring counters to count CRC errors, framing bit errors, loss of frame events and change of frame alignment events.
- Detects mimic framing patterns.
- Provides programmable in-band loop-back code generator/detector and bit-oriented message transmitter/receiver.
- Supports multiplexed / non-multiplexed 8-bit MCU interface for configuration, control and status monitoring.
- JTAG boundary scan meets IEEE 1149.1.
- Low power 3.3V CMOS technology with 5V tolerant.
- Operating industrial temperature range: -40°C to +85°C
- Package available: 128 pin PQFP (14mm by 20mm)
  144 pin PBGA (11mm by 11mm)

APPLICATIONS

- High density internet E1 or T1/J1 interface for routers, multiplexers, switches and digital modems.
- Frame relay switches and access devices (FRADS)
- SONET / SDH add drop multiplexers
- Digital private branch exchanges (PBX)
- Channel service units (CSU) and data service units (DSU)
- Channel banks and multiplexers
- Digital access and cross-connect systems (DACS)

STANDARDS

E1 MODE:

ITU-T: G.704, G.706, G.802, G.737, G.738, G.739, G.742, G.823, G.964, G.965, I.431, O.151, O.152, O.153;
ETSI: ETS 300 011, ETS 300 233, ETS 324-1, ETS 347-1, TBR 4, TBR 12, TBR 13;
GO - MVIP

T1 / J1 MODE:

ANSI: T1.107, T1.231, T1.403, T1.408;
TR: TSY-000147, TSY-000191, NWT-000303, TSY-000312, TSY-000-499;
AT&T: TR 54016, TR 62411
TTC: JT-G 704, JT-G706, JT-G 1431

DESCRIPTION

The IDT82V2108 is a flexible feature-rich octal T1/E1/J1 Framer. Controlled by the software, the IDT82V2108 can be globally configured as an Octal E1 or T1/J1 Framer. When E1 or T1/J1 has been set globally, the operation mode of each of the eight framers can be configured independently. The configuration is performed through a parallel Multiplexed/Non-Multiplexed microprocessor interface.

The IDT82V2108 performs frame synchronization, frame composing, signaling extraction and insertion, alarm and test signals generation and detection in a single chip. It also integrates up to three HDLC receivers and HDLC transmitters for each of the eight framers.

In E1 Mode, the receive path of each framer can be configured to frame to Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be bypassed (unframed mode). It detects and indicates the event of out of Basic Frame Sync, out of CRC Multi-Frame, out of Signaling Multi-Frame, the Remote Alarm Indication signal and the Remote Signaling Multi-Frame Alarm Indication signal. It also monitors the Red and AIS alarms. Basic Frame Alignment Signal errors, Far End Block Errors (FEBE) and CRC errors are counted for performance monitoring. Up to three HDLC links are provided to extract the HDLC message on TS16, the Sa National bits and/or any arbitrary timeslot. Elastic Store Buffers can be used to support slip buffering and adaptation to backplane timing is provided. In E1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, trunk conditioning, data inversion and pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, the transmit path of each framer can be configured to generate Basic Frame, CRC Multi-Frame and Signaling Multi-Frame. The framing can also be disabled (unframed mode). It can also transmit Remote Alarm Indication signal, the Remote Signaling Multi-Frame Alarm Indication signal, AIS signal and FEBE. Up to three HDLC links are provided to insert the HDLC message on TS16, the Sa National bits and/or any arbitrary timeslot. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-timeslot basis.

In E1 mode, any four of the eight framers can be multiplexed or de-multiplexed to or from one of the two 8.192M bit/s buses.

In T1/J1 mode, the receive path of each framer can be configured to frame to Super Frame (SF) or Extended Super Frame (ESF) formats. The framing can also be bypassed (unframed mode). It detects and indicates the out of SF/ESF sync event, the presence of mimic framing pattern, the Yellow Alarm, Red Alarm and AIS. It also detects the presence of inband loopback codes, ESF bit oriented code. Frame Alignment Signal errors, CRC errors, out of SF/ESF events and Frame Alignment position changes are counted for performance monitoring. Two duplex HDLC links are provided to extract the HDLC message on the F-bit or any arbitrary channels for ESF mode. Elastic Store Buffers can be used to support slip buffering and adaptation to backplane timing is provided. In T1/J1 receive path, signaling debounce, signaling freezing, idle code substitution, digital milliwatt code insertion, idle code insertion, data inversion and pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the transmit path of each framer can be configured to generates SF or ESF. The framing can also be disabled (unframed mode). It can also transmit Yellow Alarm signal and AIS signal. Inband loopback codes and ESF bit oriented code can also be transmitted. Two HDLC links are provided to insert the HDLC message on the F-bit or any arbitrary channels for ESF mode. The signaling insertion, idle code substitution, data insertion, data inversion and test pattern generation or detection are also supported on a per-channel basis.

In T1/J1 mode, the data stream of 1.544M bit/s can be converted to/from the data stream of 2.048M bit/s on the system side by software configuration. In addition, any four of the eight framers can be multiplexed or de-multiplexed to or from one of the two 8.192M bit/s buses.

FUNCTIONAL BLOCK DIAGRAM

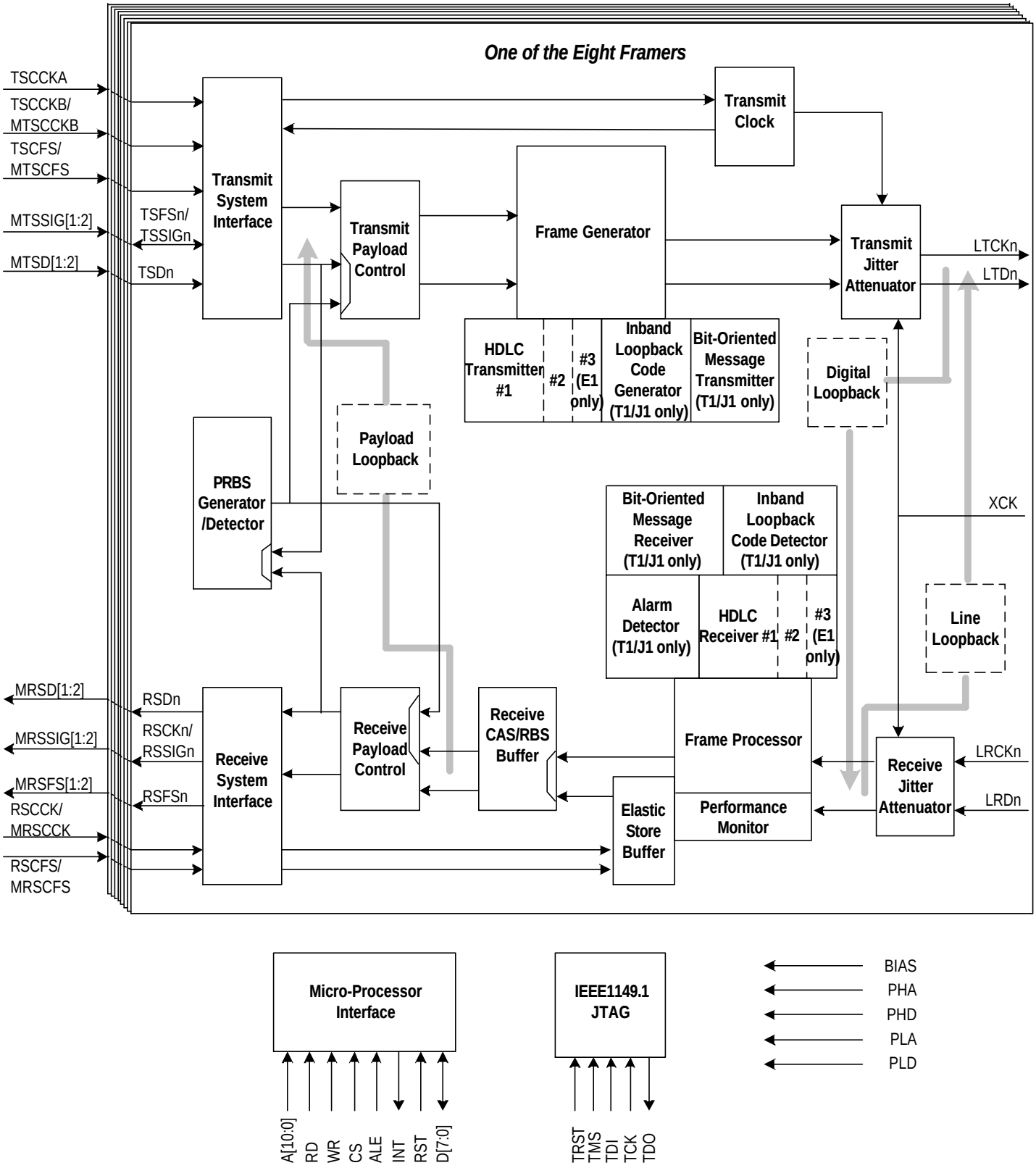


Figure - 1. Block Diagram

PIN ASSIGNMENTS

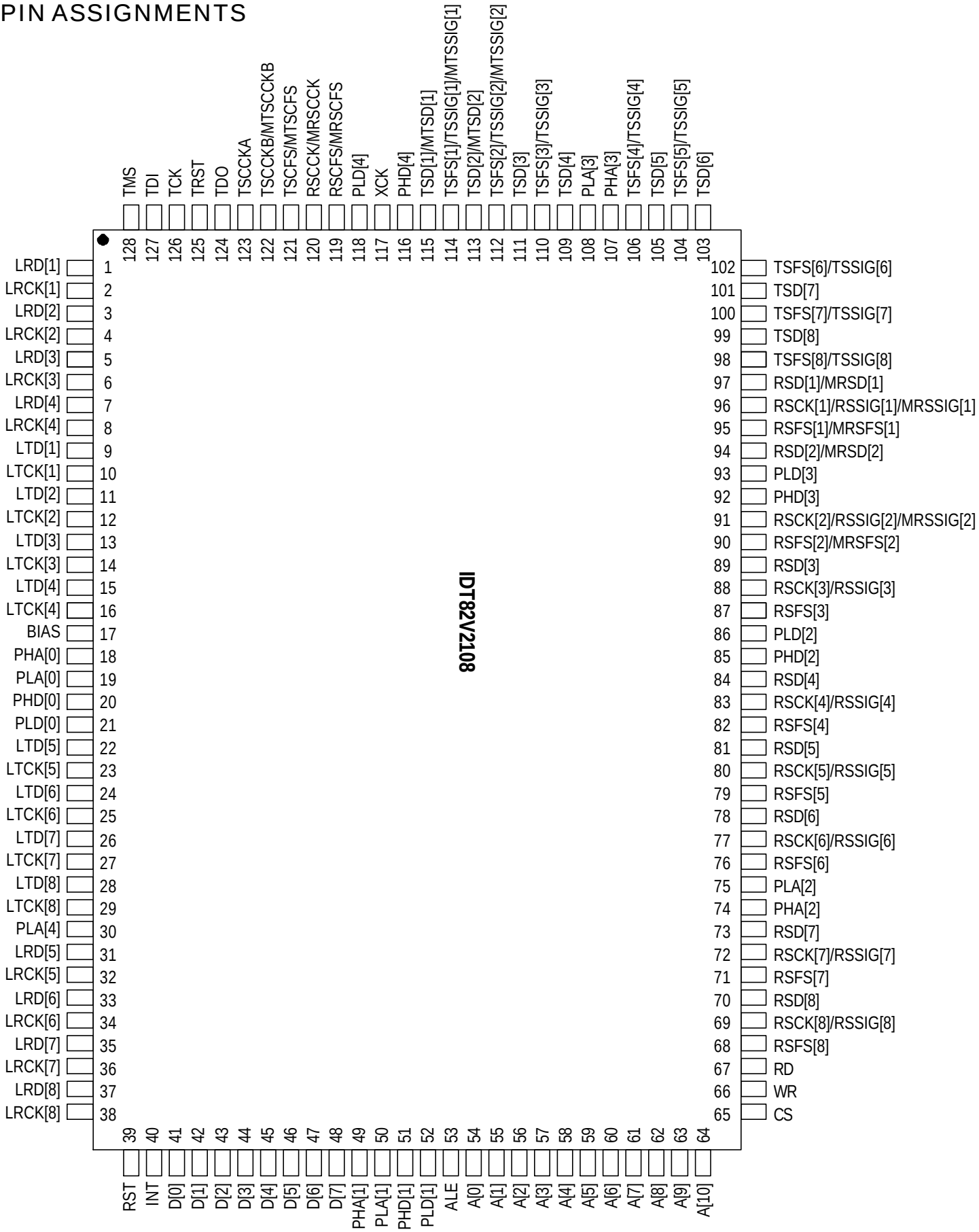


Figure - 2a. 128 Pin PQFP Package Pin Assignment (Top View)

PIN ASSIGNMENTS (CONTINUED)

	12	11	10	9	8	7	6	5	4	3	2	1	
A	TSD[7]	TSD[6]	TSFS[4]/ TSSIG[4]	PLD[4]	TSD[3]	TSFS[1]/ TSSIG[1]/ MTSSIG[1]	PHD[3]	RSCCK/ MRSCCK	TSCCKA	TCK	LRD[1]	LRD[3]	A
B	RSD[1]/ MRSD[1]	TSD[8]	TSFS[6]/ TSSIG[6]	TSD[5]	TSFS[2]/ TSSIG[2]/ MTSSIG[2]	TSD[1]/ MTSD[1]	XCK	RSCFS/ MRSCFS	TSCCKB/ MTSCCKB	TMS	LRD[2]	LRD[4]	B
C	RSD[2]/ MRSD[2]	RSCK[1]/ RSSIG[1]/ MRSSIG[1]	TSFS[8]/ TSSIG[8]	TSFS[7]/ TSSIG[7]	PHD[4]	TSFS[3]/ TSSIG[3]	PLD[3]	TSCFS/ MTSCFS	TDO	LRCK[1]	LRCK[3]	LTCK[1]	C
D	RSCK[2]/ RSSIG[2]/ MRSSIG[2]	RSFS[2]/ MRSFS[2]	PHA[3]	RSFS[1]/ MRSFS[1]	TSFS[5]/ TSSIG[5]	TSD[4]	TSD[2]/ MTSD[2]	TRST	TDI	LRCK[2]	LTD[1]	LTCK[2]	D
E	RSCK[3]/ RSSIG[3]	RSFS[3]	RSD[3]	PLA[4]	PHD[5]	PHD[6]	PHD[7]	PHD[8]	LRCK[4]	LTD[2]	LTCK[4]	LTD[4]	E
F	RSD[4]	PHD[2]	PLD[2]	RSD[5]	PHD[9]	PHD[10]	PHD[11]	PHD[12]	LTD[3]	LTCK[3]	PLA[0]	PHA[0]	F
G	RSFS[4]	RSCK[4]/ RSSIG[4]	RSD[6]	RSCK[6]/ RSSIG[6]	PLD[5]	PLD[6]	PLD[7]	PLD[8]	BIAS	LTD[5]	PLD[0]	PHD[0]	G
H	RSFS[5]	RSCK[5]/ RSSIG[5]	PLA[3]	RSCK[7]/ RSSIG[7]	PLD[9]	PLD[10]	PLD[11]	PLD[12]	LTCK[8]	LTCK[6]	LTCK[5]	LTD[6]	H
J	RSFS[6]	RSD[7]	RSFS[8]	A[9]	A[7]	PHA[1]	D[4]	INT	LRD[5]	LTD[8]	LTD[7]	LTCK[7]	J
K	PHA[2]	RSD[8]	WR	A[6]	A[3]	A[0]	D[5]	D[2]	LRCK[7]	LRCK[6]	LRCK[5]	PLA[1]	K
L	RSFS[7]	RD	A[10]	A[4]	A[1]	ALE	PHD[1]	D[7]	D[0]	LRCK[8]	LRD[7]	LRD[6]	L
M	RSCK[8]/ RSSIG[8]	CS	A[8]	A[5]	A[2]	PLD[1]	PLA[2]	D[6]	D[3]	D[1]	RST	LRD[8]	M
	12	11	10	9	8	7	6	5	4	3	2	1	

Figure - 2b. 144 Pin PBGA Package Pin Assignment (Bottom View)

PIN DESCRIPTION

Name	Type	Pin No.		Description
		PQFP	PBGA	
Line and System Interface				
LRD[1] LRD[2] LRD[3] LRD[4] LRD[5] LRD[6] LRD[7] LRD[8]	Input	1 3 5 7 31 33 35 37	A2 B2 A1 B1 J4 L1 L2 M1	**LRD[1:8]: Line Receive Data for Framer 1 ~ 8** These pins receive the data stream from line interface units or from a higher demultiplex interface. Data on these pins are sampled in on the active edge of the corresponding LRCKn.
LRCK[1] LRCK[2] LRCK[3] LRCK[4] LRCK[5] LRCK[6] LRCK[7] LRCK[8]	Input	2 4 6 8 32 34 36 38	C3 D3 C2 E4 K2 K3 K4 L3	**LRCK[1:8]: Line Receive Clock for Framer 1 ~ 8** These pins receive externally recovered line clock (2.048 or 1.544MHz). The clock is used to sample the data on the corresponding LRDn. The clock may be gapped clock.
RSCK[1]/RSSIG[1]/ MRSSIG[1] RSCK[2]/RSSIG[2]/ MRSSIG[2] RSCK[3]/RSSIG[3] RSCK[4]/RSSIG[4] RSCK[5]/RSSIG[5] RSCK[6]/RSSIG[6] RSCK[7]/RSSIG[7] RSCK[8]/RSSIG[8]	Output	96 91 88 83 80 77 72 69	C11 D12 E12 G11 H11 G9 H9 M12	**RSCK[1:8]: Receive Side System Clock for Framer 1 ~ 8** In Receive Clock Master Full E1 or T1/J1 mode, the clock is a smoothed version of the corresponding 2.048 or 1.544 MHz Line Receive Clock (LRCK). The RSCKn is pulsed for each bit in the 256-bit or 193-bit frame. The corresponding RSFSn and RSDn are updated on the active edge of the RSCKn. (refer to Figure – 3). In Receive Clock Master Nx64K mode, the clock is a gapped version of the associated smoothed LRCKn. The number of the RSCKn pulses is controllable from 0 to 255 or from 0 to 192 pulses per frame on a per-timeslot/channel basis. The corresponding RSFSn and RSDn are updated on the active edge of the RSCKn. (refer to Figure – 4) In Receive Clock Slave RSCK Reference mode, the RSCKn can be selected to be either a 2.048/1.544 MHz jitter attenuated version of the corresponding LRCKn or 8KHz. (refer to Figure – 5) **RSSIG[1:8]: Receive Side System Signaling for Framer 1 ~ 8** In Receive Clock Slave External Signaling mode, the extracted signaling is output on these pins. The signal on these pins is timeslot/channel-aligned with the data output on the corresponding RSDn pin and is updated on the active edge of the RSCCK. The extracted signaling is located in the lower nibble (b4 ~ b7). In E1 mode, the extracted signaling repeats during the entire Signaling Multi-Frame for the same timeslot. In T1/J1 mode, the extracted signaling repeats during the entire SF/ESF for the same channel. (refer to Figure – 6) **MRSSIG[1:2]: Multiplexed Receive Side System Signaling** When the multiplexed bus structure is configured, the extracted signaling data from the selected framers are multiplexed on this pin using a byte-interleaved multiplexing scheme. The data on the MRSSIG[1:2] are updated on the active edge of the MRSCCK. (refer to Figure – 7)
RSD[1]/MRSD[1] RSD[2]/MRSD[2] RSD[3] RSD[4] RSD[5] RSD[6] RSD[7] RSD[8]	Output	97 94 89 84 81 78 73 70	B12 C12 E10 F12 F9 G10 J11 K11	**RSD[1:8]: Receive Side System Data for Framer 1 ~ 8** The processed data stream is output on these pins. (refer to Figure – 3~6) In Receive Clock Master mode, the RSDn is updated on the active edge of the corresponding RSCKn. (refer to Figure – 3,4) In Receive Clock Slave mode, the RSDn is updated on the active edge of the RSCCK. (refer to Figure – 5,6) **MRSD[1:2]: Multiplexed Receive Side System Data** When the multiplexed bus structure is configured, the processed data stream from the selected framers is multiplexed on this pin using the byte-interleaved multiplexing scheme. The data on the MRSD[1:2] are updated on the active edge of the MRSCCK. (refer to Figure – 7)

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin No.		Description
		PQFP	PBGA	
RSFS[1]/MRSFS[1] RSFS[2]/MRSFS[2] RSFS[3] RSFS[4] RSFS[5] RSFS[6] RSFS[7] RSFS[8]	Output	95 90 87 82 79 76 71 68	D9 D11 E11 G12 H12 J12 L12 J10	**RSFS[1:8]: Receive Side System Frame Pulse for Framer 1 ~ 8** In E1 mode, RSFSn can be configured to indicate the beginning of Basic Frame, or CRC Multi-Frame or/and Signaling Multi-Frame for data stream on RSDn. When configured for the Basic Frame, RSFSn will be high during the first bit of each Basic Frame. When configured for CRC Multi-Frame, RSFSn will be high during the first bit of the first frame of the CRC Multi-Frame. When configured for the Signaling Multi-Frame, RSFSn will be high during the first bit of the first frame of the Signaling Multi-Frame. When configured to indicate both Signaling and CRC Multi-Frame, RSFSn will go high on the first bit of the first frame of the Signaling Multi-Frame and low after the first bit of the first frame of the CRC Multi-Frame. In T1/J1 mode, RSFSn can be configured to indicate each F-bit, or every second F-bit, or the first F-bit of every 12-frame SF / every 24-frame ESF, or the first F-bit of every 24 / 48 frames. RSFSn pulse high during the above-mentioned F-bit. In both E1 and T1/J1 mode, when Receive Clock Master mode is active, the RSFSn is updated on the active edge of the corresponding RSCKn (refer to Figure – 3,4); when Receive Clock Slave mode is active, the RSFSn is updated on the active edge of the RSCCK (refer to Figure – 5,6). **MRSFS[1:2]: Multiplexed Receive Side System Frame Pulse** When the multiplexed bus structure is configured, the signals on these pins indicate the beginning of a multiplexed frame. The MRSFS[1:2] are updated on the active edge of the MRSCCK. (refer to Figure – 7)
RSCCK/MRSCCK	Input	120	A5	**RSCCK: Receive Side System Common Clock** RSCCK is used only in Receive Clock Slave mode. In E1 mode, it is a 2.048 or 4.096 MHz clock; In T1 mode, it is a 1.544 or 2.048 or 4.096 MHz clock. In Receive Clock Slave RSCK Reference mode, the RSDn and the RSFSn are updated and the RSCFS is sampled on the active edge of the RSCCK (refer to Figure – 5). In Receive Clock Slave External Signaling mode, the RSDn, the RSFSn and the RSSIGn are updated and the RSCFS is sampled on the active edge of the RSCCK (refer to Figure – 6). **MRSCCK: Multiplexed Receive Side System Common Clock** When the multiplexed bus structure is configured, MRSCCK is an 8.192 or 16.384 MHz clock for the receive system multiplexed bus. The MRSCFS is sampled and the MRSD[1:2], the MRSFS[1:2] and the MRSSIG[1:2] are updated on the active edge of the MRSCCK. (refer to Figure – 7)
RSCFS/MRSCFS	Input	119	B5	**RSCFS: Receive Side System Common Frame Pulse** In Receive Clock Slave mode, RSCFS can be selected as a frame alignment reference. It is asserted on the request of each Basic Frame or each Multi-Frame in E1 mode, or it is asserted on the request of F-bit in T1/J1 mode. The RSCFS is sampled on the active edge of the RSCCK. (refer to Figure – 5,6) **MRSCFS: Multiplexed Receive Side System Common Frame Pulse** When the multiplexed bus structure is configured, the signal on this pin aligns the multiplexed frame to the backplane timing. The MRSCFS is sampled on the active edge of the MRSCCK. (refer to Figure – 7)
TSD[1]/MTSD[1] TSD[2]/MTSD[2] TSD[3] TSD[4] TSD[5] TSD[6] TSD[7] TSD[8]	Input	115 113 111 109 105 103 101 99	B7 D6 A8 D7 B9 A11 A12 B11	**TSD[1:8]: Transmit Side System Data for Framer 1 ~ 8** The data stream from the system backplane is input on these pins. In Transmit Clock Master mode, the TSDn is updated on the active edge of the corresponding LTCKn. (refer to Figure – 8) In Transmit Clock Slave mode, the TSDn is updated on the active edge of the TSCCKB. (refer to Figure – 9,10) **MTSD[1:2]: Multiplexed Transmit Side System Data** When the multiplexed bus structure is configured, the data stream from the backplane is carried on the multiplexed bus for the selected framers. The MTSD[1:2] are sampled on the active edge of the MTSCCKB. (refer to Figure – 11)

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin No.		Description
		PQFP	PBGA	
TSFS[1]/TSSIG[1]/ MTSSIG[1] TSFS[2]/TSSIG[2]/ MTSSIG[2] TSFS[3]/TSSIG[3] TSFS[4]/TSSIG[4] TSFS[5]/TSSIG[5] TSFS[6]/TSSIG[6] TSFS[7]/TSSIG[7] TSFS[8]/TSSIG[8]	Output /Input	114 112 110 106 104 102 100 98	A7 B8 C7 A10 D8 B10 C9 C10	**TSFS[1:8]: Transmit Side System Frame Pulse for Framer 1 ~ 8** In Transmit Clock Master mode, the TSFSn indicates the beginning of each Basic Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. The TSFSn is updated on the active edge of the corresponding LTCKn. (refer to Figure – 8) In Transmit Clock Slave TSFS Enabled mode, the TSFSn indicates the beginning of each Basic Frame or Multi-Frame in E1 mode, or indicates the F-bit of SF/ESF in T1/J1 mode. The TSFSn is updated on the active edge of the TSCCKB. (refer to Figure – 9) **TSSIG[1:8]: Transmit Side System Signaling for Framer 1 ~ 8** In Transmit Clock Slave External Signaling mode, these are the TSSIG inputs. The signaling is located in the lower nibble (b4 ~ b7) and sampled on the active edge of the TSCCKB. In E1 mode, the signaling repeats during the entire Signaling Multi-Frame for the same timeslot. In T1/J1 mode, the signaling repeats during the entire SF/ESF for the same channel. (refer to Figure – 10) **MTSSIG[1:2]: Multiplexed Transmit Side System Signaling** When the multiplexed bus structure is configured, the signaling on the bus is organized in a byte-interleaved scheme for the selected framers. The MTSSIG[1:2] are sampled on the active edge of the MTSCCKB. (refer to Figure – 11)
TSCCKA	Input	123	A4	**TSCCKA: Transmit Side System Common Clock A** TSCCKA is one of the reference clocks for the Tx jitter attenuator DPLL. TSCCKA can be configured to input the clock as: 1. Line rate: 2.048MHz (for E1) or 1.544MHz (for T1); 2. Nx8KHz (N is from 1 to 256) so long as TSCCKA is jitter-free when divided down to 8KHz. (refer to Figure – 8~11) The IDT82V2108 can be configured to ignore the TSCCKA and utilize LRCK and TSCCKB instead. The TSCCKA is replaced by LRCK if line loopback is enabled.
TSCCKB/ MTSCCKB	Input	122	B4	**TSCCKB: Transmit Side System Common Clock B** In E1 mode, the TSCCKB is a 2.048 or 4.096 MHz clock; In T1/J1 mode, the TSCCKB is a 1.544 or 2.048 or 4.096 MHz clock. In Transmit Clock Slave TSFS mode, the TSDn and TSCFS are sampled and the TSFSn is updated on the active edge of the TSCCKB. In Transmit Clock Slave External Signaling mode, the TSDn, TSSIGn and TSCFS are sampled on the active edge of the TSCCKB. (refer to Figure – 8~10) **MTSCCKB: Multiplexed Transmit Side System Common Clock B** When the multiplexed bus structure is configured, MTSCCKB is an 8.192 or 16.384 MHz reference clock for the transmit system multiplexed bus. The MTSCFS, the MTSD[1:2] and the MTSSIG[1:2] are sampled on the active edge of the MTSCCKB. (refer to Figure – 11)
TSCFS/ MTSCFS	Input	121	C5	**TSCFS: Transmit Side System Common Frame Pulse** In Transmit Clock Slave mode, TSCFS is used to frame align all the framers to the system backplane. In E1 mode, the pulse can be configured to indicate the first bit of a Basic Frame, CRC Multi-Frame / Signaling Multi-Frame. In T1/J1 mode, the pulse can be configured to indicate the first bit of SF/ESF. The width of the pulse must be at least 1 TSCCKB cycle wide. The TSCFS is sampled on the active edge of the TSCCKB. (refer to Figure – 9,10) **MTSCFS: Multiplexed Transmit Side System Common Frame Pulse** When the multiplexed bus structure is configured, MTSCFS is used to frame align the multiplexed frames to the system backplane. The MTSCFS is sampled on the active edge of the MTSCCKB. (refer to Figure – 11)

PIN DESCRIPTION (CONTINUED)

Name	Type	Pin No.		Description
		PQFP	PBGA	
LTD[1] LTD[2] LTD[3] LTD[4] LTD[5] LTD[6] LTD[7] LTD[8]	Output	9 11 13 15 22 24 26 28	D2 E3 F4 E1 G3 H1 J2 J3	**LTD[1:8]: Line Transmit Data for Framer 1 ~ 8** These pins output the data stream to line interface units or a higher multiplex interface. The data on the LTDn is updated on the active edge of the corresponding LTCKn.
LTCK[1] LTCK[2] LTCK[3] LTCK[4] LTCK[5] LTCK[6] LTCK[7] LTCK[8]	Output	10 12 14 16 23 25 27 29	C1 D1 F3 E2 H2 H3 J1 H4	**LTCKn: Line Transmit Clock for Framer 1 ~ 8** It is a nominal E1 (2.048MHz) or T1/J1 (1.544MHz) clock. The LTCK can be derived from TSCCKA, TSCCKB, LRCK or XCK. On the active edge of the LTCKn, the corresponding LTDn is updated. (refer to Figure – 8~11)
XCK	Input	117	B6	**XCK: Crystal Clock** The clock frequency equals 49.152MHz ± 50 ppm 50% duty cycle for E1 and 37.056MHz ± 32 ppm 50% duty cycle for T1/J1.
Microprocessor Interface				
RST	Input	39	M2	**RST: Reset (Active Low)** A low signal for at least 100ns on this pin can reset the device anytime. The RST is a Schmitt-trigger input with weak pull-up.
CS	Input	65	M11	**CS: Chip Select (Active Low)** This pin must be asserted low to enable the microprocessor interface. The signal must be asserted high at least once after power up to clear the internal test modes. A transition from high to low must occur on this pin for each Read/Write operation and cannot return to high until the operation is over.
INT	Output	40	J5	**INT: Open-Drain Interrupt Signal (Active Low)** This pin will keep low until all the active unmasked interrupt are acknowledged at their sources.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	54 55 56 57 58 59 60 61 62 63 64	K7 L8 M8 K8 L9 M9 K9 J8 M10 J9 L10	**A[10:0]: Address Bus** The signals on these pins select the register for the microprocessor to access.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	41 42 43 44 45 46 47 48	L4 M3 K5 M4 J6 K6 M5 L5	**D[7:0]: Bi-directional Data Bus** Signals on these pins are the data for Read/Write operation.
RD	Input	67	L11	**RD: Read Strobe (Active Low)** A low signal on this pin enables a read operation on the selected registers.
WR	Input	66	K10	**WR: Write Strobe (Active Low)** A low signal on this pin enables a write operation on the selected registers.

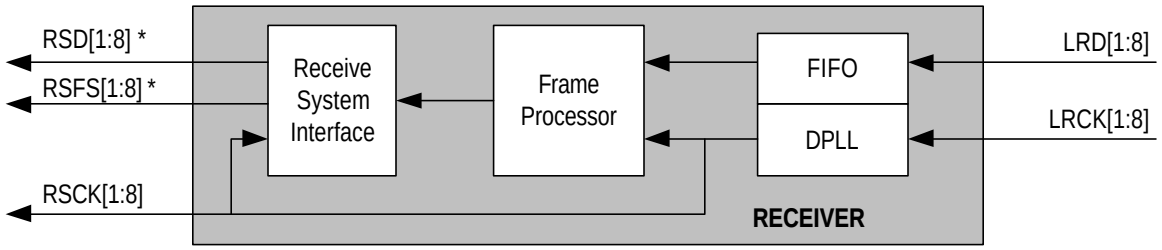
PIN DESCRIPTION (CONTINUED)

Name	Type	Pin No.		Description
		PQFP	PBGA	
ALE	Input	53	L7	**ALE: Address Latch Enable** A low signal on this pin latches the contents of the A[10:0] pins. It can be set when the interface is a multiplexed address/data bus. A high signal on this pin enables the transparence of the A[10:0]. ALE has an integral pull-up.
JTAG Signals (per IEEE P1149.1)				
TRST	Input	125	D5	**TRST: Test Reset (Active Low)** A low signal on this pin can reset the JTAG test port anytime. This pin is a Schmitt-triggered input with an internal pull-up resistor. It must be connected to the RST pin or ground.
TMS	Input	128	B3	**TMS: Test Mode Select** The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edge of the TCK. This pin has an integral pull-up resistor.
TCK	Input	126	A3	**TCK: Test Clock** The clock for the JTAG test is input on this pin. The TDI and the TMS are clocked into the device on the rising edge of the TCK and the TDO is clocked out of the device on the falling edge of the TCK.
TDI	Input	127	D4	**TDI: Test Input** The test data are input on this pin. It is sampled on the rising edge of the TCK. This pin has an integral pull-up resistor.
TDO	Tri-State	124	C4	**TDO: Test Output** The test data are output on this pin. It is sampled on the falling edge of the TCK. This pin is tri-state except the process of scanning of the data.
Supplies and Grounds				
BIAS	Input	17	G4	**BIAS: +5V Bias** This pin enables +5V tolerance on the inputs. When +5V tolerance inputs are required, the BIAS must be connected to a well-decoupled +5V rail through a 1K pull-up resistor and paralleled to the ground through a 0.1μf capacitance. When +3V input is required, the BIAS must be connected to a well-decoupled +3.3V DC supply together with the power pins PHA[4:0] and PHD[3:0]. During power-up and power-down, the voltage on the BIAS pin must be kept ≥ the voltage on the PHA[4:0] and the PHD[3:0] pins to avoid damage to the device.
PHA[0] PHA[1] PHA[2] PHA[3]	Power	18 49 74 107	F1 J7 K12 D10	**PHA[3:0]: Pad Ring Power Pins** These pins must be connected to a common, well-decoupled +3.3V DC supply together with the core power pins PHD[4:0] externally.
PHD[0] PHD[1] PHD[2] PHD[3] PHD[4] PHD[5:12]	Power	20 51 85 92 116 -	G1 L6 F11 A6 C8 E8, E7, E6, E5, F8, F7, F6, F5	**PHD[4:0]: Core Power Pins** These pins must be connected to a common, well-decoupled +3.3V DC supply together with the pad ring power pins PHA[3:0] externally.
PLA[0] PLA[1] PLA[2] PLA[3] PLA[4]	Ground	19 50 75 108 30	F2 K1 M6 H10 E9	**PLA[4:0]: Pad Ring Ground Pins** These pins must be connected to a common ground together with the core ground pins PLD[4:0].

PIN DESCRIPTION (CONTINUED)

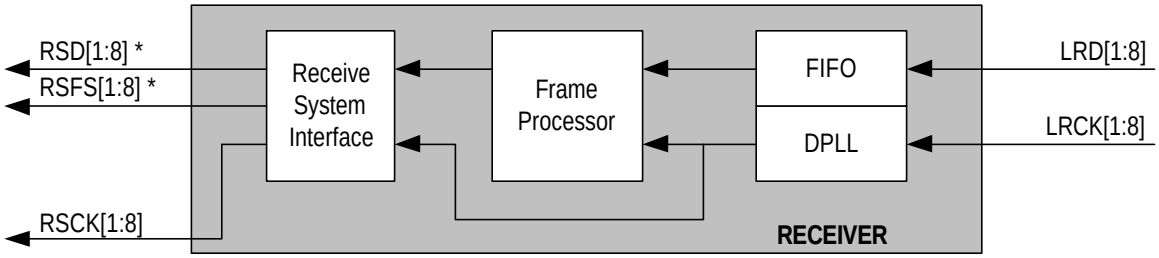
Name	Type	Pin No.		Description
		PQFP	PQFP	
PLD[0] PLD[1] PLD[2] PLD[3] PLD[4] PLD[5:12]	Ground	21 52 86 93 118 -	G2 M7 F10 C6 A9 G8, G7, G6, G5, H8, H7, H6, H5	**PLD[3:0]: Core Ground Pins** These pins must be connected to a common ground together with the pad ring ground pins PLA[4:0].

Notes:
1. All outputs have 4mA drive capability except for the D[7:0], the LTCK[1:8] and the RSCK[1:8] pins which have 6mA drive capability.
2. All input and bi-directional pins present minimum capacitive loading.



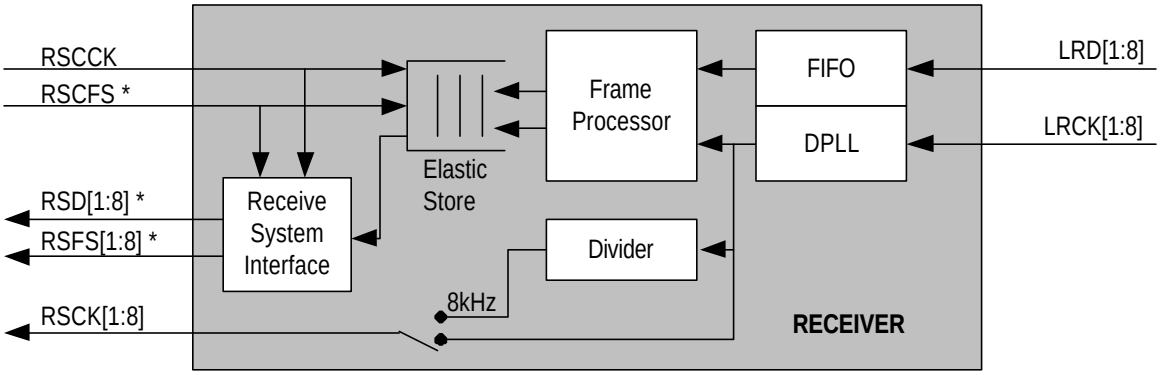
Note: * RSD, RSFS are timed to RSCK

Figure - 3. Receive Clock Master Full E1 or T1/J1 Mode



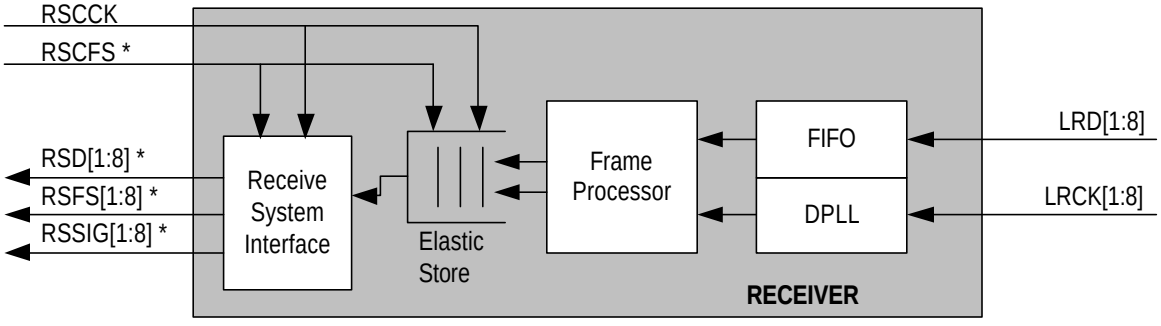
Note: * RSD, RSFS are timed to gapped RSCK

Figure - 4. Receive Clock Master Nx64k Mode



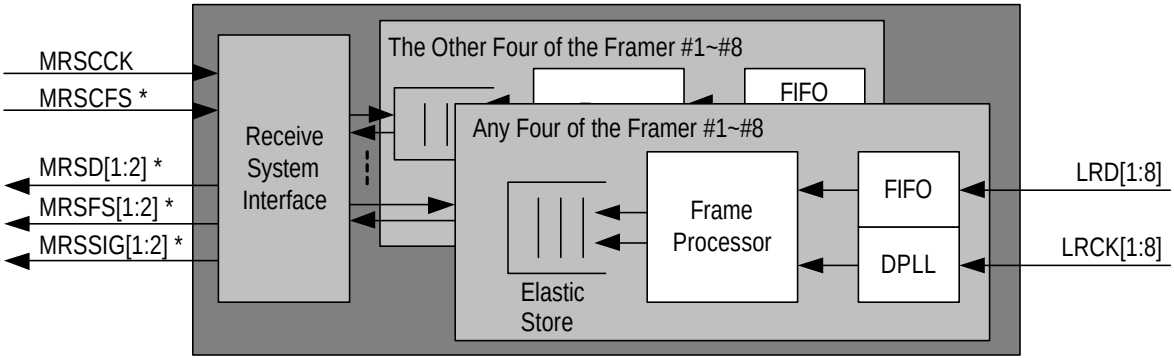
Note: * RSCFS, RSD, RSFS are timed to RSCCK

Figure - 5. Receive Clock Slave RSCK Reference Mode



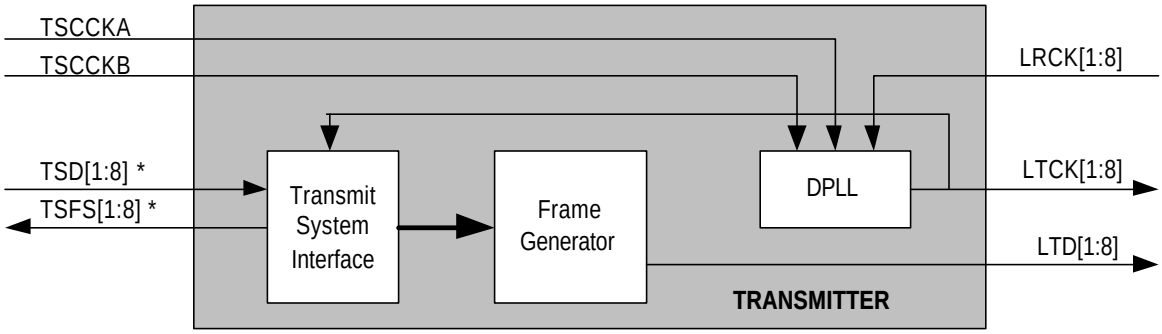
Note: * RSCFS, RSD, RSSIG, RSFS are timed to RSCCK

Figure - 6. Receive Clock Slave External Signaling Mode



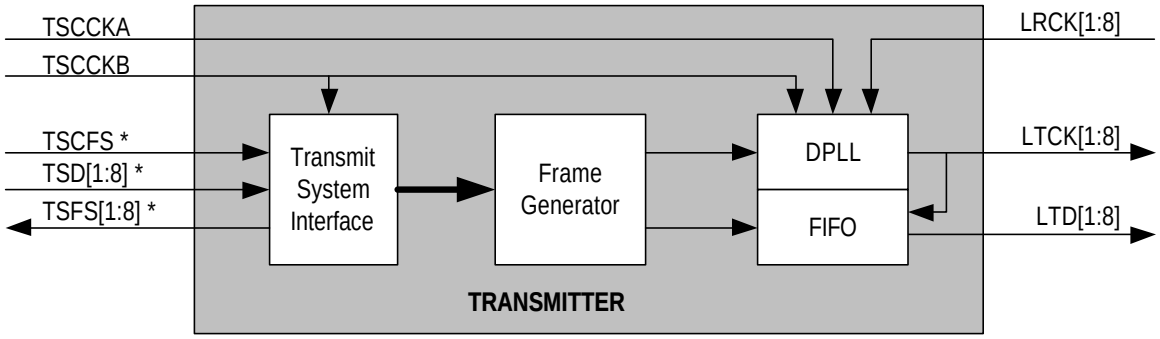
Note: * MRSCFS, MRSD, MRSFS, MRSSIG are timed to MRSCCK

Figure - 7. Receive Multiplexed Mode



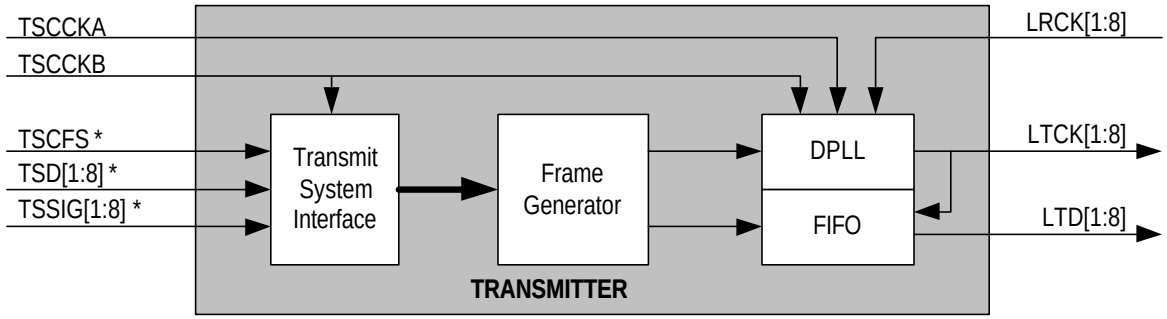
Note: * TSD, TSFS are timed to LTCK

Figure - 8. Transmit Clock Master Mode



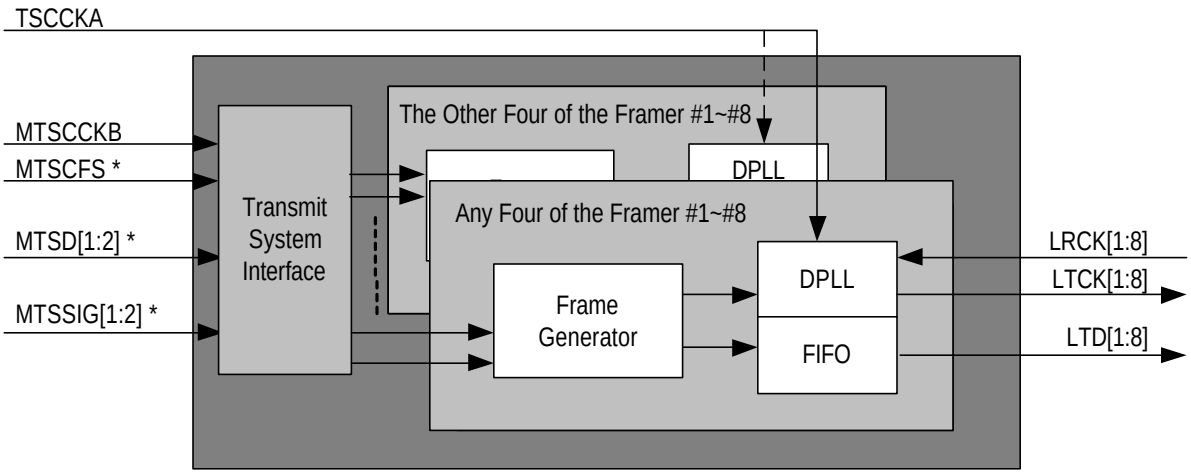
Note: * TSCFS, TSD, TSFS are timed to TSCCKB

Figure - 9. Transmit Clock Slave EFP Enable Mode



Note: * TSCFS, TSD, TSSIG are timed to TSCCKB

Figure - 10. Transmit Clock Slave External Signaling Mode



Note: * MTSCFS, MTSD, MTSSIG are timed to MTSCCKB

Figure - 11. Transmit Multiplexed Mode