IMISC609 SYSTEM CLOCK CHIP

December 1995

CMOS LSI
PLL FREQUENCY SYNTHESIZER

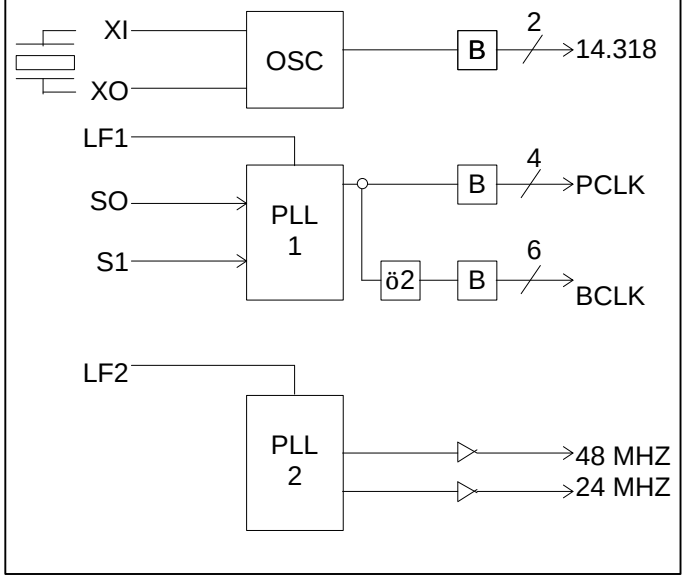
PRODUCT FEATURES

- Integrates clock generator and distribution buffers
- 3.3V to 5V operating supply range
- Supports Pentium™ based designs
- 200 ps typical buffer skew
- Supports USB (Universal Serial Bus)
- 28 Pin SSOP for minimum board space.
- Power down and tristate inputs

FREQUENCY TABLE

S0	S1	PCLK
0	0	50 MHz
0	1	60 MHz
1	0	66 MHz

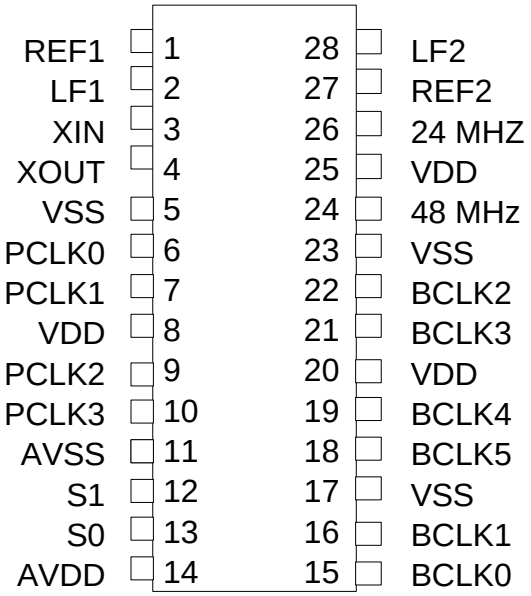
BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISC609 provides the clock frequencies and distribution buffers required on a Pentium™ system board. The SC609 contains a programmable PLL which provides the CPU and PCI clocks and a fixed PLL which povides the clocks necessary for the Universal Serial Bus (48MHz) and for the SuperIO (24mhz). The frequency output is determined by the S0-S1 pins. The on-chip buffers provide the low skew performance required by the CPU and PCI busses.

CONNECTION DIAGRAM



APPLICATIONS

The IMISC609 supports synchronous Pentium™ designs by providing clock distribution for the CPU and PCI bus and system fixed frequencies. The performance and functionality, conform to the Intel Mars and Triton II core logic requirements.

INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
MILPITAS, CA 95035 TEL: 408-263-6300 FAX 408-263-6571

PIN DESCRIPTIONS

Xin and Xout- These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal of 14.31818 at 12 PF load. Xin may also serve as an input for an externally generated CMOS reference signal.

PCLK0, PCLK1, PCLK2, and PCLK3- Low skew CPU bus clock outputs.

BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, and BCLK5- Low skew PCI bus clock outputs. These are one-half the frequency of PCLK.

48 MHz - 48 MHz Uniersal Serial Bus clock output
24 MHz - 24 MHz clock output.

REF1, and REF2- 14.31818 MHz clock outputs.

S1 and S0- Frequency select inputs. These inputs select the frequency of the PCLK and BCLK outputs. Both have internal pull-down resistors to VSS.

VSS- Circuit grounds.

VDD- Positive power supplies.

AVSS- Analog circuit ground.

AVDD- Analog positive power supply.

SC 609 FREQUENCY SELECT TABLE

S0	S1	XIN	PCLK	BCLK	REF	48 MHz	24 MHz
0	0	14.318	50	25	14.318	48	24
0	1	14.318	60	30	14.318	48	24
1	0	14.318	66	33	14.318	48	24
1	1	TCLK	TCLK/2	TCLK/4	TCLK	TCLK/2	TCLK/4

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MAXIMUM RATINGS

Voltage Relative to VSS	-0.3V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65°C to +150°C
Ambient Temperature:	-0°C to + 70°C
Maximum voltage supply	6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	S0-S1 Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	SO-S1 Inputs
Input Low Current with Pull up or Pull-down	IIL	-	-	5 ±50	uA	S0-S1 Inputs
Input High Current with Pull-up or Pull-down	IIH	-	-	5 ±50	uA	S0-S1 Inputs
Output Low Voltage IOL = 12mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH=12mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	IOZ	-	-	10	uA	LF1 and LF2
Dynamic Supply Current	ICC	-	-	30*	mA	PCLK = 66 MHz
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - max 30 sec.
Power Supply Condition						VDD = 3.3 ± 10%, TA = 0°C to +70°C

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SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	**t**TLH, **t**THL	-	-	1.5*	ns	15 pf Load
Output Duty Cycle		45	50	55	%	Measured at 1.5V
Offset PCLK to BCLK	**t**OFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew PCLK or BCLK	**t**SKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles PCLK	ΔP	-	-	±200	ps	-
Jitter Absolute PCLK and REF	**t**jab	-	±200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	us	-
Switching Current Low: REF1, PCLK, BCLK Outputs Other Outputs	IOL (AC) IOL (AC)	-	60* 30*	-	mA mA	VOL = 1.5V VOL = 1.5V
Switching Current High: REF1, PCLK, BCLK Outputs Other Outputs	IOH (AC) IOH (AC)	-	50* 28*	-	mA mA	VOL = 1.5V VOL = 1.5V
Power Supply Condition						VDD = 3.3V ± 10%, TA = 0°C to 70°C

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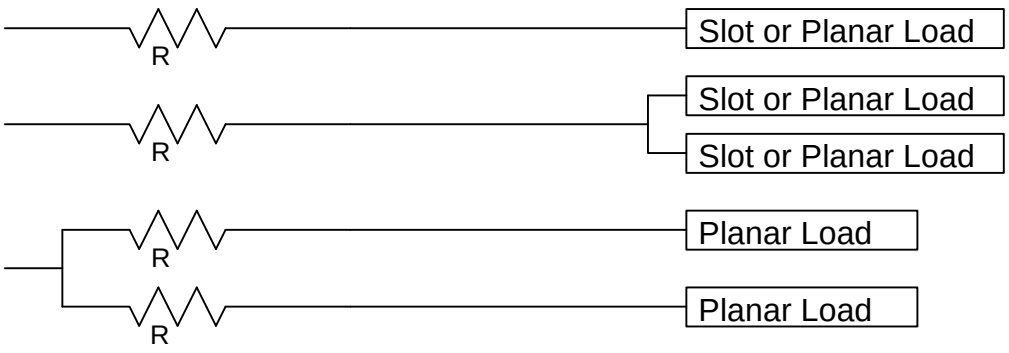
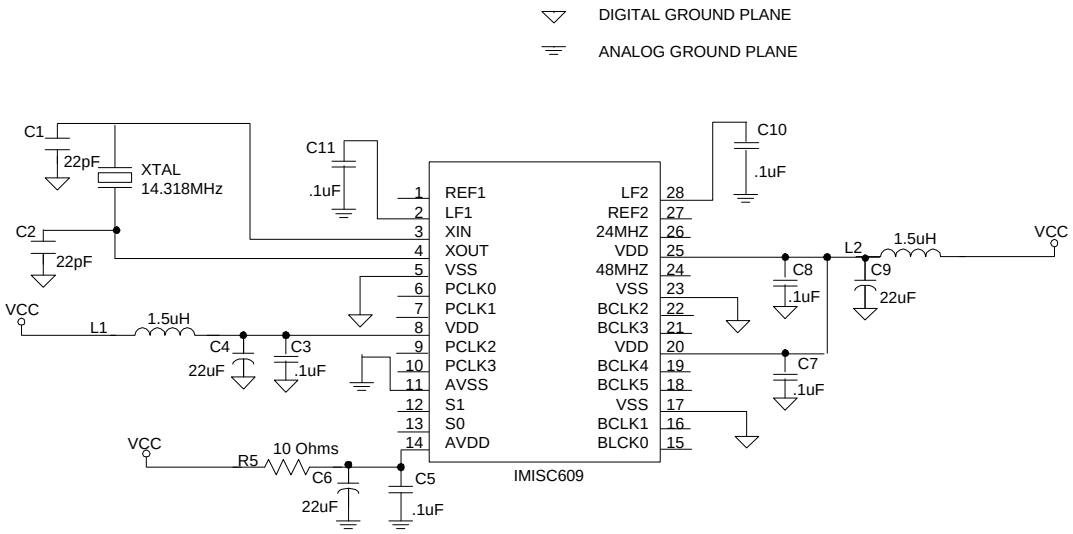
Output Loading Suggestion.



SUGGESTED MAXIMUM TRACE LENGTH, 8 INCHES.
(The above suggestions are based on VDD = 3.3 v)

APPLICATION DIAGRAM

C3, C5, C7, C8 MUST BE CLOSE TO THEIR VDD PINS.



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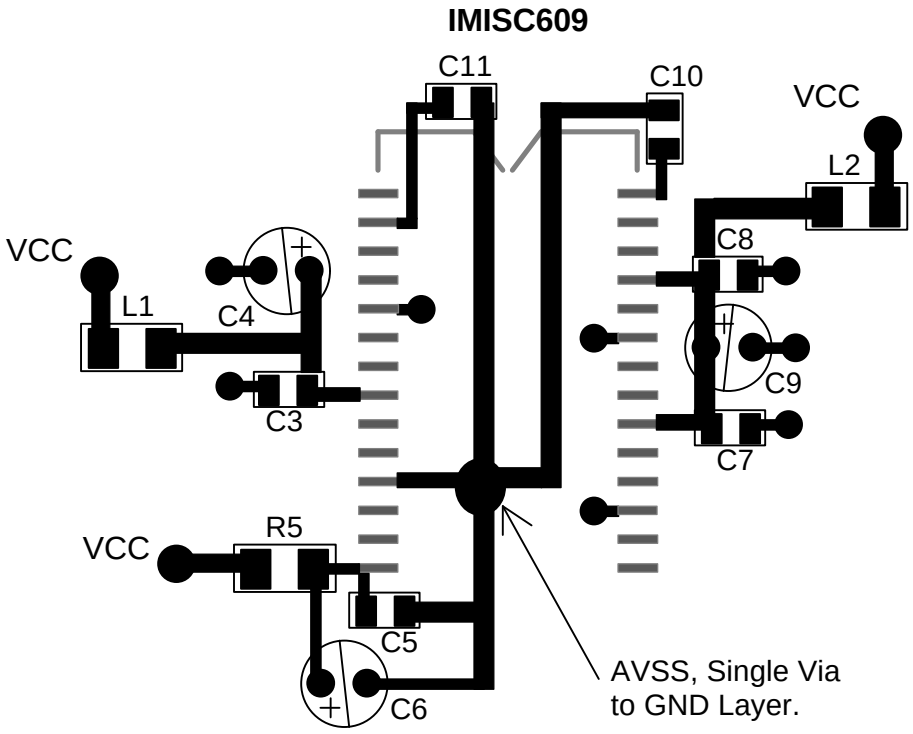
PCB LAYOUT SUGGESTION



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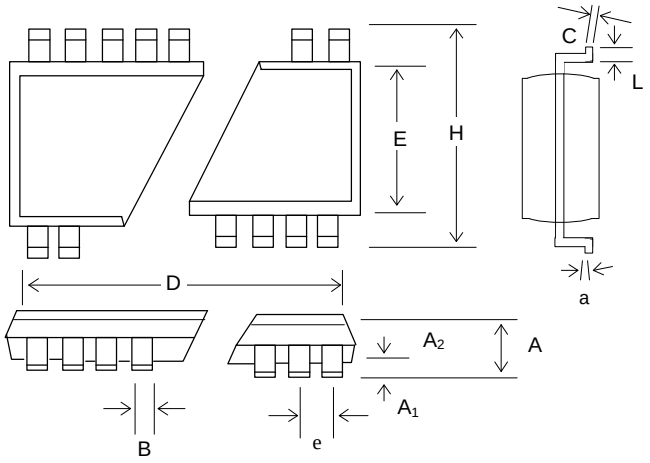
PACKAGE DRAWING AND DIMENSIONS



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A_2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0º	4º	8º	0º	4º	8º
L	0.022	0.030	0.037	0.55	0.75	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC609xYB	28 PIN SSOP	Commercial, 0°C to + 70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC609xYB
Date Code, Lot #

IMISC609xYB

Flow
= Commercial, 0°C to + 70°C

Package
Y = SSOP

Revision

IMI Device Number

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