Power PC 603/604 Motherboard Clock Generator

Approved Product

PRODUCT FEATURES

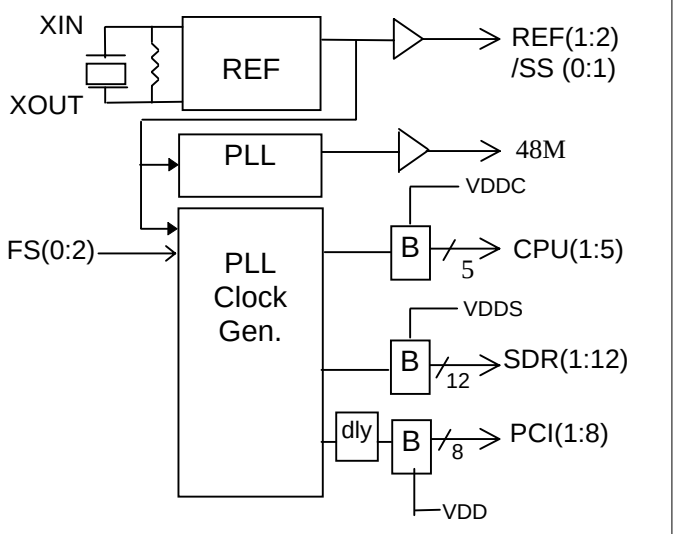
- Supports PPC603 and PPC604 Processors.
- 5 CPU clocks
- Up to 12 SDRAM clocks for 3 DIMMs.
- 8 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (VDD = VDDS = VDDC = 3.3V) or
- (VDD = VDDS =3.3V, VDDC = 2.5V)
- < 250ps skew among CPU or SDRAM clocks.
- < 250ps skew among PCI clocks.
- 2 Buffered reference clocks
- 52-pin QFP package

FREQUENCY TABLE (in MHz)

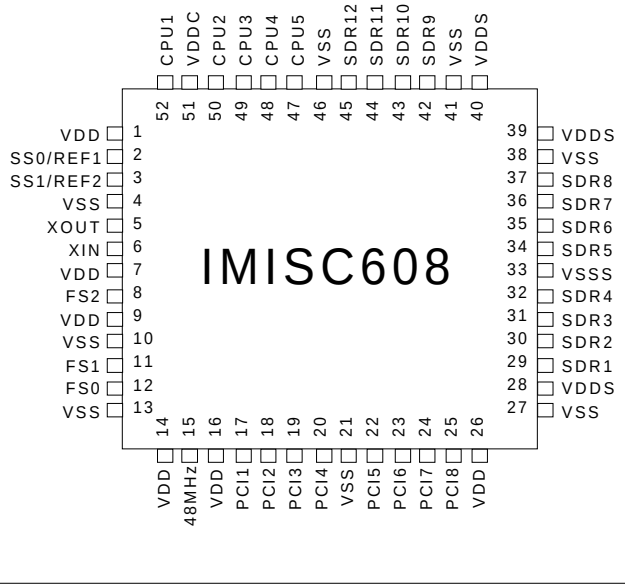
FS2	FS1	FS0	CPU (1:8)	PCI (1:8)
0	0	0	XIN/2*	XIN/4
0	0	1	70.00	35.00
0	1	0	78.75	31.50
0	1	1	Tri-state	Tri-state
1	0	0	75.17	30.07
1	0	1	60.14	30.07
1	1	0	66.82	33.41
1	1	1	83.30	33.32

Notes: *Test Mode (all fixed clocks = XIN)

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
6	**Xin**	VDD	I	OSC1 Rext	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1 Rext	On-chip reference oscillator output pin. Drives an external parallel resonant crystal when an externally generated reference signal is used, is left unconnected
12, 11, 8	**FS(0:2)**	---	I	PAD	Frequency select input pins. See frequency select table. These pins have internal pull-up resistors.
52, 50, 49, 48	**CPU(1:4)**	VDDC	O	TB4	Clock outputs. CPU frequency table specified.
47	**CPU5**	VDDC	0	TB4LB	High drive CPU output clock.
29, 30, 31, 32, 34, 35, 36, 37, 42, 43, 44, 45	**SDR(1:12)**	VDDS	O	TB4	Synchronous Dynamic RAM clock outputs.
17, 18, 19, 20, 22, 23, 24, 25	**PCI(1:8)**	VDD	O	TB4	PCI Bus clock outputs.
4, 10, 13, 21, 27, 33, 38, 41, 46	**Vss**	---	P	PWR	Ground pins for the device.
1, 7, 9, 14, 16, 26	**Vdd**	---	P	PWR	Power supply pins for analog circuit , Fixed clocks, PCI clocks and core logic
51	**VddC**	---	P	PWR	3.3 or 2.5 volt power supply pins for CPU clock output buffers pins.
28, 39, 40	**VddS**	---	P	PWR	3.3 volt power supply pins for SDRAM clock output buffers pins.
2, 3	**REF(1:2)**	VDD	O	TB4	Buffered output of on-chip reference oscillator. This pin is bidirectional.
15	**48MHz**	VDD	O	TB4	48 Mhz fixed frequency clock output for USB.

***NOTE**: An external resistor must be connected between the Xin (pin 6) and Xout (pin 5) pins to insure oscilator startup. The value of this must be between 200 and 500 Kohms.*

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	175	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	75	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDS =3.3V ±5***%, VDDC = 2.5V*** ±5***%, TA = 0ºC to +70ºC***

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SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	CPU measured @ 1.25V SDRAM, PCI & fixed @ 1.5 V
CPU to PCI Offset	tOFF	-1.5	0	+1.5	ns	20 pf Loads, PCI measured at 1.5 V, CPU measured at 1.25V
Output Skew any CPU to any CPU Buffer	Ts1	-	-	±250	ps	20 pf Load Measured at 1.25V
Output Skew any PCI to any PCI Buffer.	Ts2	-	-	±500	ps	20 pf Load, CPU Measured @ 1.25V, SDRAM measured @ 1.5V
Output Skew any SDRAM to any SDRAM Buffer.	Ts3	-	-	±250	ps	30 pf Load, Measured at 1.50V
Output Skew any CPU to any SDRAM Buffer.	Ts4			±500	ps	20 pf Load, CPU Measured @ 1.25V, 30 pf SDRAM measured @ 1.5V
ΔPeriod Adjacent Cycles	ΔPs			±250	ps	Short term jitter
ΔPeriod, Absolute	ΔPl			±500	ps	Long term jitter
VDD = VDDS =3.3V ±5%, VDDC =2.5V ±5%,,, TA = 0ºC to +70ºC						

TYPE TB4LB_V BUFFER CHARACTERISTICS FOR CPU5						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	22	-	31	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	37	-	56	mA	Vout = 1.25V
Pull-Down Current Min	IOL_{min}	30	-	41	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	75	-	100	mA	Vout = 1.2V
Rise & Fall Time Between 0.4 V and 2.0 V	TRF	0.4	-	2.0	nS	20 pF Load
VDD = VDDS =3.3V ±5%, VDDC =2.5V ±5%, TA = 0ºC to +70ºC						

TYPE TB4 BUFFER CHARACTERISTICS FOR 48M REF(1:2), CPU (1:4), SDR (1:12), AND PCI (1:8)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	18	-	23	mA	Vout = VDD - .5V
Pull-Up Current Max	IOH_{max}	44	-	64	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	18	-	25	mA	Vout = 0.4V
Pull-Down Current Max	IOL_{max}	50	-	70	mA	Vout = 1.5V
Rise/Fall Time Between 0.4 V and 2.4 V	TRF	0.4	-	2.0	nS	20 pF Load
VDD = VDDS =3.3V ±5%, VDDC =2.5V ±5%, TA = 0ºC to +70ºC						

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CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Shunt Resistor	Rs	200	470	510	Kohms	Must be connected between Xin and Xout pin to ensure correct startup.
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	18	-	pF	note 1
Effective Series resonant resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. Typical trace capacitance, for traces less than a half inch are 4 pF. with an internal pin capacitance of 5 pF the total parasitic capacitance would be 9 pF. It this instance a 27 pF capacitor added to both legs (pins) of the crystal would bring its total load the recommended 18 pF CL pF each leg) that the crystal was calibrated to operate at.

Note 1: It is recommended but not mandatory chooses a crystal that meets these specifications.

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PROGRAMMABLE CPU TO PCI CLOCK TIMING.

The IMISC608 features programmable CPU to PCI clock skew feature. With this feature the PCI clock can be retarded or advanced with respect to the CPU clock to permit the user the ability to adjust critical timing on a specific motherboard design. There are 4 values of skew available in this feature. They are shown in the following table. a + value indicated that the PCI clock lead or transitions before the CPU clock in time while a - value indicated that the PCI lock transitions or changes after the CPU clock has. This feature is accessible through the REF1 and REF2 clock output pins. As such they are implemented as bidirectional pins. This implementation as described below. With no programming resistors used the default table value 11 is selected causing 0 offset.

PROGRAMMABLE CPU TO PCI CLOCK SKEW TABLE

SS0/REF1	SS1/REF2	Effect
0	0	CPU clocks lags PCI clocks (PCI early) by 500 pSec
1	0	CPU clocks leads PCI clocks (CPU early) by 1500 pSec
0	1	CPU clocks leads PCI clocks (CPU early) by 1000 pSec
1	1	CPU clocks lags PCI clocks (PCI early) by 250 pSec

SELECTION ON BI-DIRECTIONAL PINS

Bi-directional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode and therefore, they are considered input select pins. Internal to the IC, these pins have a large value pull-up each (100KΩ), therefore, a selection “1” is the default. If a selection “0” is desired, then a direct connection to ground through a 10KΩ resistor should be implemented as shown in Fig. 3. Please note the selection resistor (10KΩ) is placed before the Damping resistor (Rd) and close to the devices pin.

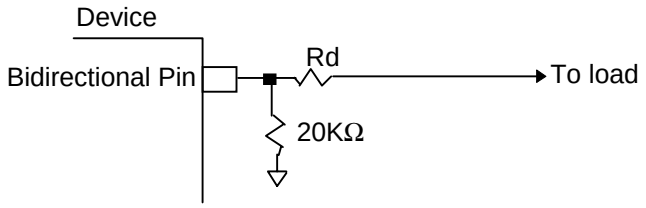

Fig. 3

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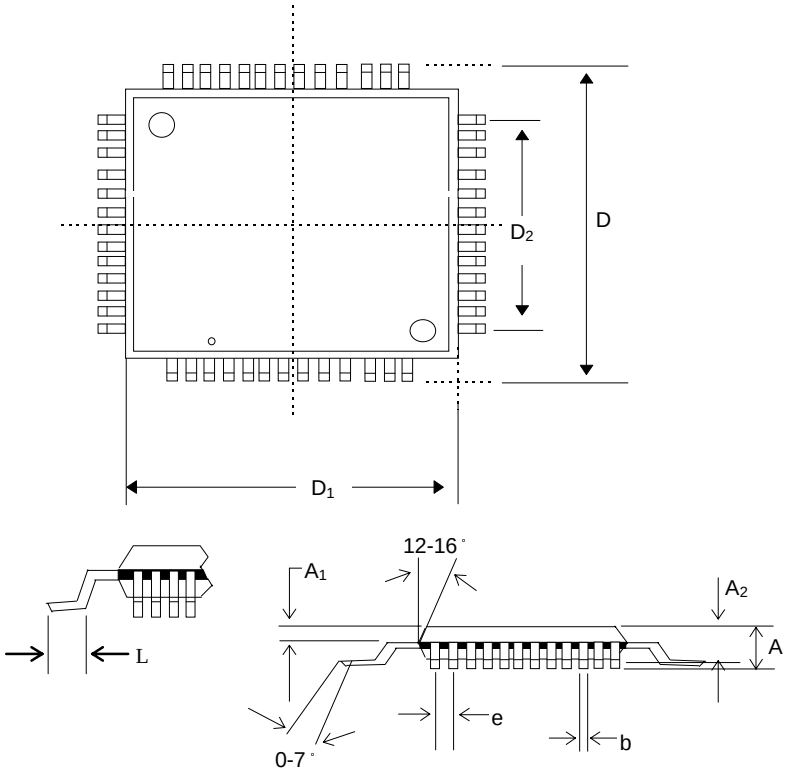
PACKAGE DRAWING AND DIMENSIONS



52 PIN QFP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	0.084	0.093	-	2.13	2.35
A_1	0.03	.006	.010	0.10	0.15	0.25
A_2	0.077	0.079	0.083	1.95	2.00	2.10
D	0.537	0.547	0.557	13.65	13.90	14.15
D_1	0.390	0.394	0.398	9.90	10.00	10.10
D_2	0.307 REF			7.80 REF		
b	0.009	-	0.015	0.22	-	0.38
e	.0256 BSC			0.65 BSC		
L	0.026	0.031	0.037	0.65	0.80	0.95

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC608AAB	52 PIN QFP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC608AAB, Date Code, Lot #

IMISC608AAB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: A = QFP
- Revision
- IMI Device Number