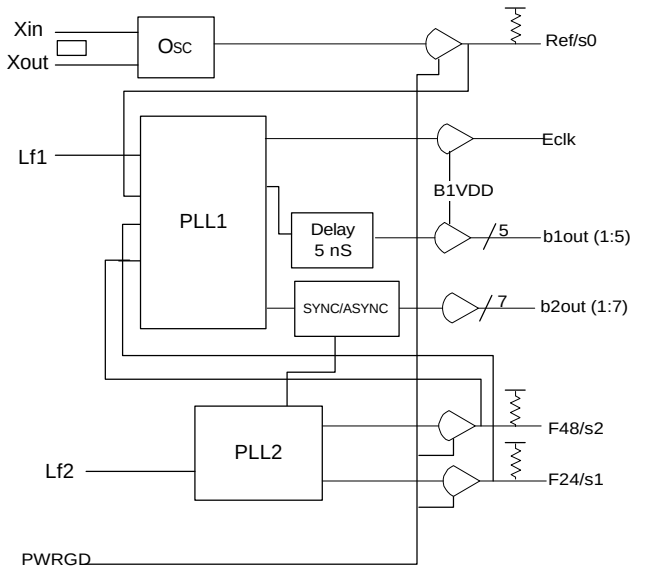
IMISC607 System Clock Generator

Preliminary
June 1996

PRODUCT FEATURES

- Supports PCI system board designs P54, P55, and P6
- Integrates system clocks and distribution buffers
- An early host clock, 5 low skew host clocks and 7 low skew PCI clocks
- Supports 5V or 3.3V or mixed supply.
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISC607A provides the clocks and the low skew distribution buffers required to drive the Pentium™ CPU and PCI busses. Mixed supply option for P55/54 applications. Fixed 24 for the keyboard and 48 MHz for U.S.B.

APPLICATIONS

60 mA of switching current is provided on all outputs at B1VDD = VDD = 5V.

3.3V operating modes support new low voltage components on the CPU bus. Operating the B1 buffer at 3.3V (B1VDD) and routing the CPU clock through B1 distributes a 3.3V signal to the CPU bus. The outputs provide 30 mA switching current.

FREQUENCY TABLE

SELECT			OUTPUTS (MHz)	
F12/S2	F24/S1	Ref/S0	ECLK+	B2out*
0	0	0	50	a.32
0	0	1	55	a.32
0	1	0	75	a.32
0	1	1	75	37.5
1	0	0	50	25
1	0	1	55	27.5
1	1	0	60	30
1	1	1	66.6	33.3

+ ECLK = B1out*
a.32 = asyncronous 32 MHz.

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PIN DESCRIPTION

Xin Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

ECLK - Early Host Clock output. When PWRGD is low, this pin is low.

B1out* - Delayed buffered outputs of ECLK.

B2out* - Buffered outputs for PCI bus. Synchronous to ECLK.

F24/S1 - When PWRGD is low this pin is used as an input select line, S1. When PWRGD is high this pin is 24 MHz output. This pin has an internal pull-up.

F48/S2 - When PWRGD is low this pin is used as an input select line, S2. When PWRGD is high this pin is 48 MHz output. This pin has an internal pull-up.

PWRGD - Logic low on this input tristates the fixed frequency outputs and forces Eclk, B1out*, and B2out* outputs to a low state synchorously. When logic transitions to high, the select is latched, the fixed frequency outputs are enabled, and Eclk, B1out*, B2out* toggle syncronously at the rising edge.

Ref/S0 - When PWRGD is low this pin is used as an input select line, S0. When PWRGD is high this pin is a reference output of the crystal input. This pin has an internal pull-up.

LF1 and LF2 - These are the loop filter pins for the clock generators. A 0.1µF capacitor should be connected from each pin to AVSS. Grounding LF puts PLL in low power mode.

VSS - Circuit ground.

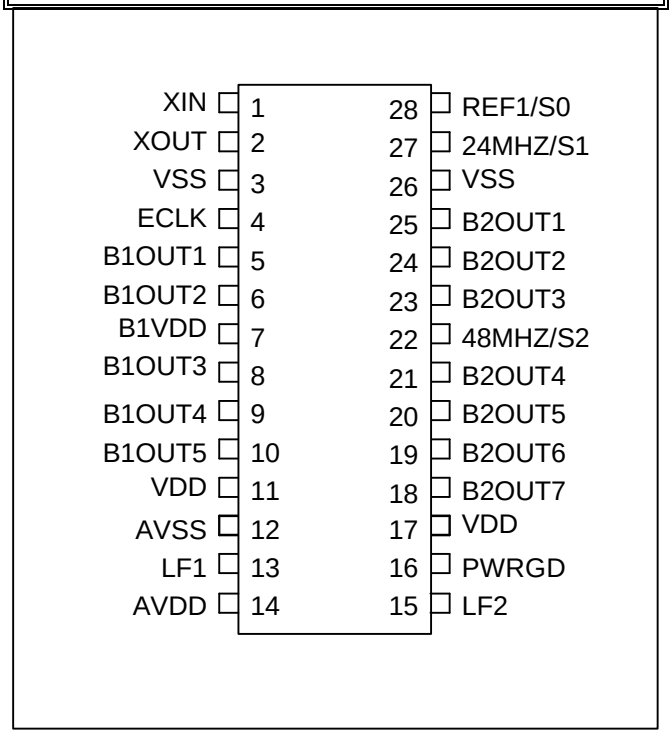
VDD - Positive power supply.

AVSS - Analog circuit ground.

AVDD - Analog positive power supply.

B1VDD - 3.3V/5V logic level control for ECLK and B1out* outputs.
Note: always B1VDD $\leq$ VDD.

CONNECTION DIAGRAM



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MAXIMUM RATINGS

Voltage Relative to VSS: -0.3V
Voltage Relative to VDD: 0.3V
Storage Temperature: -65ºC to 150ºC
Ambient Temperature: -55ºC to +125ºC
Maximum Operating Supply: 6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to its circuit. For proper operation, Vin and Vout should be constrained to the range:

Vss< (Vin or Vout) < VDD

Unused inputs must always be tied to an appropriate logic voltage level (either Vss or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-	-	0.8	Vdc	PWRGD, F12/S2, F24/S1, Ref/S0
Input High Voltage	V_{IH}	2.0	-	-	Vdc	
Input Low Current	I_{IL}, I_{IH}			5	µA	
with Pull-up or Pull-down				± 50		
Output Low Voltage IOL = 6mA	V_{OL}	-	-	0.4	Vdc	ECLK/B1out*
Output High Voltage IOH=6mA	V_{OH}	2.4	-	-	Vdc	
Output Low Voltage IOL = 12mA	V_{OL}	-	-	0.4	Vdc	All other outputs
Output High Voltage IOH=12mA	V_{OH}	2.4	-	-	Vdc	
Tri-State leakage Current	I_{OZ}	-	-	10	µA	LF1, LF2, and tristate outputs
Dynamic Supply Current	I_{DD}	-	-	TBD	mA	B1OUT* = 50 MHz
Static Supply Current	I_{DD}	-	TBD	-	µA	LF1 = LF2 = 0, Xin = 1
Short Circuit Current	I_{OS}	25	-	-	mA	1 output at a time - max 30 sec.
VDD=AVDD= 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0ºC to 70ºC						

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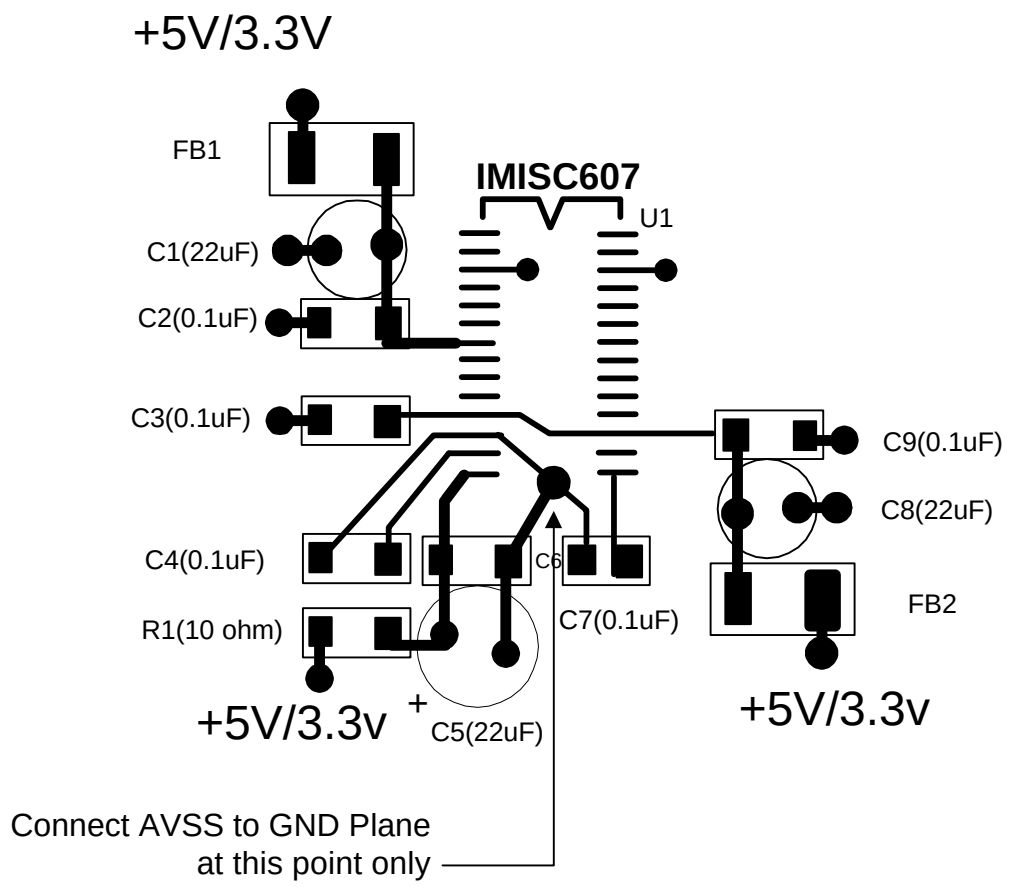
PCB LAYOUT SUGGESTIONS

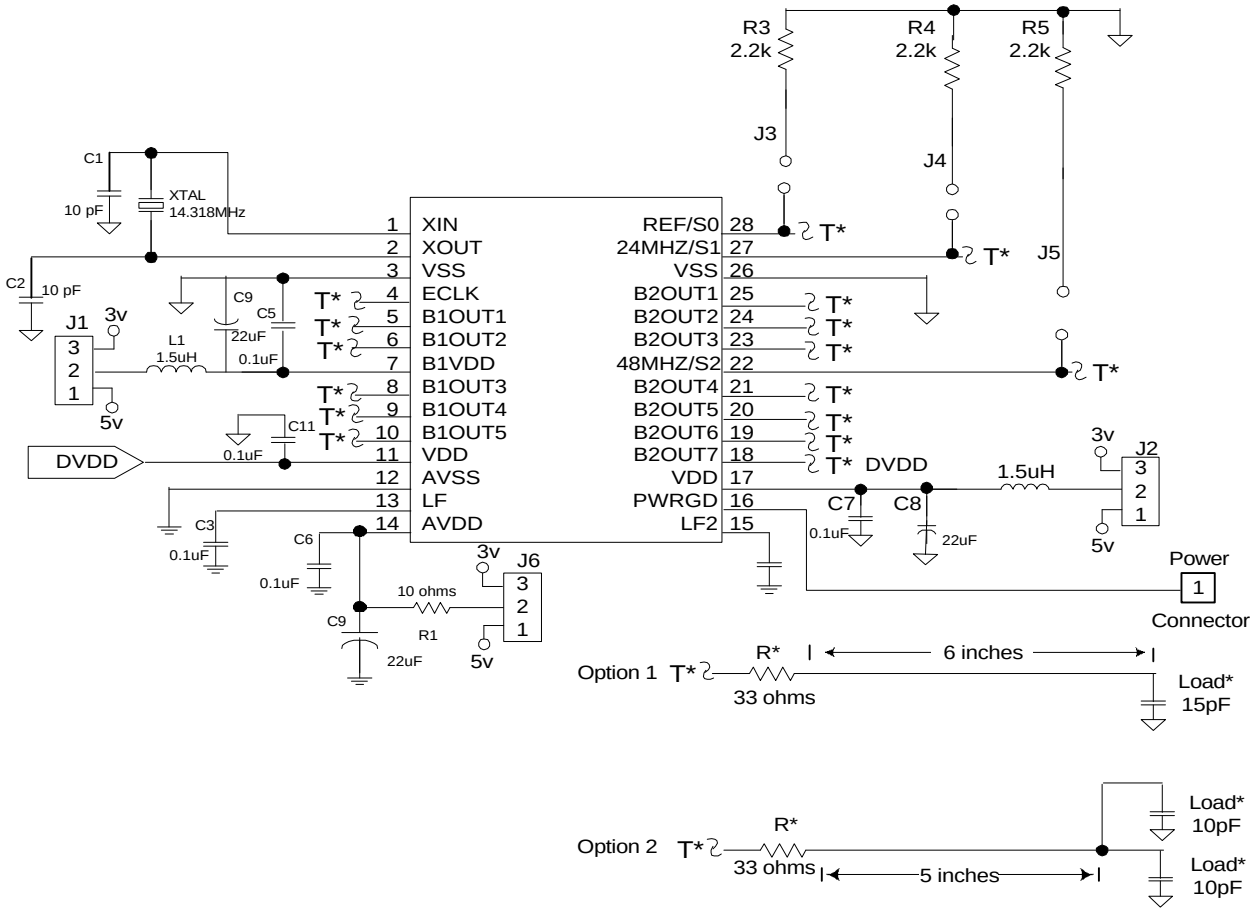


COMPONENT LAYER

NOTES

1. Power supply bypass caps (0.1µF and 22 µF) must be positioned close to VDD pins to be effective.
2. LF caps must be low leakage, such as ultilayer ceraic Z5U or X7$ material.

APPLICATION SUGGESTION



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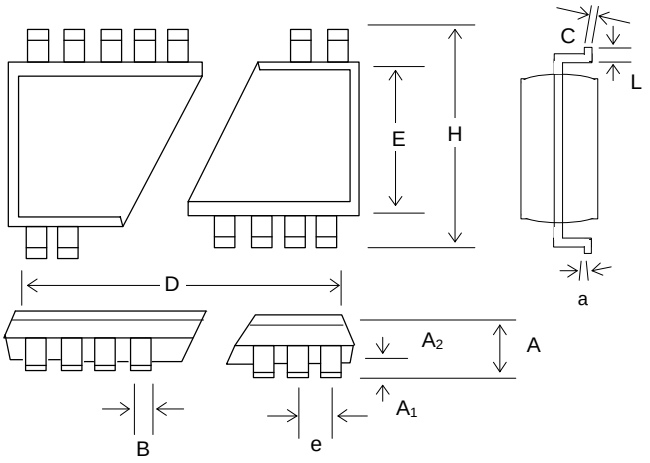
SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V)	tTLH,	-	-	1.5	nS	15 pF load. B1out*
and Fall (2.0V-0.8V) time	tTHL	-	-	1.5	nS	15pF load. All other outputs
Output duty cycle		45	50	55	%	Measured at 1.5V, 15 pF load
B1out*-Skew	t1SKW	-	-	250	pS	Measured at 1.5V
B2out*-Skew	t2SKW	-	-	500	pS	Measured at 1.5V
B1out* - B2out* OFFSET	tOFF	0	-	4	nS	Measured at 1.5V
ECLK to B1out* Delay	tDLY	-	6.0		nS	Measured at 1.5V (selectable)
ΔPeriod Adjacent Cycles	ΔP	-	-	± 200	pS	Measured at 1.5V on B1OUT*
Jitter Absolute	tjab	-	± 250		pS	Measured at 1.5V on B1OUT*

VDD=AVDD= 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0ºC to 70ºC

PACKAGE DRAWINGS AND DIMENSIONS



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.078	1.73	1.8	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC607AYB	28 Pin SSOP	Commercial, 0° C to + 70 C°

NOTE: The order part number is formed b a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC607AYB
Date Code
Lot #

IMISC607AYB

Flow

B = Commerical, 0° C to + 70 C°

Package

Y = SSOP

Revision

IMI Device Number