IMISC498 SYSTEM CLOCK CHIP

July 1995
Preliminary

CMOS LSI
PLL FREQUENCY SYNTHESIZER

PRODUCT FEATURES

- Integrates clock generator and distribution buffers
- 3.3V to 5V operating supply range
- Supports Pentium™ based designs
- 200 ps typical buffer skew
- Supports USB (Universal Serial Bus)
- 28 Pin SOIC
- Power down and tristate inputs

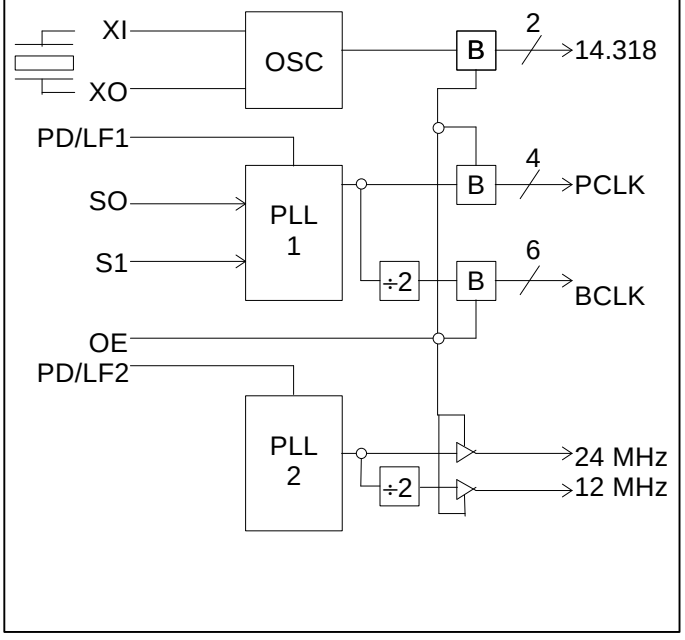
APPLICATIONS

The IMISC498 supports synchronous Pentium™ designs by providing clock distribution for the CPU and PCI bus and system fixed frequencies. The performance, functionality, and pin out conform to the Intel Mars and Triton II core logic requirements.

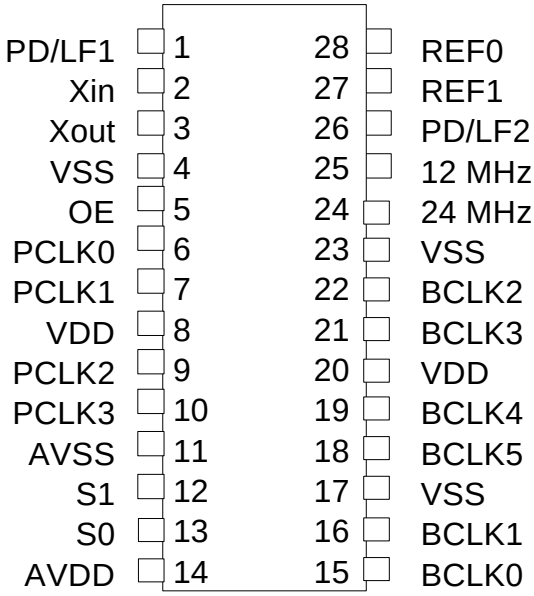
SC 498 FREQUENCY SELECT TABLE

S0	S1	XIN	PCLK	BCLK	REF	24 MHz	12 MHz
0	0	14.318	50	25	14.318	24	12
0	1	14.318	60	30	14.318	24	12
1	0	14.318	66	33	14.318	24	12
1	1	TCLK	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

BLOCK DIAGRAM



CONNECTION DIAGRAM



INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
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PIN DESCRIPTIONS

Xin and Xout- These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal of 14.31818 at 12 PF load. Xin may also serve as an input for an externally generated CMOS reference signal.

OE- Output enable. When OE is high, all clock outputs are enabled. When OE is low, all clock outputs are tristated. This input has internal pull-up resistor to VDD.

PCLK0, PCLK1, PCLK2, and PCLK3 - CPU bus clock outputs.

BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, and BCLK5 - PCI bus clock outputs. These are one-half the frequency of PCLK.

24 MHz - 24 MHz clock output

12 MHz - 24 MHz clock output

REF0 and REF1- 14.31818 MHz clock outputs.

S1 and S0- Frequency select inputs. These inputs select the frequency of the PCLK and BCLK outputs. Both have internal pull-down resistors to VSS.

PD/LF1 and PD/LF2- These are the phase detector outputs for the clock generators. They are single-ended, tri-state outputs for use as loop error signals. The loop filter should be connected as shown in the application diagram. Forcing these pins to a voltage below 0.8 turns off PLL.

VSS (3)- Circuit grounds.

VDD(2)- Positive power supplies.

AVSS- Analog circuit ground.

AVDD- Analog positive power supply.

MAXIMUM RATINGS

Voltage Relative to VSS	-.03 to 6V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65°C to +150°C
Ambient Temperature:	-0°C to + 70°C
Recommended Operating Range	3V - 6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-	-	0.8	Vdc	OE, S0-S1 Inputs
Input High Voltage	V_{IH}	2.0	-	-	Vdc	OE, SO-S1 Inputs
Input Low Current with Pull up or Pull-down	I_{IL}	-	-	5 ±50	uA	OE, S0-S1 Inputs
Input High Current with Pull-up or Pull-down	I_{IH}	-	-	5 ±50	uA	OE, S0-S1 Inputs
Output Low Voltage IOL = 6mA	V_{OL}	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH=6mA	V_{OH}	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	I_{OZ}	-	-	10	uA	LF1 and LF2 and All Outputs
Dynamic Supply Current	I_{CC}	-	-	30	mA	PCLK = 66 MHz
Short Circuit Current	I_{SC}	25	-	-	mA	

VDD = + 3.3 ± 10%, TA = 0°C to +70°C

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	$\mathbf{t}_{TLH}$, $\mathbf{t}_{THL}$	-	-	1.5*	ns	15 pf Load
Output Duty Cycle		45	50	55	%	Measured at 1.5V
Skew PCLK to BCLK	$\mathbf{t}_{SKEW}$PB	1.0	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew PCLK or BCLK	$\mathbf{t}_{SKEW}$	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles PCLK	ΔP	-	±200	-	ps	-
Jitter Absolute PCLK and REF	$\mathbf{t}_{jab}$	-	±200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	us	-
Switching Current Low, PCLK, BCLK Outputs Other Outputs	I_{OL} (AC) I_{OL} (AC)	-	60 30	-	mA mA	VOL = 1.5V VOL = 1.5V
Switching Current High, PCLK, BCLK Outputs Other Outputs	I_{OH} (AC) I_{OH}(AC)	-	50 28	-	mA mA	VOL = 1.5V VOL = 1.5V

VDD = +3.3V ± 10%, TA = 0°C to 70°C

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APPLICATION DIAGRAM

NOTE 1: CONNECT DIGITAL GROUND AND ANALOG GROUND THROUGH ONE POINT ONLY ON PC BOARD.

NOTE 2: C4 AND C5 - C8 MUST BE CLOSE TO THEIR PINS.

NOTE 3: C3 AND C9 SHOULD CONNECT TO AVSS INDEPENDENT OF CONNECTION CARRYING CURRENT FROM AVSS TO SYSTEM GROUND.

NOTE 4: IF VCC AT CLOCK GENERATOR CONTAINS POSITIVE VOLTAGE STEPS > OR -100 MV WITHIN 5 US (FROM TURNING DISK DRIVE OFF, ETC.), THE VALUES OF L1, C1, AND C2 SHOULD BE INCREASED APPROXIMATELY 10X TO AVOID OUT-OF-SPEC SHORT CLOCK CYCLES.

NOTE 5: VALUES OF C6 AND C7 MUST BE INCREASED TO INSURE FREQUENCY ACCURACY FOR CRYSTALS TUNED AT CL HIGHER THAN 12 PF.

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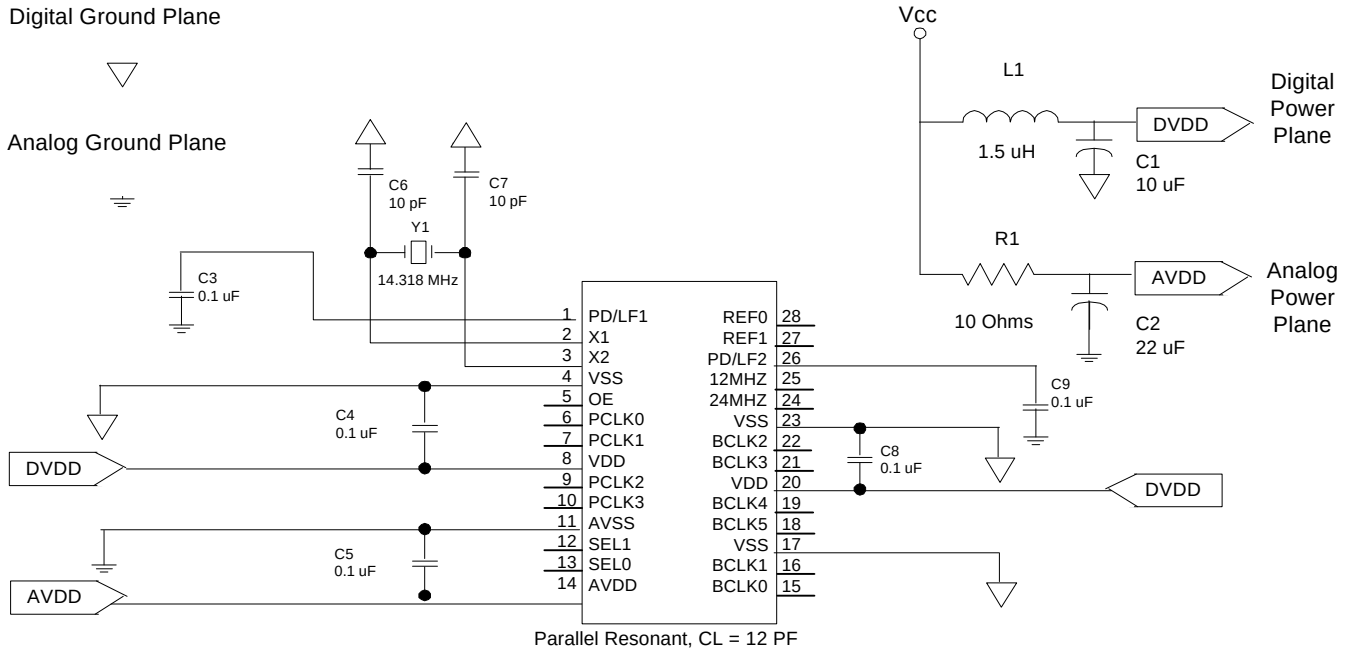
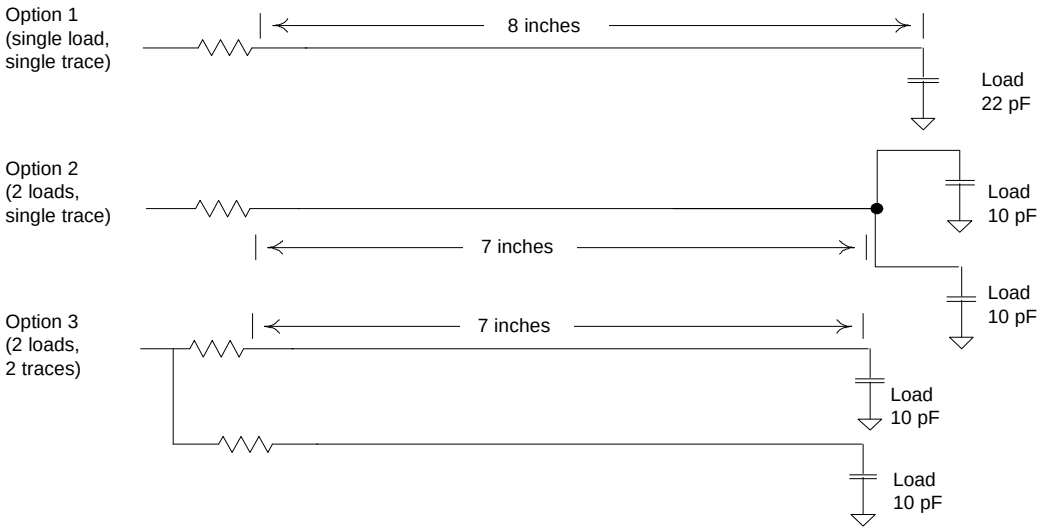
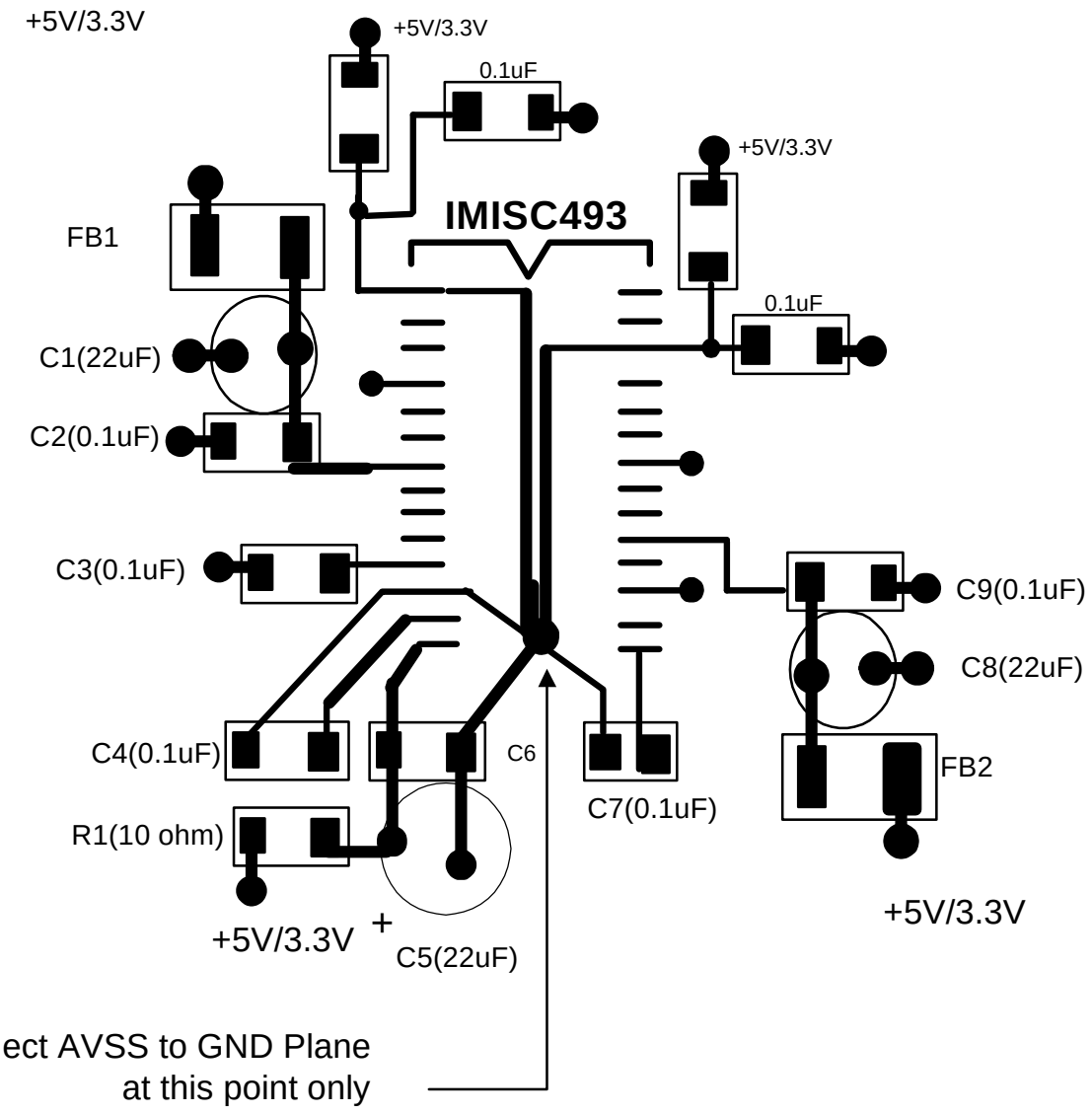


Parallel Resonant, CL = 12 PF



PCB LAYOUT SUGGESTION



COMPONENT LAYER

NOTES

1. Power supply bypass caps (0.1uF and 22 uF) must be positioned close to VDD pins to be effective.
2. LF caps must be low leakage, usch as multilayer ceramic Z5U or X7R materials

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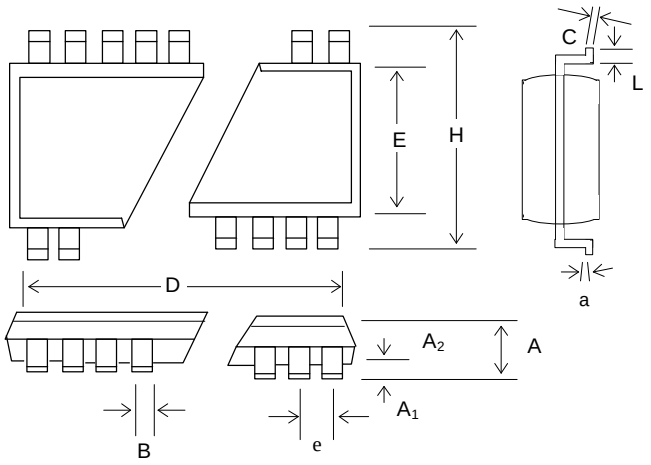
PACKAGE DRAWING AND DIMENSIONS



SOIC Package (300 mil)

28 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.005	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.009	0.010	0.0125	0.23	0.25	032
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0°	5°	8°	0°	5°	8°
L	0.024	0.032	0.040	0.61	0.81	1.02

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC498xXB	28 PIN SOIC	Commercial, 0°C to + 70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC498xXB
Date Code, Lot #

IMISC498xXB

Flow
B = Commercial, 0°C to + 70°C

Package
X = SOIC

Revision

IMI Device Number

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