# IMISC485 SYSTEM CLOCK CHIP

September 1, 1995

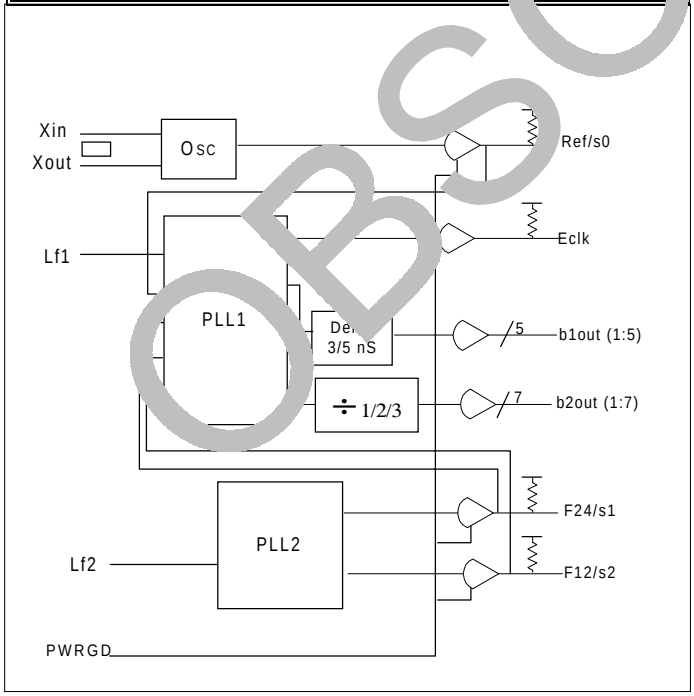
**Patent Pending**

PLL FREQUENCY SYNTHESIZER
CMOS LSI

## PRODUCT FEATURES

- Supports PCI system board designs P54, P55, and P6
- Integrates system clocks and distribution buffers
- An early host clock (programmable delay), 5 host clocks and 7 PCI clocks
- Supports 5V or 3.3V on ECLK and B1out*
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

## BLOCK DIAGRAM




## PRODUCT DESCRIPTION

The IMISC485 provides the clocks and the low skew distribution buffers required to drive the Pentium™ CPU and PCI busses. Selectable delay between ECLK and B1out*. Mixed supply option for P55/54 applications. Fixed 24 and 12 Mhz for floppy and keyboard.

## CONNECTION DIAGRAMS

| | | | | | |
|---|---|---|---|---|---|
| Xin | 1 | 28 | Ref/S0 |
| Xout | 2 | 27 | F24/S1 |
| VSS | 3 | 26 | VSS |
| Eclk | 4 | 25 | B2out1 |
| B1out1 | 5 | 24 | B2out2 |
| B1out2 | 6 | 23 | B2out3 |
| B1vdd | 7 | 22 | F12/S2 |
| B1out3 | 8 | 21 | B2out4 |
| B1out4 | 9 | 20 | B2out5 |
| B1out5 | 10 | 19 | B2out6 |
| VDD | 11 | 18 | B2out7 |
| AVSS | 12 | 17 | VDD |
| Lf1 | 13 | 16 | PWRGD |
| AVDD | 14 | 15 | Lf2 |

## APPLICATIONS

60 mA of switching current is provided on all outputs at B1VDD = VDD = 5V.

3.3V operating modes support new low voltage components on the CPU bus. Operating the B1 buffer at 3.3V (B1VDD) and routing the CPU clock through B1 distributes a 3.3V signal to the CPU bus. The outputs provide 30 mA switching current.

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## PIN DESCRIPTION

**Xin Xout** - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as input for an externally generated reference signal.

**ECLK** - Programmable early clock output. When PWRGD is low, this pin is tristated and is then used as an input to select the offset delay of B1out * buffers. This pin has an internal pull-up.

**B1out*** - Delayed buffered outputs of ECLK.

**B2out*** - Buffered outputs for PCI bus. Synchronous to ECLK.

**F24/S1** - When PWRGD is low this pin is used as an input select line, S1. When PWRGD is high this pin is 24 MHz output. This pin has an internal pull-up.

**F12/S2** - When PWRGD is low this pin is used as an input select line, S2. When PWRGD is high this pin is 12 MHz output. This pin has an internal pull-up.

**PWRGD** - Logic low on this input tristates all outputs. When logic transitions to high, it causes the select data to be latched and the outputs are enabled.

**Ref/S0** - When PWRGD is low this pin is used as an input select line, S0. When PWRGD is high this pin is a reference output of the crystal input. This pin has an internal pull-up.

**LF1 and LF2** - These are the loop filter pins for the clock generators. A 0.1µF capacitor should be connected from each pin to AVSS. Grounding LF puts PLL in low power mode.

**VSS** - Circuit ground.

**VDD** - Positive power supply.

**AVSS** - Analog circuit ground.

**AVDD** - Analog positive power supply.

**BUFVDD** - 3.3V/5V logic level control for ECLK and B1out* outputs.

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**FREQUENCY TABLE**

| SELECT | | | OUTPUTS (MHz) | |
|---|---|---|---|---|
| F12/S2 | F24/S1 | Ref/S0 | ECLK+ | B2out* |
| 0 | 0 | 0 | 40 | 20 |
| 0 | 0 | 1 | 75 | 37.5 |
| 0 | 1 | 0 | 40 | 40 |
| 0 | 1 | 1 | reserved | reserved |
| 1 | 0 | 0 | 50 | 33.3 |
| 1 | 0 | 1 | 50 | 25 |
| 1 | 1 | 0 | 60 | 30 |
| 1 | 1 | 1 | 66.6 | 33.3 |

**+ ECLK = B1out***

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## MAXIMUM RATINGS

Voltage Relative to VSS: -0.3V
Voltage Relative to VDD: 0.3V
Storage Temperature: -65ºC to 150ºC
Ambient Temperature: -55ºC to +125ºC
Maximum Operating Supply: 6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to its circuit. For proper operation, Vin and Vout should be constrained to the range:

Vss< (Vin or Vout) < VDD

Unused inputs must always be tied to an appropriate logic voltage level (either Vss or VDD).

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | - | | | Vdc | PWRGD, F12/S2, F24/S1, Ref/S0, ECLK |
| Input High Voltage | $V_{IH}$ | 2.0 | - | - | Vdc | |
| Input Low Current with Pull-up or Pull-down | $I_{IL}$, $I_{IH}$ | | | 5 | µA | |
| | | | - | ± 50 | | |
| Output Low Voltage IOL = 6mA | $V_{OL}$ | - | - | 0.4 | Vdc | ECLK and B1out* |
| Output High Voltage IOH=6mA | $V_{OH}$ | 2.4 | - | - | Vdc | |
| Output Low Voltage IOL = 12mA | $V_{OL}$ | - | - | 0.4 | Vdc | All other outputs |
| Output High Voltage IOH=12mA | $V_{OH}$ | 2.4 | - | - | Vdc | |
| Tri-State leakage Current | $I_{OZ}$ | - | - | 10 | µA | LF1, LF2, and tristate outputs |
| Dynamic Supply Current | $I_{DD}$ | - | - | TBD | mA | ECLK = 50 MHz |
| Static Supply Current | $I_{DD}$ | - | TBD | - | µA | LF1 = LF2 = 0, Xin = 1 |
| Short Circuit Current | $I_{OS}$ | 25 | - | - | mA | 1 output at a time - max 30 sec. |

VDD=AVDD= 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0ºC to 70ºC

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## SWITCHING CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time | tTLH, | - | - | 1.5 | nS | 15 pF load. B1out* + ECLK |
| | tTHL | - | - | 1.5 | nS | 15pF load. All other outputs |
| Output duty cycle | | 45 | 50 | 55 | % | Measured at 1.5V, 15 pF load |
| B1out*-Skew | t1SKW | - | - | 250 | pS | Measured at 1.5V |
| B2out*-Skew | t2SKW | - | - | 500 | pS | Measured at 1.5V |
| B1out* - B2out* | | 0 | - | 4 | nS | Measured at 1.5V |
| ECLK to B1out* CLK Offset | tOFF | - | 2.5* | | nS | Measured at 1.5V (selectable) |
| ΔPeriod Adjacent Cycles | ΔP | - | ± 20 | - | pS | Measured at 1.5V on ECLK |
| Jitter Absolute | tjab | - | ± 200 | | pS | Measured at 1.5V on ECLK |
| | | | | | | VDD=AVDD= 5V ± 10% B1VDD = 3.3V ± 10%. TA = 0ºC to 70ºC |

*See Application Note for implementation

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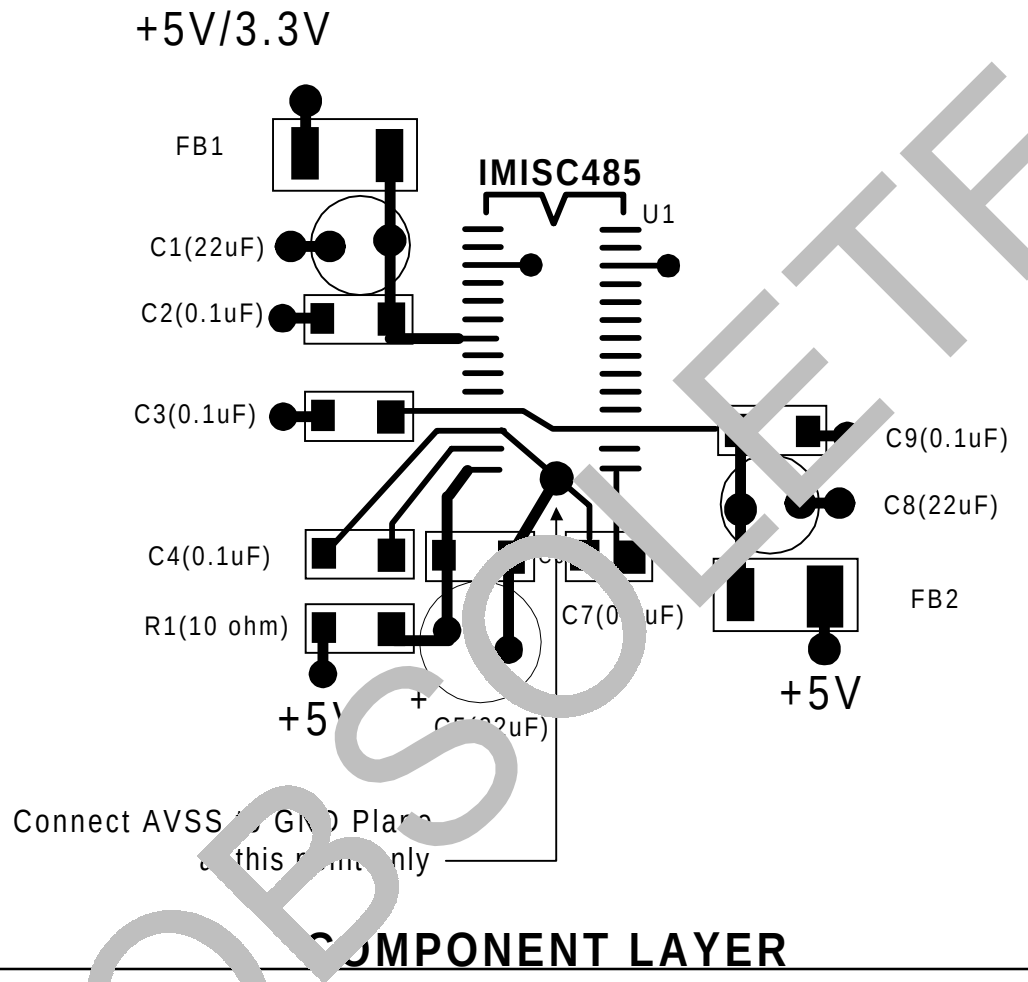
## PCB LAYOUT SUGGESTION

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## NOTES

1. Power supply bypass caps (0.1μF and 22 μF) must be positioned close to VDD pins to be effective.
2. LF caps must be low leakage, such as multilayer ceramic Z5U or X7R material.

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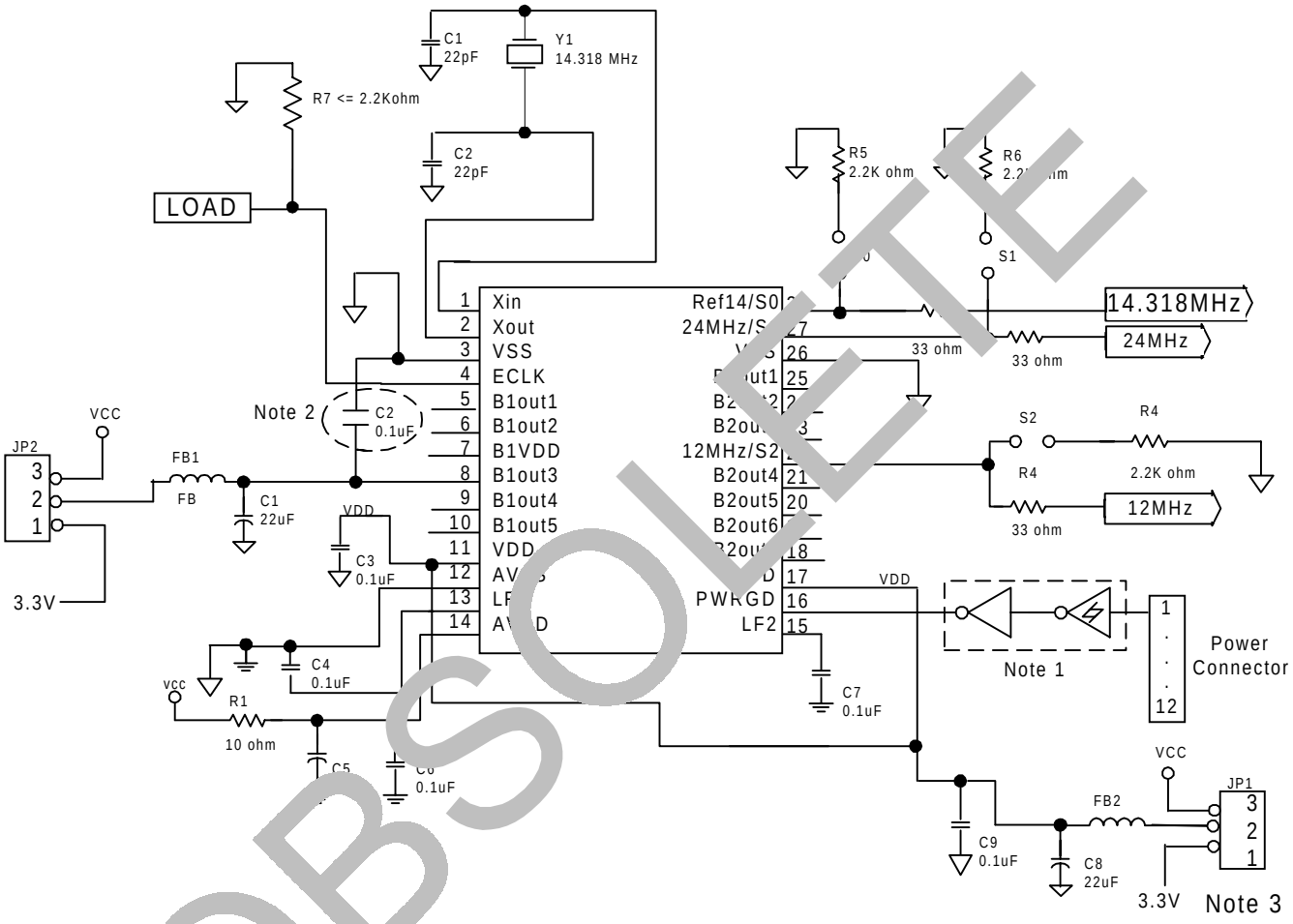
## APPLICATION SUGGESTION (Update)

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1. For 2.5 ns buffer delay place a resistor R7(≤ 5 kΩ).
2. For a 4.5 ns delay remove R7 and leave open.

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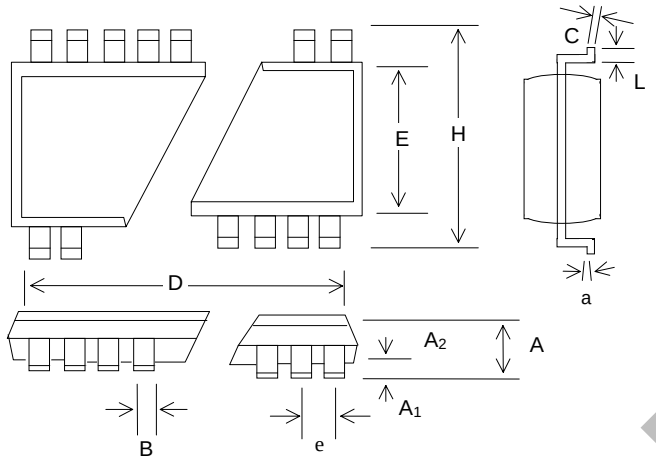
## PACKAGE DRAWING AND DIMENSIONS




**28 PIN SSOP OUTLINE DIMENSIONS**

| SYMBOL | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.068 | 0.073 | 0.078 | 1.73 | 1.86 | 1.99 |
| $A_1$ | 0.002 | 0.005 | 0.008 | 0.05 | 0.13 | 0.21 |
| $A_2$ | 0.066 | 0.070 | 0.070 | 1.68 | 1.73 | 1.78 |
| B | 0.010 | 0.012 | 0.015 | 0.25 | 0.30 | 0.38 |
| C | 0.005 | 0.006 | 0.009 | 0.13 | 0.15 | 0.22 |
| D | 0.397 | 0.402 | 0.407 | 10.07 | 10.20 | 10.33 |
| E | 0.205 | 0.209 | 0.212 | 5.20 | 5.30 | 5.38 |
| e | 0.0256 BSC | | | 0.65 BSC | | |
| H | 0.301 | 0.307 | 0.311 | 7.65 | 7.80 | 7.90 |
| a | 0º | 4º | 8º | 0º | 4º | 8º |
| L | 0.022 | 0.030 | 0.037 | 0.55 | 0.75 | 0.95 |

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## ORDERING INFORMATION

| Part Number | Package Type | Production Flow |
|---|---|---|
| IMISC485BYB | 28 PIN SSOP | Commercial, 0ºC to 70ºC |

Marking: IMI
SC485BYB
Date Code Lot #

IMISC485BY

**Flow**

B = Commercial, 0ºC to 70ºC

**Package**

SSOP

**Revision**

**IMI Device Number**