SC464

Motherboard Clock Chip

Approved Product

PRODUCT FEATURES

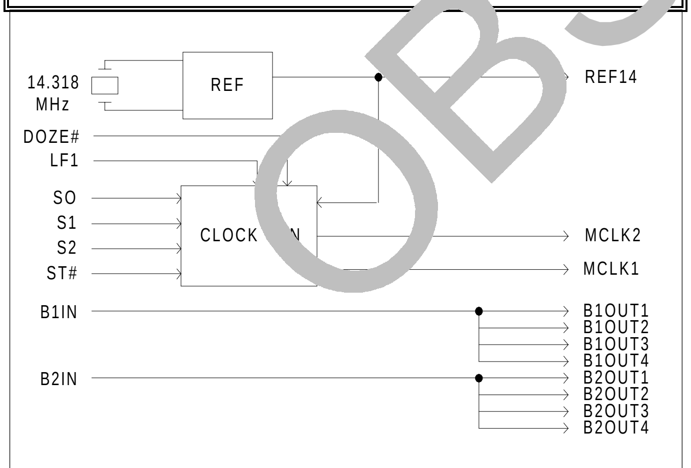
- Generates All Essential Clock Signals for the Motherboards
- 4V to 7V Operating Supply Range
- Supports 8086, 80286, 80386 and 80486 Including S Series ® and Pentium™ Based Designs
- Supports ISA, VESA, and PCI Based Designs
- Supports GREEN PC Applications
- On-Chip Dual Quad Buffers
- Integrates CPU Clock and Buffered 14.318 MHz Output
- Wide Range of Selectable Output Frequencies Including 80, 66.6, 60, 50, 40, 33.3, 30, 25, 16 and 8 MHz.
- Doze Mode for Low Power Consumption
- Single, Low Cost Crystal (14.318 MHz Used as Reference Frequency
- Smooth and Glitch-Free Switching for Programmable Clock Generator
- 50% Duty Cycle
- TTL or CMOS compatible Outputs
- Low, Short and Long Term Jitter
- 28 PDIP and 28 Pin SSOP (209 Mil Bod[illegible]ckag[illegible] Options

IMISC464 eliminates the need for multiple oscillators and generates all the essential clock signals for the Personal Computer Motherboards. Supports 8086, 80286, 80386SX, 80386DX, 80486SX, 80486DX, 80486DX2, 80486 S Series ® and Pentium™ based designs. IMISC464 can be us[illegible] with Green PC, laptop or notebook computers to [illegible]ve power by running the system slower than norma[illegible] CPU sp[illegible]eds.

FREQUENCY TABLE

INPUTS			MCLK1 AND MCLK2 OUTPUTS (MHz)		
				DOZE# = 0	
S2	S1	S0	DOZE# = 1	ST# = 1	ST# = 0
0	[illegible]	0	66.6	33.3	16
0	0	[illegible]	[illegible]	16	8
0	1	[illegible]	60	33.3	16
0	1	1	30	8	4
1	0	0	33.3	8	4
[illegible]	0	1	40	8	4
1	1	0	50	8	16
1	[illegible]	1	25	8	4

BLOCK DIAGRAM



SSOP/P-DIP PACKAGE

Signal	Pin	Pin	Signal
OSCin	1	28	REF14
OSCout	2	27	B2in
B1in	3	26	VSS
VSS	4	25	MCLK2
B1out1	5	24	MCLK1
B1out2	6	23	B2out4
VDD	7	22	B2out3
B1out3	8	21	B2out2
B2out4	9	20	B2out1
S1	10	19	VSS
S0	11	18	ST#
AVSS	12	17	S2
LF1	13	16	VDD
AVDD	14	15	DOZE#

APPLICATIONS

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PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). OSCin may also serve as an input for an externally generated reference signal.

S0, S1, and S2 - Standard frequency select inputs. These inputs control the high speed MCLK frequency selection. S0-S2 inputs control the CPU clock frequencies. All these inputs have internal pull-ups. Frequency table shows the output frequency selection conditions.

MCLK1 and MCLK2 - Synchronous master clock outputs. Programmable output frequencies can be selected using S0 - S2 inputs shown in Frequency table.

DOZ**E#** - Doze control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, MCLK1 and MCLK2 frequencies are switched to the pre-programmed DOZE frequencies. Switching to DOZE frequencies occur smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.

REF14 - 14.31818 MHz output. Buffered output of on-chip reference oscillator or externally provided reference.

LF1 - This is the phase detector output for the clock generator. It is a single ended, tri-state output for use as a loop error signal. A 1uF capacitor to ground should be connected from this pin to form the loop filter.

VSS - Circuit Ground

VDD - Positive power supply.

AVSS - Analog circuit ground

AVDD - Analog positive power supply.

ST # - When this pin is active low, MCLK20 stops after 1.1ms. When this pin is deactive, MCLK20 starts up immediately.

RESUME # - When ST# pin is active low, Resume# pin goes to zero immediately. When ST# pin is deactive, Resume# in goes to high after 1.1ms.

MAXIMUM RATINGS

Input Voltage Relative to VSS:	-0.3V to 7V
Input Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to 150ºC
Ambient Temperature:	0ºC to 70ºC
Recommend Operating Range:	4.5 - 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS < (Vin or Vout) < VDD

Unused inputs must always be tied to an appropriate logic voltage level (ever VSS or VDD).

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	DOZE#, ST#, S0-S2 Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	DOZE#, ST#, S0-S2 Inputs
Input Low Voltage	VIL	-	-	0.8	Vdc	B1in, B2in Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	B1in, B2in Inputs
Input Low Current with Pull- up or Pull-down	IIL	-	-	5 ±50	µA	DOZE#, ST#, S0-S2 Inputs
Input High Current with Pull-up or Pull-down	IIH		-	5 ±50	µA	DOZE#, ST#, S0-S2 Inputs
Output Low Voltage IOL = 12mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH=12mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State leakage Current	Ioz	-	-	10	µA	LF1
Dynamic Supply Current	Icc	-	-	35	mA	VDD@ 5V, MCLK2 = 50 MHz
Short Circuit Current	ISC	25	-		mA	

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V - 0.8V) Time MCLK and REF14 Outputs	**t**TLH **t**THL	-		2	ns	30 pf Load
Duty Cycle - MCLK and REF14			50/50	45/55	%	-
Propagation Delay - Bin to Bout	**t**TLH, **t**THL	[illegible].0	3.2	4.2	ns	15 pf Load Measured at 1.4V
Buffer Out Skew B1out1-B1out4 or B2out-B2out4	**t**SKEW	-	-	250	ps	15 pf Load Measured at 1.4V
Jitter One Sigma MCLK and REF14	**t**j1s	-	-	±2	%	As Compared with Clock Period
Jitter Absolute MCLK and REF14	**t**jab	-	-	±5	%	As Compared with Clock Period
Input Rise/Fall Time S0-S3	-	-	-	2	µs	-

VDD = 5V±10%, TA = 0°C to 70°C

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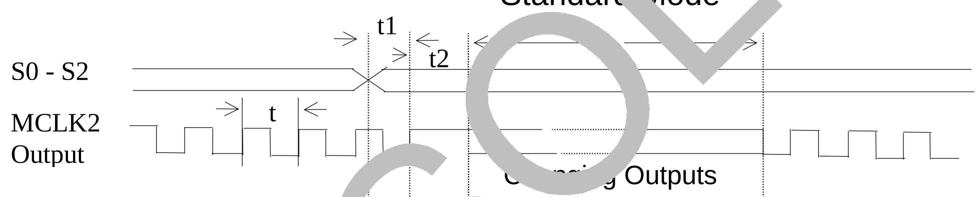
OSCILLATOR CHARACTERISTICS						
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	gm	20	330	-	Millimhos	@14.3 MHz
Output Impedance	Zo	-	200	800	ohms	@14.3 MHz
Input Capacitance	Ci	8	13	18	pf	-
Output Capacitance	Co	3	6	9	pf	-
DC Bias Voltage	VB	1.5	VDD/2	3.5	Volt	-
Start-up Time	ts	-	-	10	µs	@14.3 MHz
Input Rise Time OSCIN	ICLKr	-	-	2	µs	-
Input Fall Time OSCIN	ICLKf	-	-	2	µs	-
VDD = 5V±10%, TA = 0°C to 70°C						

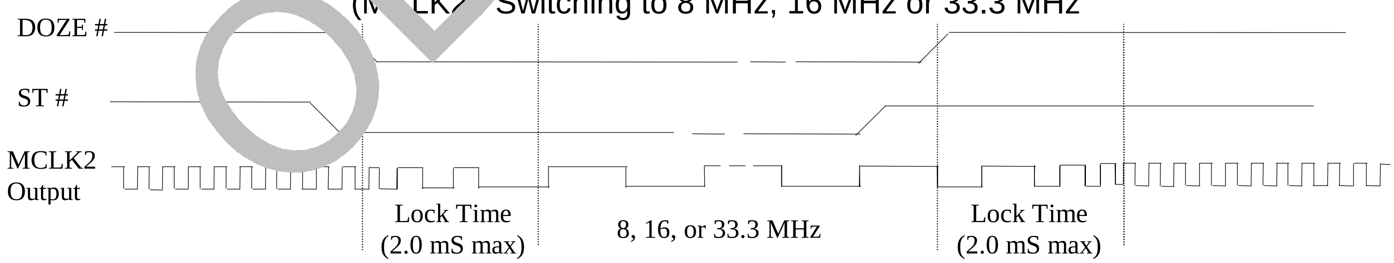
TIMING DIAGRAMS

Standard Mode



t: Current cycle time
t1: Time to first positive edge after address change
t2: Ouput high time. t2 [illegible] 4
t3: Lock time. 2.0ms max

DOZE Mode
(MCLK2 Switching to 8 MHz, 16 MHz or 33.3 MHz



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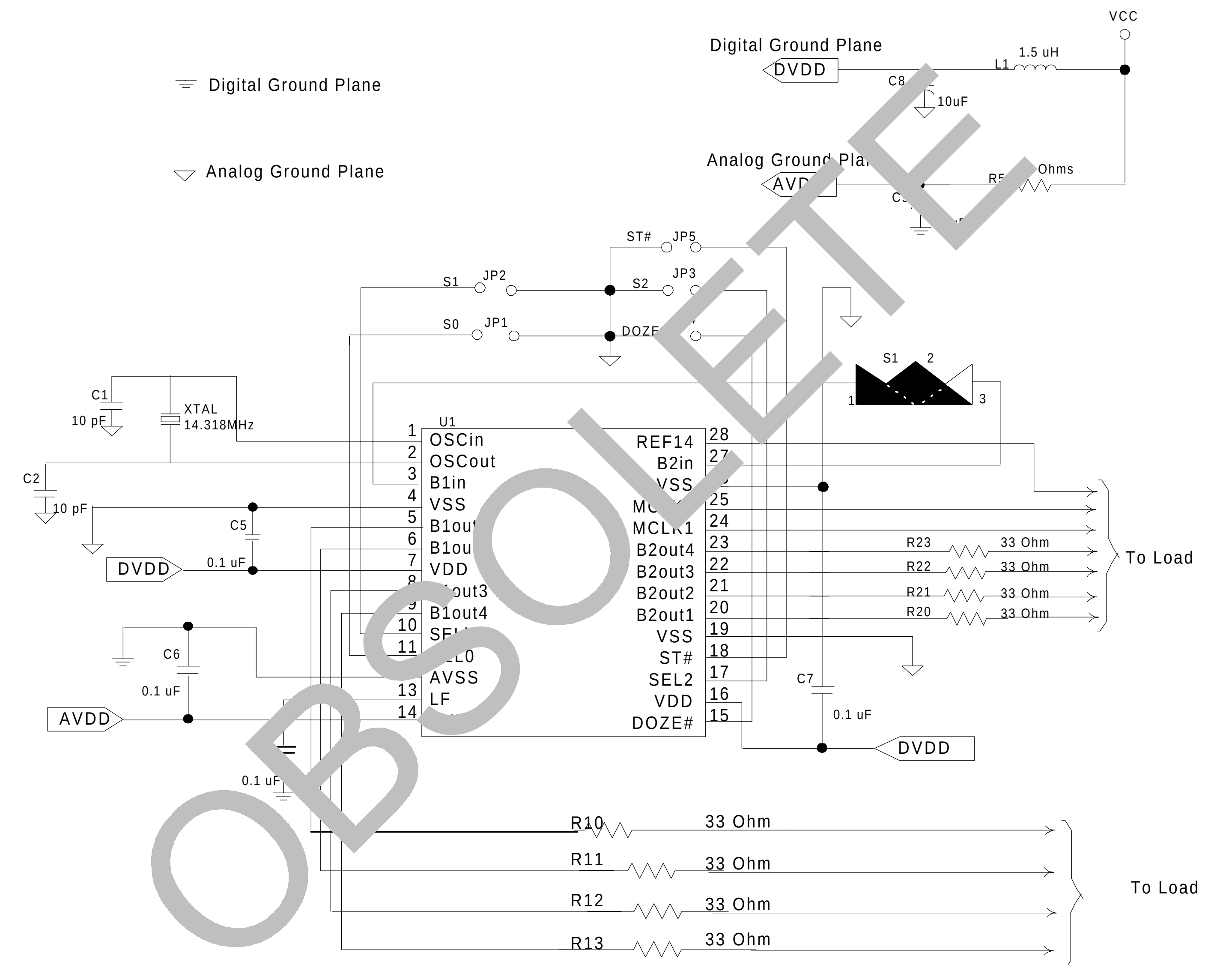
APPLICATION SUGGESTION



NOTE 1: C3, C5, C6, C7 must be close to their pins.

NOTE 2: R10, R11, R12, R13 are close to their pins with equal traces to the probe holes. R20, R21, R22, R23 are close to their pins with equal traces to the probe holes.

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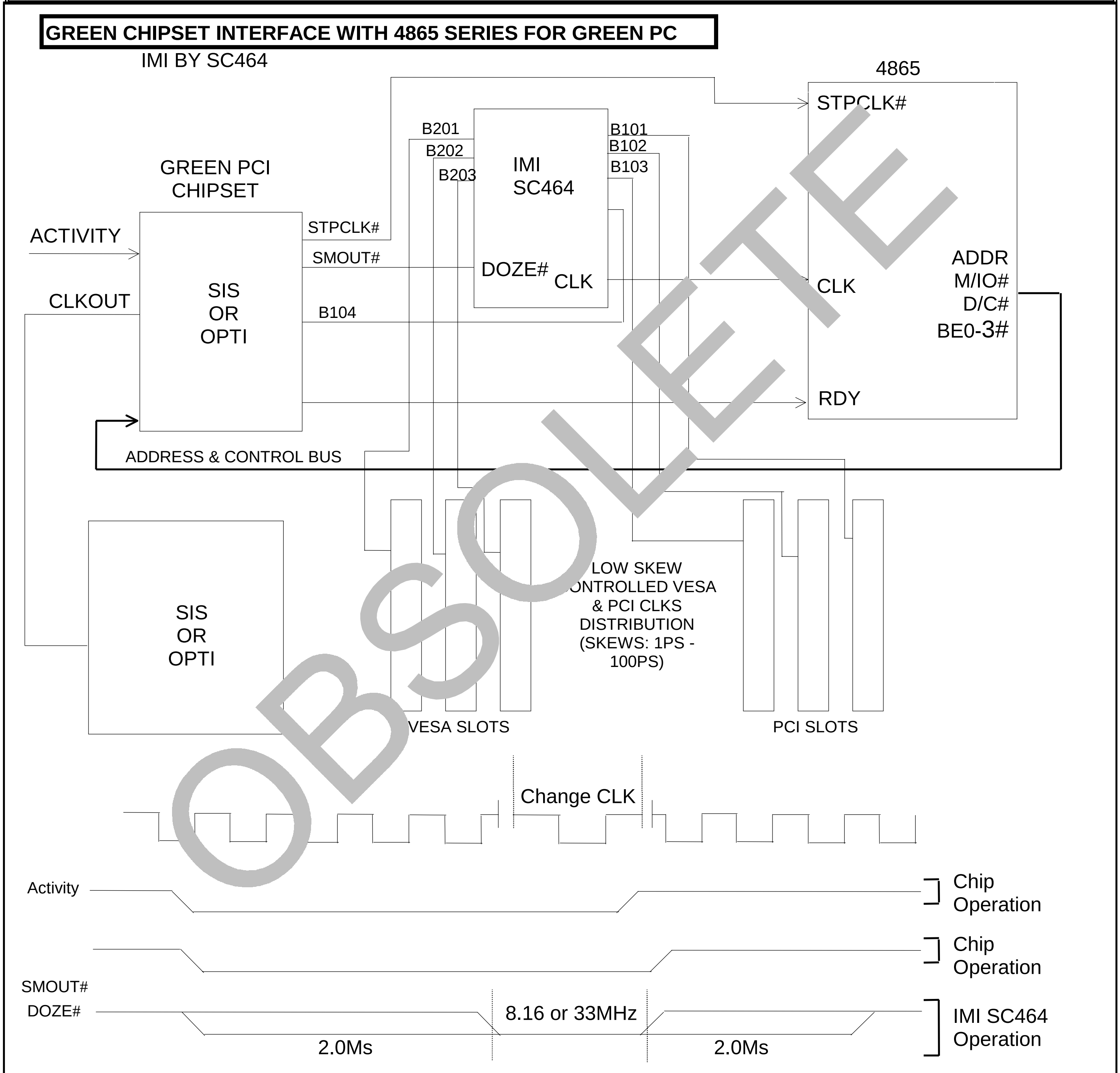
APPLICATION DIAGRAM



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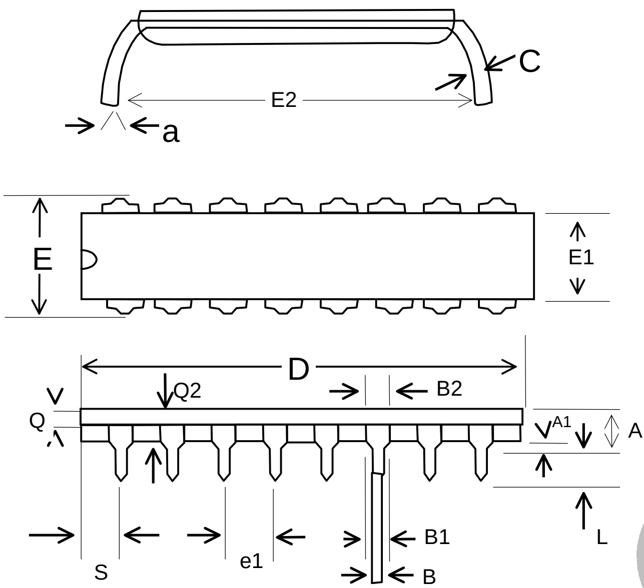
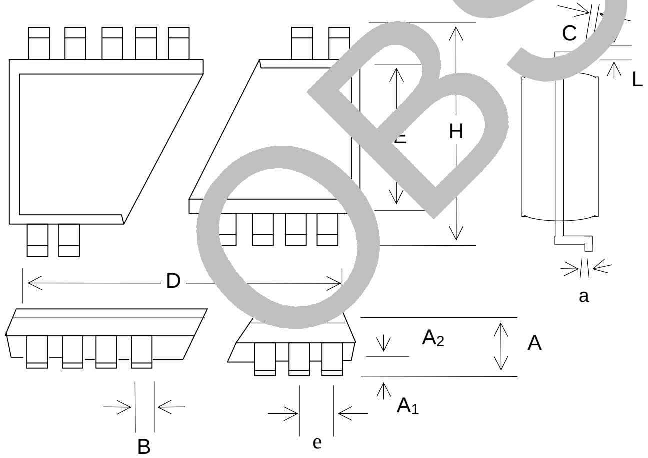
PACKAGE DRAWINGS AND DIMENSIONS



28 PIN SKINNY PLASTIC DIP DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-		[illegible]	-	-	4.57
A_1	0.020	-		[illegible]	-	-
B	[illegible]	0.0.8	[illegible]	0.38	0.46	0.51
B_1	0.045	0.050	0.055	1.14	1.27	1.40
B_2	0.035	[illegible]	0.045	0.89	1.02	1.14
C	0.008	0.010	0.012	0.20	0.25	0.30
D	1.360	1.365	1.370	34.54	34.67	34.80
E	0.300		0.325	7.62	-	8.255
E_1	0.280	0.282	0.284	7.11	7.16	7.2`
E_2	[illegible]	0.284	0.286	7.16	7.21	7.25
e_1	0.100 BSC			2.54 BSC		
L	0.128	0.130	0.135	3.18	3.30	3.43
	0°	7°	15°	0°	7°	15°
Q_1	0.055	0.060	0.065	1.40	1.52	1.65
Q_2	-	130	-	-	3.30	-
S	0.028	0.033	0.038	0.71	0.84	0.97



28 PIN SSOP OUTLINE DIMENSIONS						
	MILLIMETERS			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.078	1.73	1.8	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC464APB	28 Pin Plastic Dip	Commercial, 0° C to + 70° C
IMISC464AYB	28 Pin SSOP	Commercial, 0°C to + 70°C

Marking: Example: IMI
SC464APB
Date Code
Lot #

IMISC464APB

Flow

B = Commercial, 0°C to 70°C

Package

P = Plastic Dip
Y = SSOP

Revision

IMI Device Number