Integrated Device Technology, Inc.

3.3V PHASE-LOCK LOOP CLOCK DRIVER

IDTCSP2510B
ADVANCE INFORMATION

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of ten outputs
- Output enable bank control
- External feedack (FBIN) pin is used to synchronize the outputs to the clock input signal
- On-chip series damping resistors with each driver
- No external RC network required for PLL loop stability
- Operates at 3.3V VCC
- Plastic 24-pin Thin Shrink Small-Outline package
- tpd Phase Error at 100MHz: < ±150ps
- Jitter (peak-to-peak) at 100MHz: < ±80ps
- Jitter (cycle-to-cycle) at 100MHz: < ±50ps

APPLICATIONS:

- SDRAM modules
- PC motherboards

DESCRIPTION:

The IDTCSP2510B is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2510B operates at 3.3V and provides integrated series-damping resistors that make it ideal for driving point-to-point loads, single or dual.

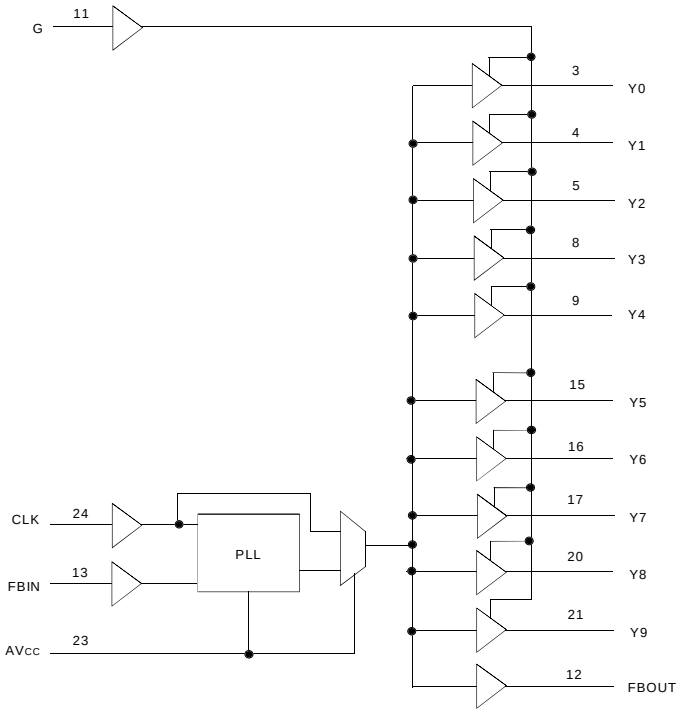
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control G input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2510B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

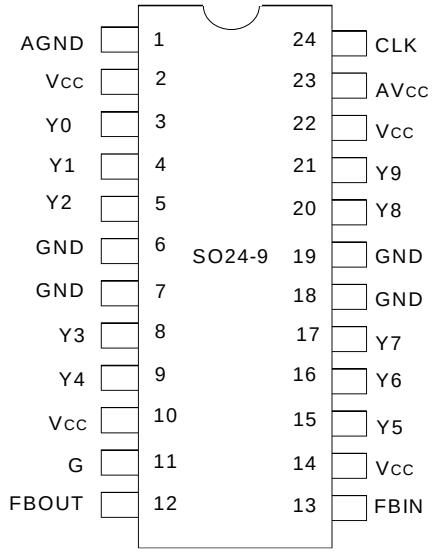
Because it is based on PLL circuitry, the CSP2510B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AVCC to ground.

The CSP2510B is characterized for operation from 0°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(1)	Input Voltage Range	–0.5 to +6.5	V
V_O(1,2)	Voltage range applied to any output in the high or low state	–0.5 to V_{CC} + 0.5	V
I_{IK} (V_I <0)	Input clamp current	–50	mA
I_{OK} (V_O <0 or V_O > V_{CC})	Terminal Voltage with Respect to GND (inputs $V_{IH2.5}$, $V_{IL2.5}$)	±50	mA
I_O (V_O =0 to V_{CC})	Continuous Output Current	±50	mA
V_{CC} or GND	Continuous Current	±100	mA
T_A = 55°C (in still air) (3)	Maximum Power Dissipation	0.7	W
T_{STG}	Storage Temperature Range	–65°C to +150°C	°C

NOTES:
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE(1)

Parameter	Description	Min.	Typ.	Max.	Unit
T_A	Operating Temperature (Ambient Temperature)	0		+85	°C
C_{IN}	Input Capacitance Vi = Vcc or GND		5		pF
C_O	Output Capacitance Vo = Vcc or GND		6		pF
C_L	Load Capacitance		30		pF

NOTE:
1. Unused inputs must be held high or low to prevent them from floating.

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CSP2510B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25Ω series-damping resistor.
Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by deasserting the G control input. Each output has an integrated 25Ω series-damping resistor.
AVCC	23	Power	Analog power supply. AVCC provides the power reference for the analog circuitry. In addition, AVCC can be used to bypass the PLL for test purposes. When AVCC is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	2, 10, 14, 22	Power	Power supply.
GND	6, 7, 18, 19	Ground	Ground.

STATIC FUNCTION TABLE (AVCC = 0V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
L	L	L	L
L	H	L	H
H	H	H	H
H	L	L	L
H	running	running	running

DYNAMIC FUNCTION TABLE (AVCC = 3.3V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
X	L	L	L
L	running	L	running in phase with CLK
L	H	L	H
H	running	running in phase with CLK	running in phase with CLK
H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions	Vcc	Min.	Typ.(1)	Max.	Unit
V_{IK}	I_I = –18 mA	3V			–1.2	V
V_{OH}	I_{OH} = –100 µA	Min. to Max.	V_{CC}–0.2			V
	I_{OH} = –12 mA	3V	2.1			
	I_{OH} = –6 mA	3V	2.4			
V_{OL}	I_{OL} = 100 µA	Min. to Max.			0.2	V
	I_{OL} = 12 mA	3V			0.8	
	I_{OL} = 6 mA	3V			0.55	
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{CC}	V_I = V_{CC} or GND, AV_{CC} = 3.3V, I_O = 0, Outputs: low or high	3.6V				µA
ΔI_{CC}	One input at V_{CC} –0.6V, Other inputs at V_{CC} or GND	3.3V to 3.6V			500	µA
I_{CCA}(2)	AV_{CC} Power Supply Current	AV_{CC} = 3.3V		10		mA

NOTES:
1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. For I_{CC} of AV_{CC}, see Figure 4.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

		Min.	Max.	Unit
f_{CLOCK}	Clock frequency	25	125	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time(1)		1	ms

NOTE:
1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30PF(1) (SEE FIGURES 1 AND 2)

Parameter	From (Input)	To (Output)	Vcc = 3.3V ± 0.165V			Vcc = 3.3V ± 0.3V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHASE} error	60MHz < CLK↑ < 125MHz (Fig. 2 and 3)	FBIN↑				–- 200		200	ps
t_{PHASE} error – jitter(2)	CLK↑ = 66MHz to 100MHz (Fig. 2 and 3)	FBIN↑	– 150		150				ps
$t_{SK\ (o)}$(3)	Any Y or FBOUT	Any Y or FBOUT						200	ps
Jitter (cycle-to-cycle)	CLK = 66MHz to 100MHz (Fig. 6)	Any Y or FBOUT				– 50		50	ps
Jitter (pk-pk)	CLK = 66MHz to 100MHz (Fig. 6)	Any Y or FBOUT				– 80		80	ps
Duty cycle reference	CLK ≥ 60MHz (Fig. 4)	Any Y or FBOUT				45		55	%
t_R		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns
t_F		Any Y or FBOUT		1.7	2.5	1.2		2.7	ns

NOTES:
1. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
2. Phase error does not include jitter. The total phase error is -250ps to 250ps for the 5% V_{CC} range.
3. The tSK(o) specification is only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION(2)

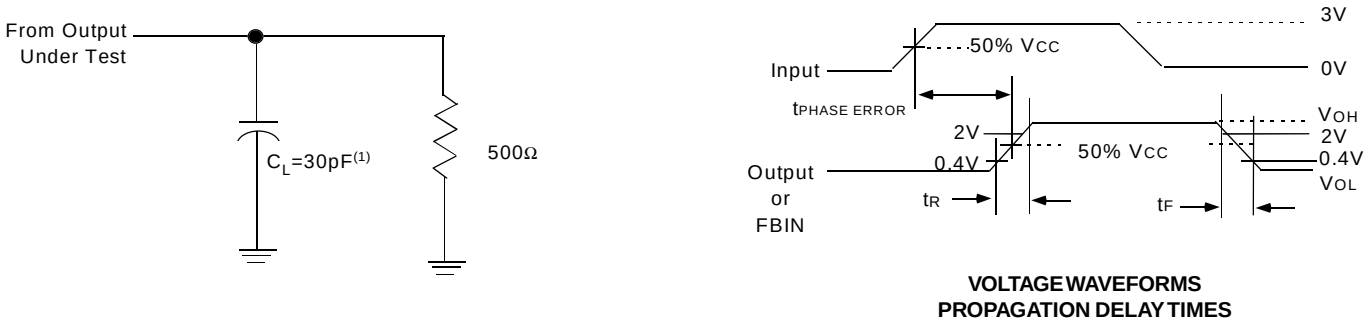


Figure 1. Load Circuit and Voltage Waveforms

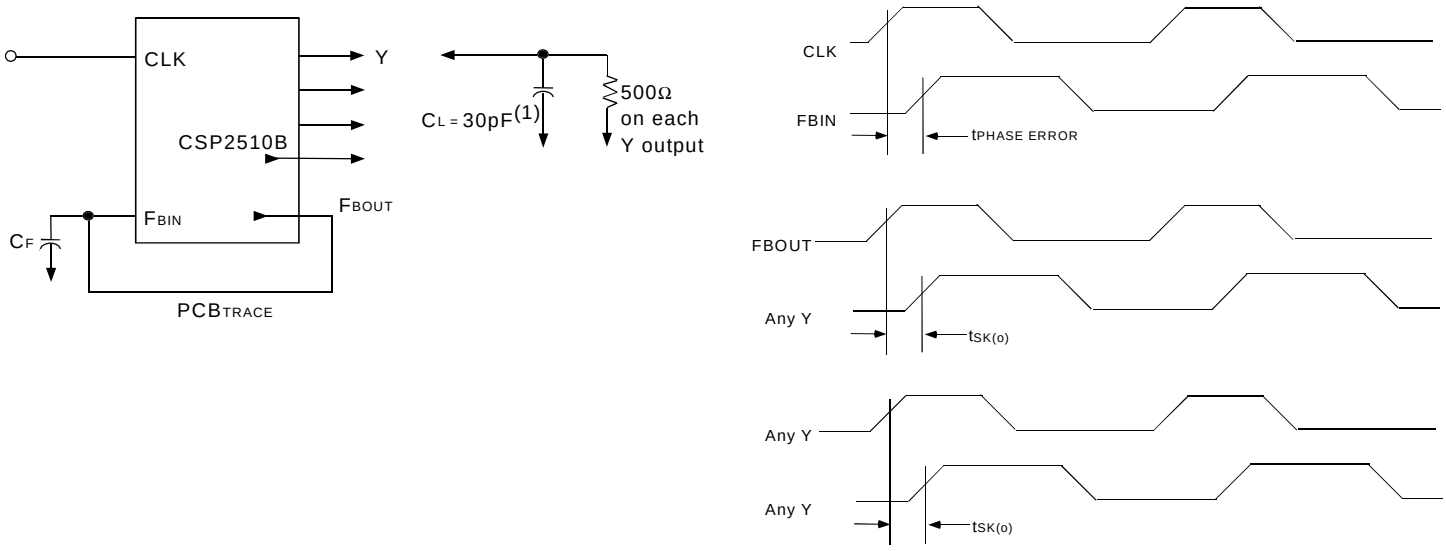


Figure 2. Phase Error and Skew Calculations (3) (4)

NOTES:
1. CL includes probe and jig capacitance.
2. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz ZO = 50Ω, tR ≤ 1.2 ns, tF≤ 1.2 ns.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. $C_F = C_L - C_{FBIN} - C_{PCB_{TRACE}}$; $C_{FBIN} \cong 6pF$.

TYPICAL CHARACTERISTICS

STATIC PHASE ERROR VS. CLOCK FREQUENCY

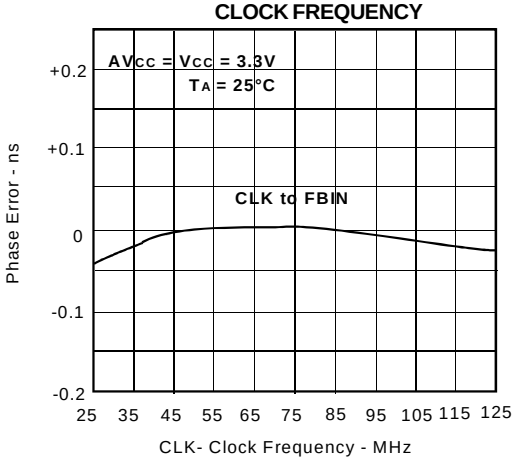


FIGURE 3

OUTPUT DUTY CYCLE VS. CLOCK FREQUENCY

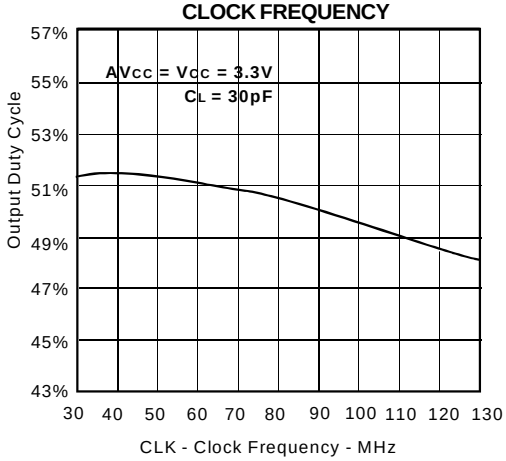


FIGURE 4

ANALOG SUPPLY CURRENT VS. CLOCK FREQUENCY

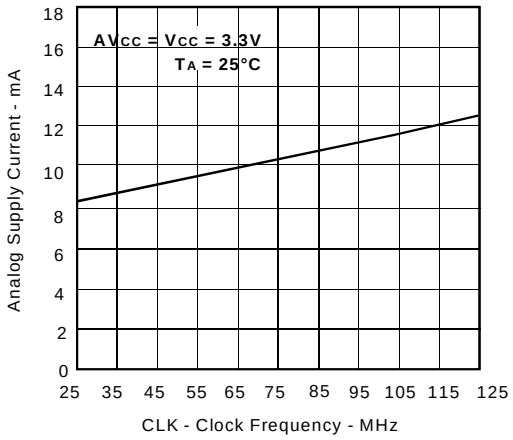


FIGURE 5

JITTER (CYCLE-TO-CYCLE AND PEAK-TO-PEAK) VS. CLOCK FREQUENCY

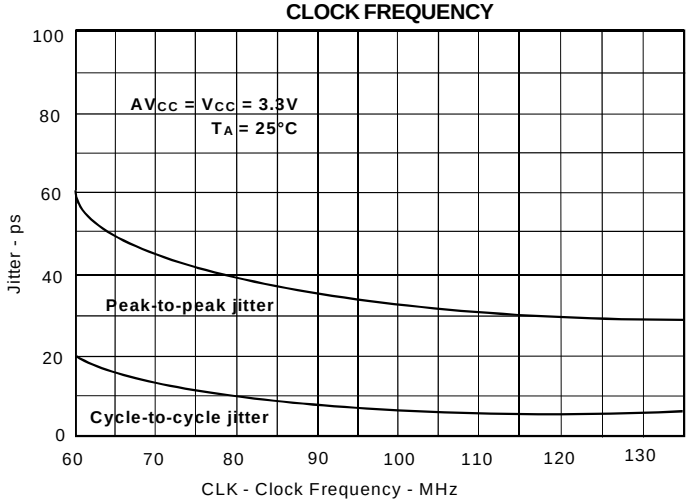


FIGURE 6

PHASE ERROR VS. LOAD CAPACITANCE

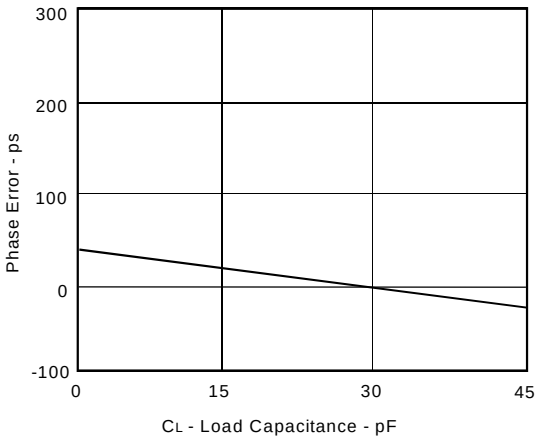


FIGURE 7

ORDERING INFORMATION