Integrated Device Technology, Inc.

3.3V PHASE-LOCK LOOP CLOCK DRIVER

IDTCSP2509B

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of five and one bank of four outputs
- Separate output enable for each output bank
- External feedack (FBIN) pin is used to synchronize the outputs to the clock input
- One-chip series damping resistors
- No external RC network required
- Operates at 3.3V VCC
- Plastic 24-pin Thin Shrink Small-Outline package

APPLICATIONS:

- SDRAM modules
- PC motherboards

DESCRIPTION:

The CSP2509B is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2509B operates at 3.3V VCC and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

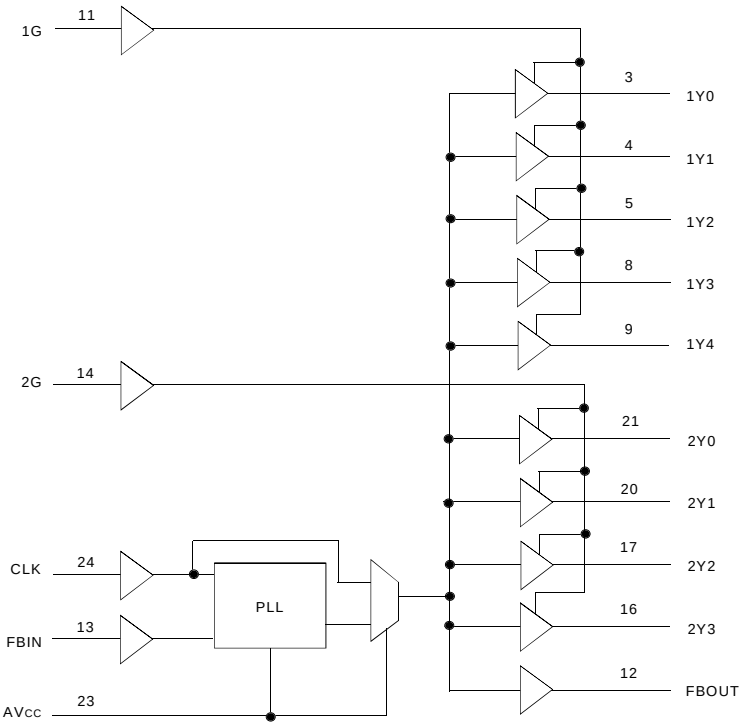
One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2509B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CSP2509B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AVCC to ground.

The CSP2509B is characterized for operation from 0°C to +85°C.

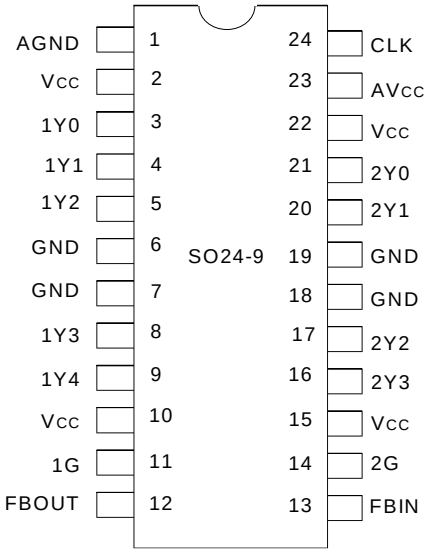
FUNCTIONAL BLOCK DIAGRAM



0 to +85°C TEMPERATURE RANGE **FEBRUARY 1999**

DSC-4684/3

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{CC}, AV_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to +6.5	V
V_O(2)	Voltage range applied to any output in the high or low state	–0.5 to V_{CC} + 0.5	V
I_{IK} (V_I <0)	Input clamp current	–50	mA
I_{OK} (V_O <0 or V_O > V_{CC})	Terminal Voltage with Respect to GND (inputs $V_{IH2.5}$, $V_{IL2.5}$)	±50	mA
I_O (V_O =0 to V_{CC})	Continuous Output Current	±50	mA
V_{CC} or GND	Continuous Current	±100	mA
T_A = 55°C (in still air) (3)	Maximum Power Dissipation	0.7	W
T_{STG}	Storage Temperature Range	–65°C to +150°C	°C

NOTES:
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE(1)

Parameter	Description	Min.	Typ.	Max.	Unit
T_A	Operating Temperature (Ambient Temperature)	0		+85	°C
C_{IN}	Input Capacitance Vi = Vcc or GND		5		pF
C_O	Output Capacitance Vo = Vcc or GND		6		pF
C_L	Load Capacitance		30		pF

NOTE:
1. Unused inputs must be held high or low to prevent them from floating.

STATIC FUNCTION TABLE (AVCC = 0V)

Inputs			Outputs		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
L	L	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

DYNAMIC FUNCTION TABLE (AVCC = 3.3V)

Inputs			Outputs		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
L	L	running	L	L	running in phase with CLK
L	H	running	L	running in phase with CLK	running in phase with CLK
H	L	running	running in phase with CLK	L	running in phase with CLK
H	H	running	running in phase with CLK	running in phase with CLK	running in phase with CLK

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CSP2509B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic-low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25Ω series-damping resistor.
2Y (0:3)	16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25Ω series-damping resistor.
AVCC	23	Power	Analog power supply. AVCC provides the power reference for the analog circuitry. In addition, AVCC can be used to bypass the PLL for test purposes. When AVCC is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VCC	2, 10, 15, 22	Power	Power supply.
GND	6, 7, 18, 19	Ground	Ground.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions	Vcc	Min.	Typ.(1)	Max.	Unit
V_{IK}	I_I = –18 mA	3V			–1.2	V
V_{OH}	I_{OH} = –100 µA	Min. to Max.	V_{CC}–0.2			V
	I_{OH} = –12 mA	3V	2.1			
	I_{OH} = –6 mA	3V	2.4			
V_{OL}	I_{OL} = 100 µA	Min. to Max.			0.2	V
	I_{OL} = 12 mA	3V			0.8	
	I_{OL} = 6 mA	3V			0.55	
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{CC}	V_I = V_{CC} or GND, AV_{CC} = 3.3V, I_O = 0, Outputs: low or high	3.6V			10	µA
ΔI_{CC}	One input at V_{CC} –0.6V, Other inputs at V_{CC} or GND	3.3V to 3.6V			500	µA
C_{PD}	Power Dissipation Capacitance	3.6V		10	14	pF
I_{CCA}(2)	AV_{CC} Power Supply Current	AV_{CC} = 3.3V		10		mA

NOTES:
1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. For I_{CC} of AV_{CC}, see Figure 5.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

		Min.	Max.	Unit
CLK	Clock frequency	25	125	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time(1)		1	ms

NOTE:
1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30PF(2) (SEE FIGURES 1 AND 2)

			Vcc = 3.3V ±0.165V			Vcc = 3.3V ±0.3V			
Parameter	**From (Input)**	**To (Output)**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{PHASE} error	80MHz < CLK↑ < 100MHz (Fig. 2 and 3)	FBIN↑				–- 200		200	ps
t_{PHASE} error – jitter(3)	CLK↑ = 100MHz (Fig. 2 and 3)	FBIN↑	– 150		150				ps
$t_{SK\ (o)}$(1)	Any Y (100MHz)	Any Y						200	ps
Jitter (cycle-to-cycle)	CLK = 100MHz (Fig. 6)	Any Y or FBOUT				– 50		50	ps
Jitter (pk-pk)	CLK = 100MHz (Fig. 6)	Any Y or FBOUT				– 100		100	ps
Duty cycle reference	CLK ≥ 80MHz (Fig. 4)	Any Y or FBOUT				45		55	%
t_R		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns
t_F		Any Y or FBOUT		1.7	2.5	1.2		2.7	ns

NOTES:
1. The tSK(o) specification is only valid for equal loading of all outputs.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.

PARAMETER MEASUREMENT INFORMATION

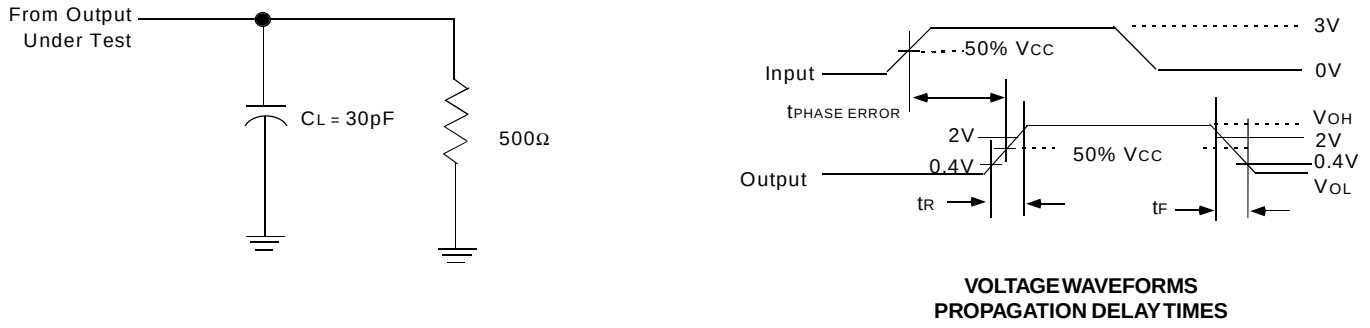


Figure 1. Load Circuit and Voltage Waveforms

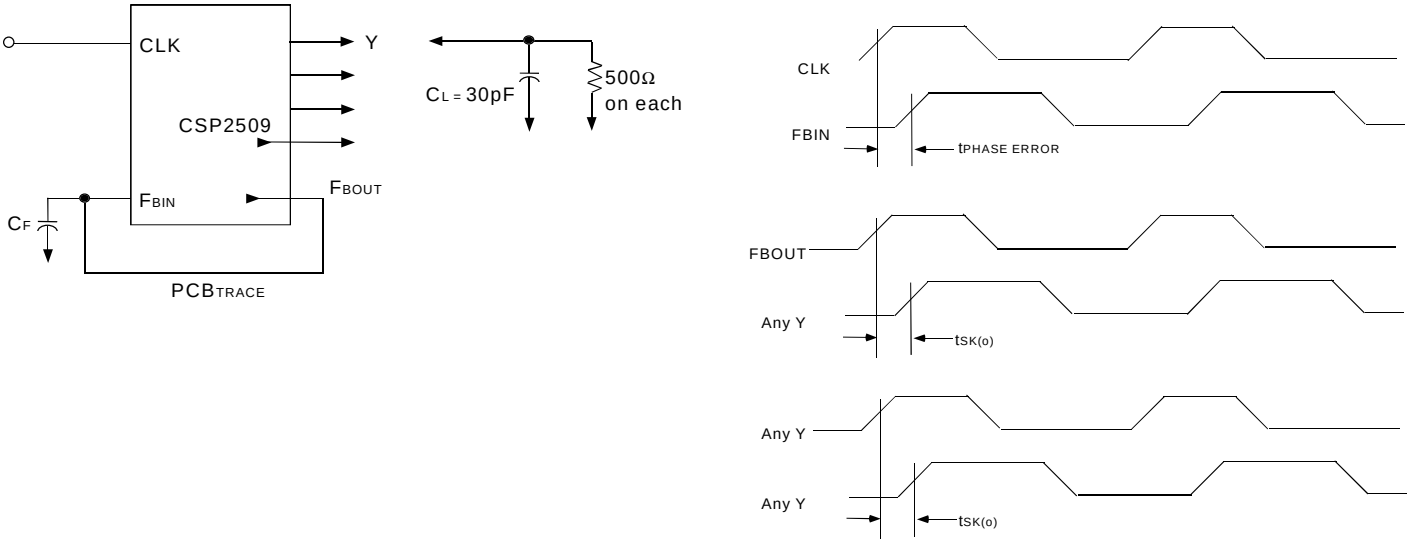


Figure 2. Phase Error and Skew Calculations

NOTES:
1. CL includes probe and jig capacitance.
2. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz ZO = 50Ω, tR ≤ 1.2 ns, tF≤ 1.2 ns.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. CF = CL – CFBIN – CPCBTRACE; CFBIN ≅ 6pF.

TYPICAL CHARACTERISTICS

STATIC PHASE ERROR vs CLOCK FREQUENCY

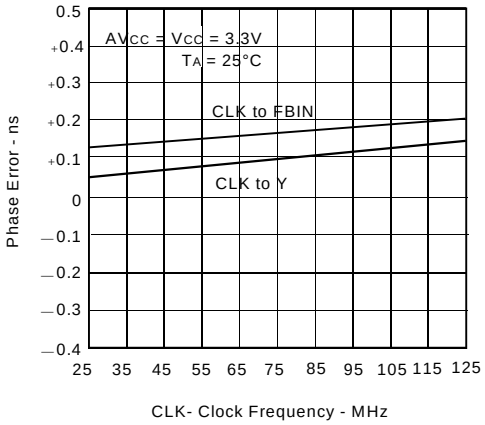


Figure 3.

OUTPUT DUTY CYCLE vs CLOCK FREQUENCY

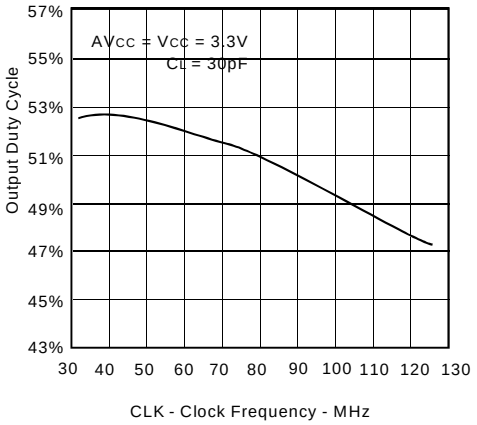


Figure 4.

ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY

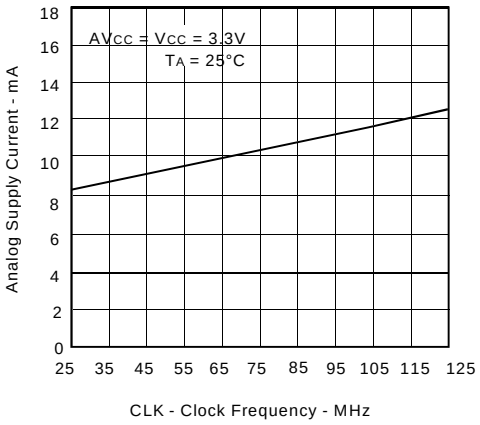


Figure 5.

JITTER (PEAK-TO-PEAK) VS. CLOCK FREQUENCY

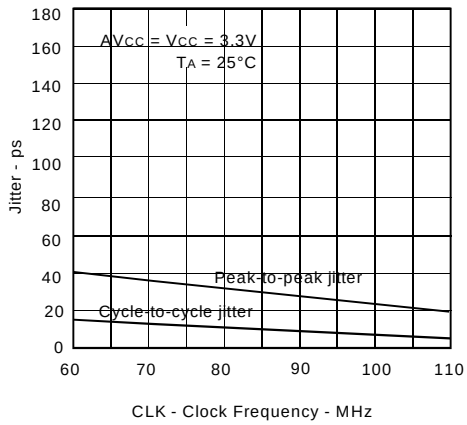


Figure 6.

ORDERING INFORMATION