I²C System Clock Buffer

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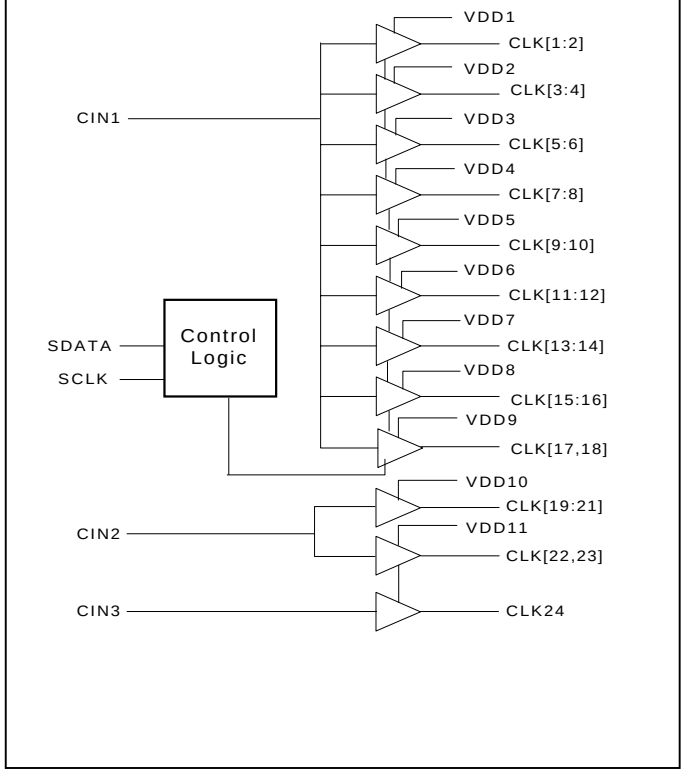
PRODUCT FEATURES

- 24 output buffer divided into 3 groups for high clock fanout applications for CPU and PCI clocks.
- Each output can be internally disabled for EMI reduction
- EMI is further reduced by requiring only 1 single long trace to the clock source.
- VDD= 3.3 volts for each clock group
- Output frequency range 30 Mhz to 126 Mhz
- < 250 ps skew between output clocks derived from the same input pin.
- < 500 ps skew between all output clocks when all input pins are connected together.
- 52-pin QFP package

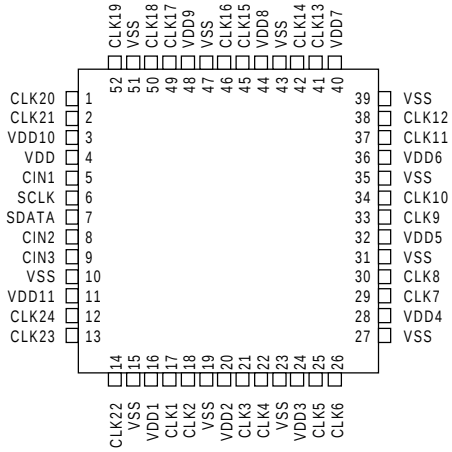
BLOCK DIAGRAM



PRODUCT DESCRIPTION

The device is a high fanout system clock buffer. Its primary application is to create the large quantity of clocks needed to support a wide range of applications that requires those clock loads signal that are referenced to a single existing clock. Loads of up to 30 pF are supported. One of the chief applications of this component is where long traces are used to transport clocks from their generating devices to their loads. The creation of EMI and the degradation of waveform rise and fall times is greatly reduced by running a single reference clock trace to this device and then using it to regenerate the clock that drives shorter traces. Using these devices EMI is therefore minimized and board real estate is saved.

CONNECTION DIAGRAM



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PIN DESCRIPTION

PIN No.	Pin Name	PWR	I/O	TYPE	Description
5	**CIN1**	VDD	I	PAD	This pin is connected to the input reference clock that drives output clocks CLK1 - CLK18. This clock must be in the range of 10.0 to 100.0 Mhz.
8	**CIN2**	VDD	I	PAD	This pin is connected to the input reference clock that drives output clocks CLK19 - CLK23. This clock must be in the range of 10.0 to 100.0 Mhz.
9	**CIN3**	VDD	I	PAD	This pin is connected to the input reference clock that drives output clocks CLK1 - CLK24. This clock must be in the range of 10.0 to 100.0 Mhz.
17, 18	**CLK(1:2)**	VDD1	O	BUF1	Low skew output clock
21, 22	**CLK(3:4)**	VDD2	O	BUF1	Low skew output clock
25, 26	**CLK(5:6)**	VDD3	O	BUF1	Low skew output clock
29, 30	**CLK(7:8)**	VDD4	O	BUF1	Low skew output clock
33, 34	**CLK(9:10)**	VDD5	O	BUF1	Low skew output clock
37, 38	**CLK(11:12)**	VDD6	O	BUF1	Low skew output clock
41, 42	**CLK(13:14)**	VDD7	O	BUF1	Low skew output clock
45, 46	**CLK(15:16)**	VDD8	O	BUF1	Low skew output clock
49, 50	**CLK(17:18)**	VDD9	O	BUF1	Low skew output clock
52, 1, 2	**CLK(19:21)**	VDD10	O	BUF1	Low skew output clock
12, 13, 14	**CLK(22:24)**	VDD11	O	BUF1	Low skew output clock
7	**SDATA**	-	I/O	PAD	Serial data of I²C 2-wire control interface. Has internal Pull-Up resistor.
6	**SDCLK**	-	I	PAD	Serial clock of I²C 2-wire control interface. Has internal Pull-Up resistor.
10, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51	**VSS**		PWR	-	Ground pins for clock output buffers. These pins must be returned to the same potential to reduce output clock skew.
16, 20, 24, 28, 32, 36, 40, 44, 48, 3, 11	**VDD(1:11)**	-	PWR	-	Power for output clock buffers. See individual buffer description for appropriate power pin commitment.
4	**VDD**	-	PWR	-	Power for core logic.

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2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on power up.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2,) will be valid and acknowledged.

Byte 0: Function Select Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	**30**	CLK8 (Active = 1, Forced low = 0)
6	1	**29**	CLK7 (Active = 1, Forced low = 0)
5	1	26	CLK6 (Active = 1, Forced low = 0)
4	1	25	CLK5 (Active = 1, Forced low = 0)
3	1	22	CLK4 (Active = 1, Forced low = 0)
2	1	21	CLK3 (Active = 1, Forced low = 0)
1	1	18	CLK2 (Active = 1, Forced low = 0)
0	1	17	CLK1 (Active = 1, Forced low = 0)

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SERIAL CONTROL REGISTERS (Cont.)

Byte 1: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	**46**	CLK16 (Active = 1, Forced low = 0)
6	1	**45**	CLK15 (Active = 1, Forced low = 0)
5	1	42	CLK14 (Active = 1, Forced low = 0)
4	1	41	CLK13 (Active = 1, Forced low = 0)
3	1	38	CLK12 (Active = 1, Forced low = 0)
2	1	37	CLK11 (Active = 1, Forced low = 0)
1	1	34	CLK10 (Active = 1, Forced low = 0)
0	1	33	CLK9 (Active = 1, Forced low = 0)

Byte 2: Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	**14**	CLK22 (Active = 1, Forced low = 0)
6	0	**13**	CLK23 (Active = 1, Forced low = 0)
5	0	12	CLK24 (Active = 1, Forced low = 0)
4	0	2	CLK21 (Active = 1, Forced low = 0)
3	0	1	CLK20 (Active = 1, Forced low = 0)
2	0	52	CLK19 (Active = 1, Forced low = 0)
1	0	50	CLK18 (Active = 1, Forced low = 0)
0	0	49	CLK17 (Active = 1, Forced low = 0)

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL	-66			µA	
Input High Current	IIH			66	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4 mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Frequency Input (all groups)	f_{IN}	50	-	105	Mhz	
Dynamic Supply Current	Idd_{66}	30	-	350	mA	Input frequency = 66 Mhz - All outputs on and at 30 pF load
	Idd_{100}	50	-	500	mA	Input frequency 100 Mhz - All outputs on and at 30 pF load
Static Supply Current	Isdd	-	-	35	mA	All outputs disabled no input clock
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDD1 thru VDD24 =3.3V ±5%, , TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V (with 50/50 input clock also measured at 1.5 V)
Buffer out/out Skew All Buffer Outputs	tSKEW	-	-	250	pS	30 pF Load Measured at 1.5V
Buffer input to output Skew	tSKEW	3.0	4.0	5.0	nS	+/- 20% over 0 to 70°C
Jitter Cycle to Cycle*	TJCC			100	pS	@ 30 pF loading at 100 Mhz
Jitter Absolute (Peak to Peak)*	TJabs			150	pS	@ 30 pF loading at 100 Mhz 5 Min sample
VDD = VDD1 thru VDD24 = 3.3V ±5%, , TA = 0ºC to +70ºC						

* this jitter is additive to the input clock's jitter.

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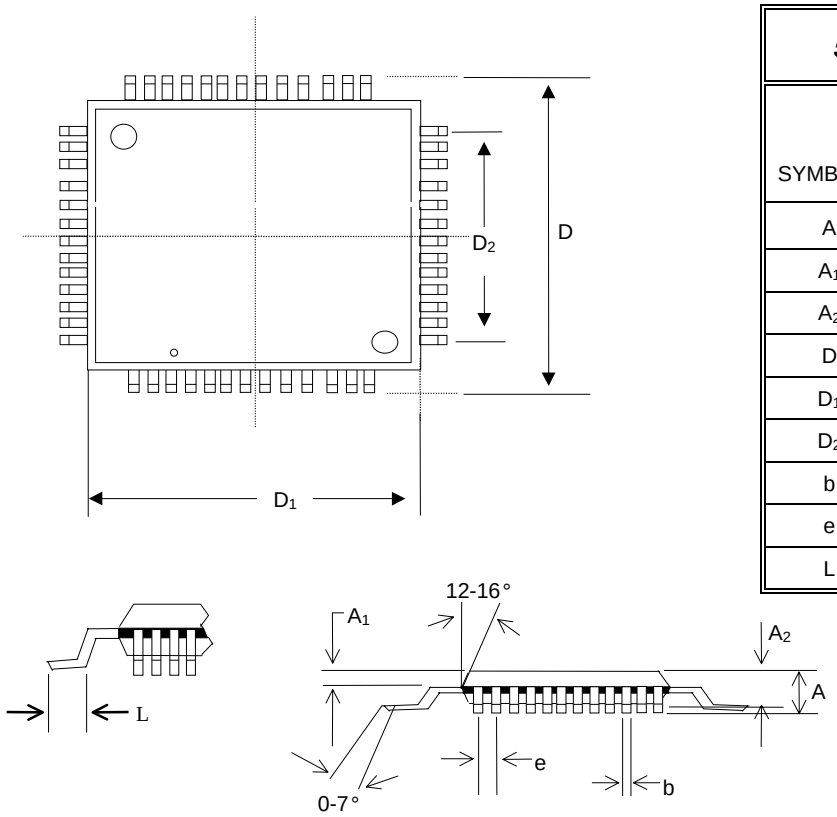
TYPE 1 BUFFER CHARACTERISTICS (ALL CLOCK OUTPUTS)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current Min	IOH_{min}	30	-	39	mA	Vout = 2.4V
Pull-Up Current Max	IOH_{max}	75	-	109	mA	Vout = 1.5V
Pull-Down Current Min	IOL_{min}	30	-	40	mA	Vout = .4V
Pull-Down Current Max	IOL_{max}	75	-	103	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	-	-	1.33	nS	30 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	1.33	nS	30 pF Load
VDD = VDD1 thru VDD24 =3.3V ±5***%, , TA = 0ºC to +70ºC***						

PACKAGE DRAWING AND DIMENSIONS



52 PIN QFP OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	0.084	0.093	-	2.13	2.35
A_1	.000	.006	.010	0.00	0.15	0.25
A_2	0.077	0.079	0.083	1.95	2.00	2.10
D	0.537	0.547	0.557	13.65	13.90	14.15
D_1	0.390	0.394	0.398	9.90	10.00	10.10
D_2	0.307 REF			7.80 REF		
b	0.009	-	0.015	0.22	-	0.38
e	.0256 BSC			0.65 BSC		
L	0.026	0.031	0.037	0.65	0.80	0.95

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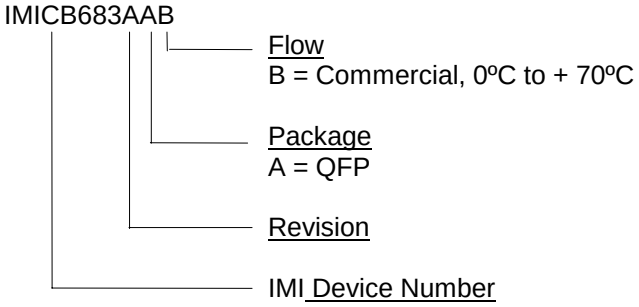
ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
CB683AAB	52 PIN QFP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
CB683AAB
Date Code, Lot #



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