Low EMI Clock Generator with I²C for Mobil Pentium System Boards

Approved Product

PRODUCT FEATURES

- Supports Synchronous PCI Bus Clocking.
- 3 CPU clocks
- 1 AGP clock
- Up to 8 SDRAM clocks for 4 mobile SO DIMMs.
- 7 PCI synchronous clocks.
  - 1 free running
  - 1 early
  - 5 normal
- Optional common or mixed supply mode:
  - VDDC=2.5 or 3.3 Volts

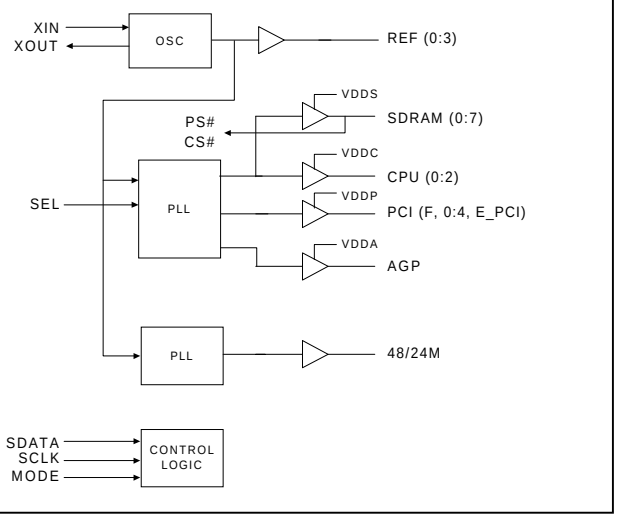
  VDD, VDDA, VDDP and VDDS=3.3 Volts
- < ±250 pS skew among CPU, AGP or SDRAM clocks.
- < ±500 pS skew among PCI clocks.
- I²C 2-Wire serial interface for:
  - SSCG EMI reduction control
  - Enable/disable each output pin
  - Testing and 48/24 MHz clock selection
- Power Management Capability (MODE pin).
- 48/24 MHz for USB support
- Internal Crystal Load Capacitors.
- 48-pin 300 mil. SSOP package
- **Spread Spectrum Technology for EMI reduction**

FREQUENCY SELECTION TABLE

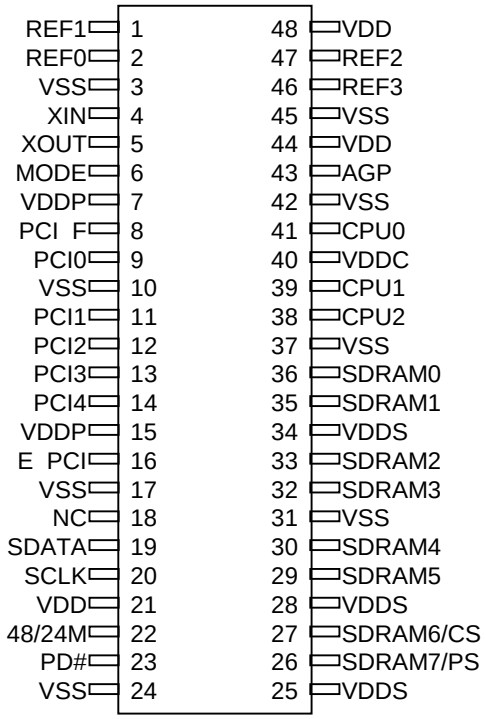
CPU	AGP	PCI
66.6	66.6	33.3

Table 1

BLOCK DIAGRAM



CONNECTION DIAGRAM



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PIN DESCRIPTION

Pin Number	Pin Name	PWR	I/O	TYPE	Description
4	**XIN**	VDD	I	OSI	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.
5	**XOUT**	VDD	O	OSO	If an external input reference is used, Pin 6 is left unconnected.
8	**PCI_F**	VDDP	O	BUF	This is a low skew PCI clock output that **does not** stop when PS# is asserted low.
9, 11, 12, 13, 14	**PCI(0:4)**	VDDP	O	BUF	Low skew (<250 pS) clock outputs for PCI frequencies. Powered by VDDP.
6	**MODE**	VDD	I	-	This pin is for selecting the direction and function of pins 26 and 27. When MODE is set high these bits are SDRAM (6:7) outputs. When MODE is low they become inputs for power management purposes.
16	**E_PCI**	VDDP	O	BUF	This pin is a PCI clock that is phased early with respect to all other PCI clocks. It stops when PS# is brought to a logic low level.
43	**AGP**	VDD	O	BUF	This pin is an AGP clock output. It is the same as the CPU clocks. (See table 1, page 1). 3.3 Volt powered by Pin 44.
41, 39, 38	**CPU(0:2)**	VDDC	O	BUF	Low skew host clock outputs. (See frequency table 1, page 1.)
36, 35, 33, 32, 30, 29	**SDRAM(0:5)**	VDDS	O	BUF	Low skew SDRAM clock outputs. They are powered by VDDS. All 3.3 volts
27	**SDRAM6**	VDDS	O	BUF	This is a bi-directional pin. When 'MODE' is set high, it is SDRAM6 clock output. When 'MODE' is low, this pins become inputs for power management function.
	CS#	VDDS	I	-	If CS# is asserted Low, then CPU (0:3) are stopped in low state.
2,1,47,46	**REF(0:3)**				Buffered copy of the Crystal Oscillator.
26	**SDRAM7**	VDD	I	-	This is a bi-directional pin. When 'MODE' is set high, it is SDRAM7 clock output. When 'MODE' is low, this pins become inputs for power management function.
	PS#	VDD	O	BUF	If PS# is asserted Low, then PCI(0:4,E) are stopped in low state
23	**PD#**	-	I	BUF	Power Down. When this pin is brought low power is removed from all internal circuitry of the device. Has internal pull-up device.
22	**48/24 MHz**	VDD	O	BUF	This is either a 24 or 48 MHz fixed frequency clock. Its frequency selection is performed using the device's I²C registers.
19	**SDATA**	VDD	I/O	-	Serial Data for I²C control interface. This pin receives data streams from the I2C bus and outputs an acknowledge for valid data.
20	**SCLK**	VDD	I	-	Serial Clock for I²C control interface.
3, 10, 17,45, 24, 31, 37, 42	**VSS**	-	PWR		Common ground pins.
48, 44, 21	**VDD**	-	PWR		Power supply for 3.3 volts
7, 15	**VDDP**	-	PWR		3.3V Power supply for PCI pins 8, 9, 11, 12, 13, 14, and 16.
34, 28, 25	**VDDS**	-	PWR		3.3 volt power supply for SDRM pins 26, 27, 29, 30, 32, 33, 35, and 36.
40	**VDDC**	-	PWR		2.5 volt Power supply for CPU pins.

NOTE: all bi-directional pins require either a 10K pull-up or pull down resistor to insure correct sensing by the device during power up.

A bypass capacitor (0.1 uF) should be placed as close as possible to each Vdd pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be canceled by the inductance's of the traces.

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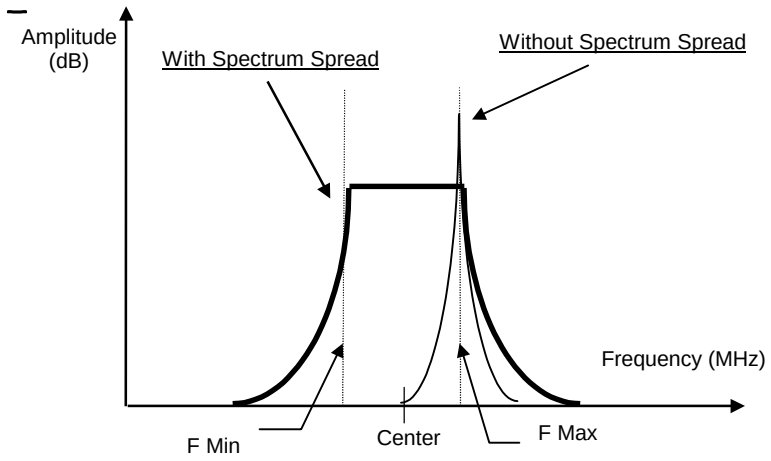
SPECTRUM SPREAD CLOCKING

Down Spread



Spectrum Analysis

SPECTRUM SPREADING SELECTION TABLE

Rest Frequency in MHz desired (actual)	Down Spreading frequencies in MHz			
	F Min.	F Center	F Max.	Spread
66 (66.6)	66.4	66.5	66.6	0.33%

POWER MANAGEMENT FUNCTIONS

When MODE=0, the device supports power management and pins 26, 27 are inputs PS# and CS# respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the I2C serial interface and these pins indicate that it should be enabled. The clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled. See fig. 2 below. When PD# is asserted low, all clocks are stopped in a low state and the crystal and PLL's are shutoff.

POWER MANAGEMENT TIMING

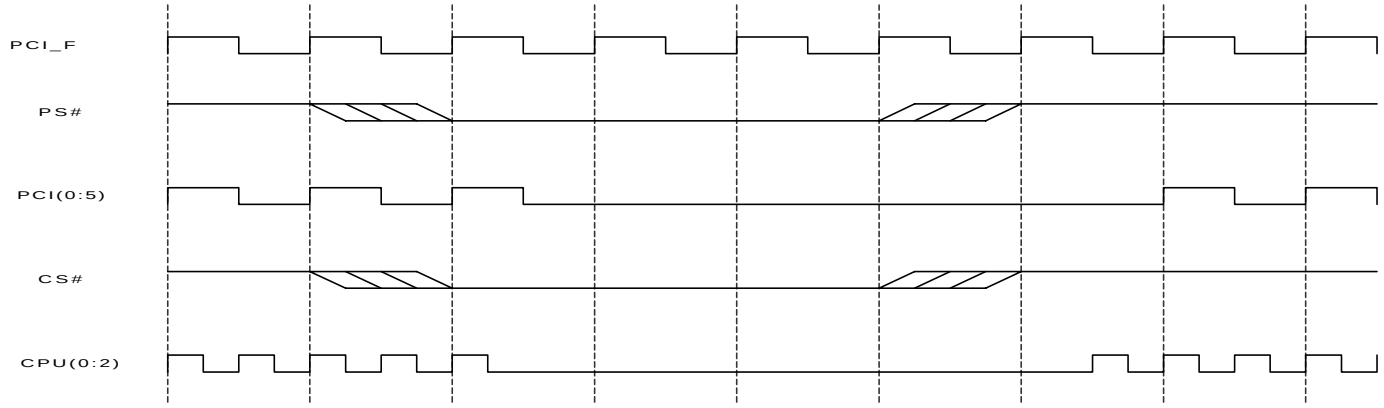


Fig. 2

Please note that all clocks can also be individually (asynchronously) enabled or stopped via the 2-wire I2C control interface. In this case all clocks are stopped in the low state.

2-WIRE I²C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

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The device will respond to writes to 10 bytes (max.) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

I²C SERIAL CONTROL REGISTERS

NOTE: The Pin # column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PD# pin is activated.

Following the acknowledge of the Address Byte (D9), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2...) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register

Bit	@Pup	Pin#	Description
7	x	*	Don't Care
6	x	*	Don't Care
5	x	*	Don't Care
4	x	*	Don't Care
3	1	*	Don't Care
2	1	22	48/24 MHz clock output frequency select 0=24 MHz, 1=48 MHz
1 0	0 0	*	Bit 1 Bit 0 0 0 = Normal Operation (power up default) 0 1 = Test Mode 1 0 = Spread Spectrum Enabled 1 1 = Tri State

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SERIAL CONTROL REGISTERS (Cont.)

TEST MODE FUNCTION TABLE (ENABLED VIA I²C BYTE 0 BIT 0)

Function Description	Outputs						
	CPU	E_PCI, PCIF, PCI	24 MHz	48 MHz	SDRAM	REF	IOAPIC
Tri-state Mode	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state
Test Mode	XIN/2	XIN/4	REF/4	REF/2	XIN/2	XIN	XIN
Normal	CPU (See Table)	PCI (See Table)	24 MHz	48 MHz	CPU (see Table)	14.318	14.318

Byte 1: CPU, SIO, USB Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Don't Care
6	1	22	48/24 MHz enable/Stopped
5	x	-	Don't Care
4	1	43	AGP
3	x	-	Don't Care
2	1	38	CPUCLK2 enable/Stopped
1	1	39	CPUCLK1 enable/Stopped
0	1	41	CPUCLK0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Don't Care
6	1	8	PCI_F enable/Stopped
5	1	16	E_PCI enable/Stopped
4	1	14	PCI4 enable/Stopped
3	1	13	PCI3 enable/Stopped
2	1	12	PCI2 enable/Stopped
1	1	11	PCI1 enable/Stopped
0	1	9	PCI0 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	SDRAM7 enable/Stopped
6	1	27	SDRAM6 enable/Stopped
5	1	29	SDRAM5 enable/Stopped
4	1	30	SDRAM4 enable/Stopped
3	1	32	SDRAM3 enable/Stopped
2	1	33	SDRAM2 enable/Stopped
1	1	35	SDRAM1 enable/Stopped
0	1	36	SDRAM0 enable/Stopped

SERIAL CONTROL REGISTERS (Cont.)

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Don't Care
6	x	-	Don't Care
5	x	-	Don't Care
4	x	-	Don't Care
3	x	-	Don't Care
2	x	-	Don't Care
1	x	-	Don't Care
0	x	-	Don't Care

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Don't Care
6	x	-	Don't Care
5	x	-	Don't Care
4	x	-	Don't Care
3	1	46	REF3 enable/Stopped
2	1	47	REF2 enable/Stopped
1	1	1	REF1 enable/Stopped
0	1	2	REF0 enable/Stopped

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Ambient Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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ELECTRICAL CHARACTERISTICS						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	260	mA	CPU = 66.6 MHz, PCI = 33.3 MHz at 3.5V
Static Supply Current	Isdd	-	-	150	µA	-
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds
VDD = VDDP = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU/AGP to PCI Offset	tOFF	-	±250	±500	pS	Load: CPU = 20 pF measured @1.25V SDRAM = 30 pF measured @1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM), (AGP-CPU)	tSKEW1	-	-	±250	pS	Load: CPU = 20 pF measured @1.25V PCI = 30 pF measured @1.5V AGP = 20 pF measured @1.5V SDRAM = 30 pF measured @1.5V
Skew E_PCI-PCI(F, 0:4)	tSKEW2	1.5	2.0	2.5	nS	Load: E_PCI = 30 pF measured @1.5V PCI = 30 pF measured @1.5V (E_PCI Leads PCI)
Skew (CPU-SDRAM)	tSKEW3	500	-	1000	pS	Load: CPU = 20 pF measured @1.25V SDRAM = 30 pF measured @1.5V SDRAM leads
JITTER PERFORMANCE						
Jitter, Adjacent Cycles	TJ_{CC1}	-	-	±250	pS	CPU, AGP and SDRAM clocks
Jitter, Adjacent Cycles	TJ_{CC2}	-	-	±500	pS	PCI, 14 MHz and 48 MHz clocks
VDD = VDDA = VDDP = VDDS = 3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

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BUFFER CHARACTERISTICS FOR CPU (0:3), AGP						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Pull-up Current Min.	IOH_{min}	22	-	-	mA	Vout = VDD -.5V
Pull-up Current Max.	IOH_{max}	-	-	-37	mA	Vout = 1.25V
Pull-Down Current Min.	IOL_{min}	30	-	-	mA	Vout = .4V
Pull-Down Current Max.	IOL_{max}	-	-	75	mA	Vout = 1.2V
Rise/Fall Time @ (0.4 V - 2.0 V)	TRF	0.4	-	1.6	nS	Load = 20 pF
VDD = VDDP = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

BUFFER CHARACTERISTICS FOR SDRAM(0:7)						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Pull-up Current Min.	IOH_{min}	30	-	-	mA	Vout = VDD - .5V
Pull-up Current Max.	IOH_{max}	-	-	-75	mA	Vout = 1.5V
Pull-Down Current Min.	IOL_{min}	30	-	-	mA	Vout = .4V
Pull-Down Current Max.	IOL_{max}	-	-	75	mA	Vout = 1.2V
Rise/Fall Time @ (0.4 V - 2.4 V)	TRF	0.5	-	1.3	nS	Load = 30 pF
VDD = VDDP = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

BUFFER CHARACTERISTICS FOR PCI(0:4,F,E_PCI)						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Pull-up Current Min.	IOH_{min}	-9	-	-	mA	Vout = VDD - .5V
Pull-up Current Max.	IOH_{max}	-	-	-32	mA	Vout = 1.5V
Pull-Down Current Min.	IOL_{min}	10	-	-	mA	Vout = .4V
Pull-Down Current Max.	IOL_{max}	-	-	25	mA	Vout = 1.5V
Rise/Fall Time @ (0.4 V - 2.4 V)	TRF	0.5	-	2.0	nS	Load = 30 pF
VDD = VDDP = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, TA = 0ºC to +70ºC						

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TB5L1 TYPE BUFFER CHARACTERISTICS FOR 24M/48M and REF (0:3)						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Pull-up Current Min.	IOH_{min}	-13	-	-	mA	Vout = VDD -.5V
Pull-up Current Max.	IOH_{max}	-	-	-30	mA	Vout = 1.5V
Pull-Down Current Min.	IOL_{min}	13	-	-	mA	Vout = .4V
Pull-Down Current Max.	IOL_{max}	-	-	32	mA	Vout = 1.5V
Rise/Fall Time @ (0.4 V - 2.4 V)	TRF	-	-	2.0	nS	20 pF Load
VDD = VDDP = VDDS =3.3V ±5%, VDDC = 2.5 ± 5%, VDDA + 2.5 or 3.3V + 5% TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3 Vdd	Vdd/2	0.7 Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	The crystals rated load. note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore = 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore = 18.0 pF

The total parasitic capacitance would therefore be = 20.0 pF.

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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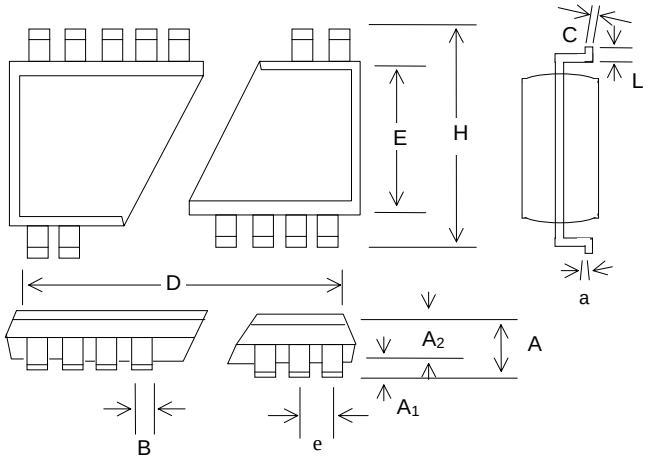
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMIC4814EYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
C4814EYB
Date Code, Lot #

IMIC4814EYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number

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