IMI145151 FREQUENCY SYNTHESIZER

CMOS LSI

PARALLEL PROGRAMMED PLL FREQUENCY SYNTHESIZER

PRODUCT DESCRIPTION

The IMI145151 is a member of a family of phaselock loop synthesizer ICs from International Microcircuits. The IMI145151 is an improved version of the Motorola MC145151 and will provide a synthesizer with noticeably improved performance.

The IMI145151 is programmed with parallel input data lines. Since it does not require a microcontroller as serial and bus programmed units do, the IMI145151 is an excellent choice for synthesizers requiring independence from digital controllers. Such applications include fixed local oscillator signals, whose tuning never changes, and signal sources, which have few operating frequencies.

Blocks in the IMI145151 include a programmable feedback divider, a reference divider, phase detector, and charge pump. The reference divider is programmed by three select lines to one of eight ROM encoded values. Both counter inputs are biased for maximum sensitivity to sinewave input signals. The reference divider input is also configured to operate as a crystal oscillator if desired.

The IMI145151 has a Type IV phase frequency detector which has eliminated by the design the inherent dead zone which causes crossover distortion at the critical center lock point. the IMI circuit enables consistent low noise loop designs using the simple single ended charge pump output. Differential charge pump outputs are also provided for those who require a more sophisticated differential active loop filter design.

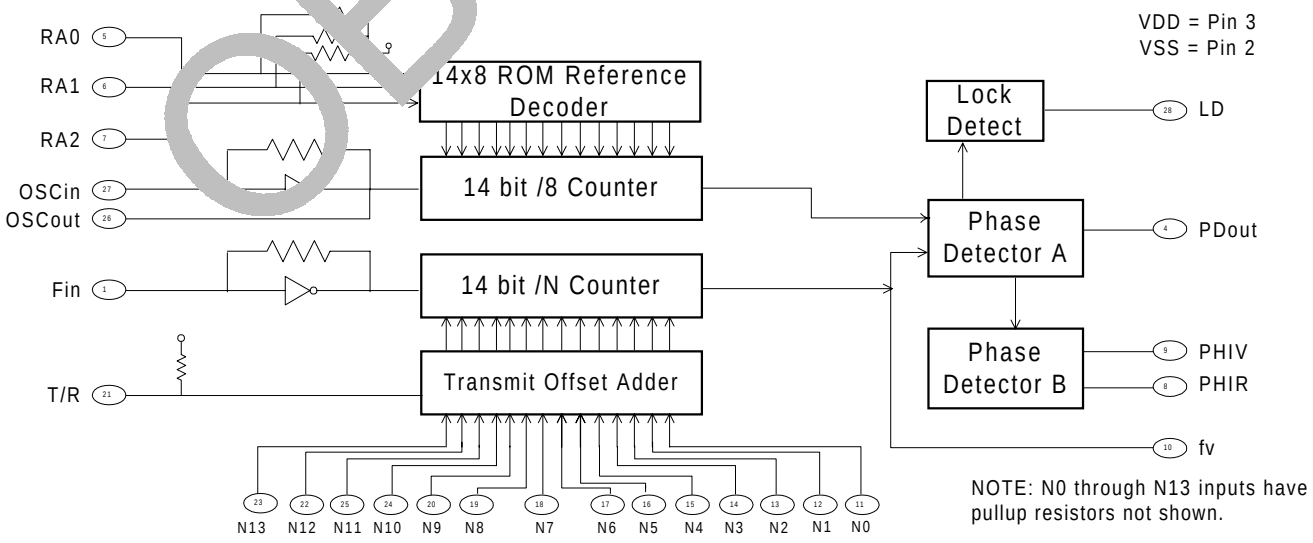
Performance improvements are in the operating bandwidth and phase detector noise floor. With its extremely low phase noise floor and wider input bandwith, prescaler ratios can be minimized allowing wide loop bandwidths for faster settling and lower phase noise.

PRODUCT FEATURES

- >200 Mhz typical input frequency.
- -163 dBc/Hz total phase noise floor.
- No dead zone by design.
- Unambiguous PLL acquisition.
- User-selectable reference divider ratios: 8, 128, 256, 512, 1024, 1048, 2410, 8192.
- Lock detect signal.
- 14 bit N counter. Divider range = 3 to 16383.

  On- or off-chip reference oscillator operation.
- 3-volt and 5-volt characterizations.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	*Name*	*Description*
1	Fin	RF input signal. Applied to both the N and A counters. This signal is intended to be AC coupled for low level sinewave input signals. For CMOS logic level input signals, DC coupling can be used.
2	Vss	Circuit ground.
3	Vdd	Circuit-positive power supply.
4	Pdout	Single-ended charge pump output, usually used with passive loop filters. This signal operates according to the following: ■ Frequency fv>fr at the phase detector: negative pulses. ■ Frequency fv<fr at the phase detector: positive pulses. ■ Frequency fv = fr at the phase detector: high-impedance state.
5	RA0	The three reference divisor ratio select pins. Pull-up resistors are included on each of
6	RA1	these pins to insure that, if left unconnected, they will remain at a logic ONE.
7	RA2	The reference divider ratio is set according to the following table:
8	PHIR	Phase detector output. This signal goes LOW when the feedback frequency is too low.
9	PHIV	Phase detector output. This signal goes LOW when the feedback frequency is too high.
10	fv	Output of the feedback divider.
11	N0	LSB of the N counter programming input bits. Pull-up resistor included.
12	N1	LSB+1 of the N counter programming input bits. Pull-up resitor included.
13	N2	LSB+2 of the N counter programming input bits. Pull-up resitor included.
14	N3	LSB+3 of the N counter programming input bits. Pull-up resitor included.
15	N4	LSB+4 of the N counter programming input bits. Pull-up resitor included.
16	N5	LSB+5 of the N counter programming input bits. Pull-up resitor included.
17	N6	LSB+6 of the N counter programming input bits. Pull-up resitor included.
18	N7	LSB+7 of the N counter programming input bits. Pull-up resitor included.
19	N8	LSB+8 of the N counter programming input bits. Pull-up resitor included.
20	N9	LSB+9 of the N counter programming input bits. Pull-up resitor included.
21	T/R	This input control an offset that can be added to the programming inputs. Thisoffset is fixed at 856 when T/R is low. When T/R is high, there is no offset added. A pull-up resistor is included.
22	N12	LSB+12 of the N counter programming input bits. Pull-up resitor included.
23	N13	LSB+13 of the N counter programming input bits. Pull-up resitor included.
24	N10	LSB+10 of the N counter programming input bits. Pull-up resitor included.
25	N11	LSB+11 of the N counter programming input bits. Pull-up resitor included.
26	OSCout	Reference signal output or output of the oscillator inverter.
27	OSCin	AC-coupled reference signal input or input to the oscillator inverter.
28	LD	Lock detect output. When the PLL is locked, this signal will be essentially HIGH, with very narrow negative spikes at the phase detection frequency. If the PLL is out of lock, this signal will pusle LOW.

RA2	RA1	RA0	Reference Divider Ratio
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65°C to 150°C
Ambient Temperature:	-55°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precaustions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$Vss<(Vin \text{ or } Vout)<V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either Vss or V_{DD}).

PLL OPERATING CHARACTERISTICS

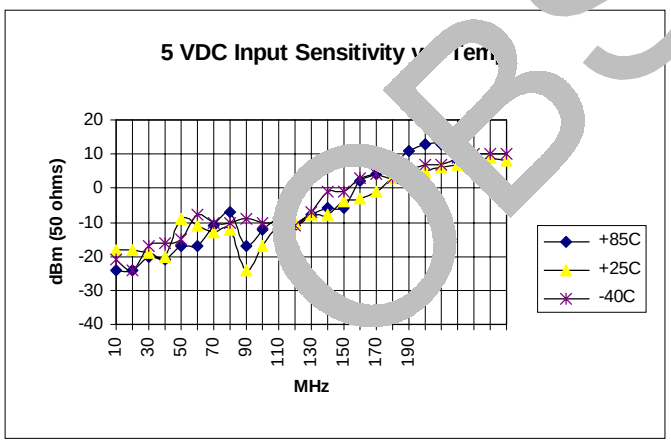
VDD = 5 VOLTS

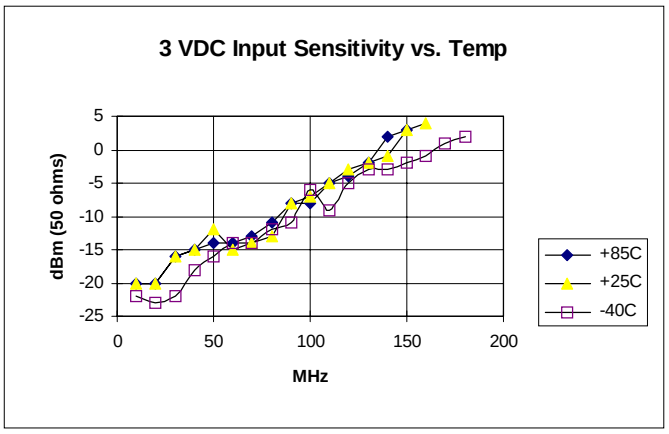
Characteristic		Symbol		-40°C		0°C		25°C			70°C		85°C		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
Dynamic	Operating Frequency	Fin	Sin	210	-	200	-	200	250	-	180	-	180	-	MHz	
			Square	210	-	200	-	200	250	-	180	-	180	-	MHz	
		Fosc													MHz	
	Synthesizer Phase Noise Floor	PDNF							-160						dBc/ Hz	
	Pin Capacitance	Cin		-				-	6	10			-	10	pF	
		Cout			10			-	6	10			-	10	pF	
Static	Input Voltages	VIL		1	1.5		1.5	-	2.75	1.5	-	1.5	-	1.5	Vdc	
		VIH		3.5		3.5	-	3.5	2.75	-	3.5	-	3.5	-	Vdc	
	Output Voltages	VOL			0.4	-	0.05	-	0.0	0.05	-	.05	-	0.05	Vdc	
		VOH		4.95	-	4.95	-	4.95	5.0	-	4.95	-	4.95	-	Vdc	
	Output Current	IOL	Logic	2.4				2.0	2.8	-			1.6	-	mA	VOL = 0.40
			OSCout		-			1.0	1.4	-			0.8	-		
		IOH	Logic	-2.4	-			-2.0	-2.8	-			-1.6	-	mA	VOH = 4.0
			OSCout	-1.2	-			-1.0	-1.4	-			-0.8	-	mA	VOH = 4.0
	Charge Pump Current								12.4						mA	Vdd = 5.0V
	Supply Currents	IDD													mA	Fosc=Fin= 10 MHz
		ISB		-	150			-	40	150			-	150	uA	Fosc=Fin=0
		IPU							50						uA	VIL = 0

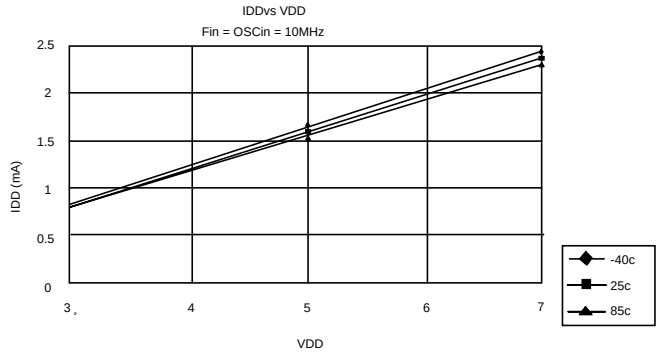
PLL OPERATING CHARACTERISTICS

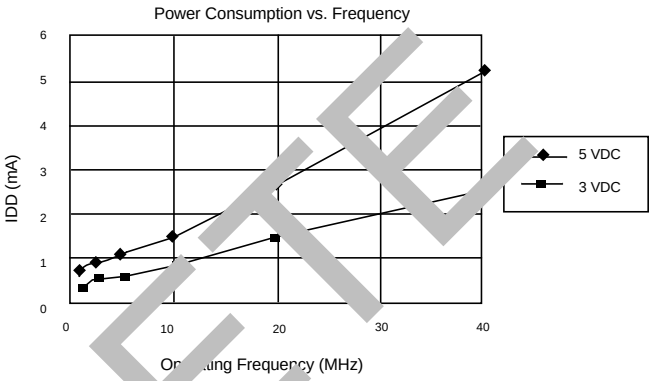
VDD = 3 VOLTS

Characteristic		Symbol		-40°C		0°C		25°C			70°C		85°C		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
Dynamic	Operating Frequency	Fin	Sin	160	-	140	-	130	150	-	120	-	110	-	MHz	
			Square	160	-	140	-	130	150	-	120	-	110	-	MHz	
		Fosc													Hz	
	Synthesizer Phase Noise Floor	PDNF							-155						dBc/ Hz	
	Pin Capacitance	Cin		-	10			-	6	10			-	10	pF	
		Cout		-	10			-	6	10			-	10	pF	
Static	Input Voltages	VIL		-	0.9			-	1.35	0.9			-	0.9	Vdc	
		VIH		2.1	-			2.1	1.65	-			2.1	-	Vdc	
	Output Voltages	VOL		-	0.05	-	0.05	-	0.0	0.05		.05	-	0.05	Vdc	
		VOH		2.95	-	2.95	-	2.95	3.0	-	2.95		2.95	-	Vdc	
	Output Current	IOL	Logic	1.6	-			1.4		-			0.8	-		VOL = 0.30
			OSCout	0.8	-			0.7	1.	-			0.4	-	mA	
		IOH	Logic	-1.6	-				-1.0	-			-0.8	-	mA	VOH = 2.4
			OSCout	-0.8	-			-0.7	0				-0.4	-	mA	VOH = 2.4
	Charge Pump Current														mA	Vdd = 3.0V
	Supply Currents	IDD													mA	Fosc=Fin= 10 MHz
		ISB		-	150			-	4	150			-	150	uA	Fosc=Fin=0
		IPU							0						uA	VIL = 0





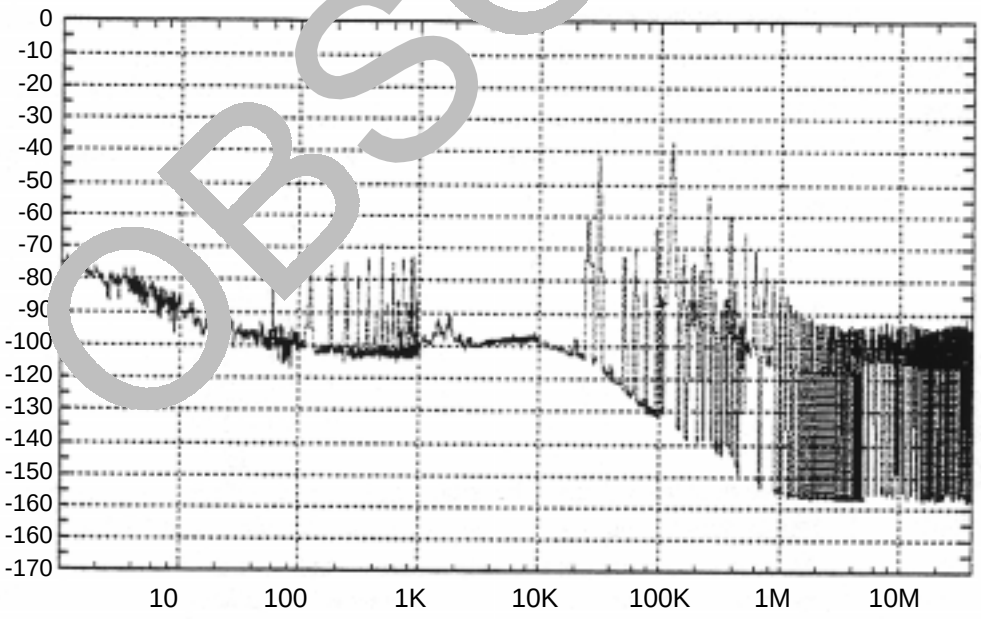




PHASE NOISE FLOOR

152/HP 10811A Ref vs 5362 Loop/Residual Noise @ 145 MHZ

(hp) 3018R Carrier: 145.E 6 Hz 8 Nov 1994 13:07:47 - 13:16:37

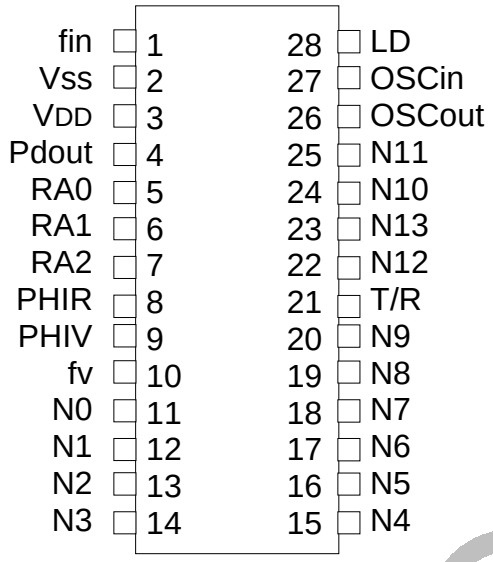


Fosc = 1 Mhz
Fref = 125 Khz
fin = 145 Mhz
N = 1160

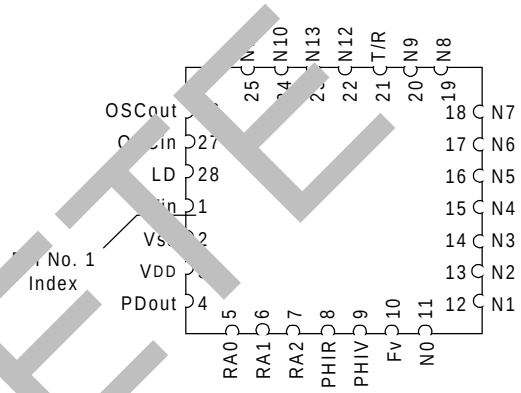
Measured floor @ 500 Hz = -102 dBc/Hz
-20 log (N) = - 61 dB
- 163 dBc/Hz

CONNECTION DIAGRAMS

SSOP, SOIC AND PDIP PACKAGES



PLCC PACKAGE



ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMI145151xPB	Plastic Dip	Commercial, 0°C to +70°C
IMI145151xXB	SOIC	Commercial, 0°C to +70°C
IMI145151xYB	SSOP	Commercial, 0°C to +70°C
IMI145151xQB	PLCC	Commercial, 0°C to +70°C

*Please contact factory for other options.

NOTE: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combinationof device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
145151xPB
Date Code, Lot #

IMI145151xPB

Flow

B = Commercial, 0° to + 70C

Package

P = Plastic Dip
X = Small Outline
Y = SSOP
Q = PLCC

Revision

IMI Device Number