PI49FCT3805
PI49FCT3806

3.3V, 2 x 1:5 CMOS Clock Driver

Features

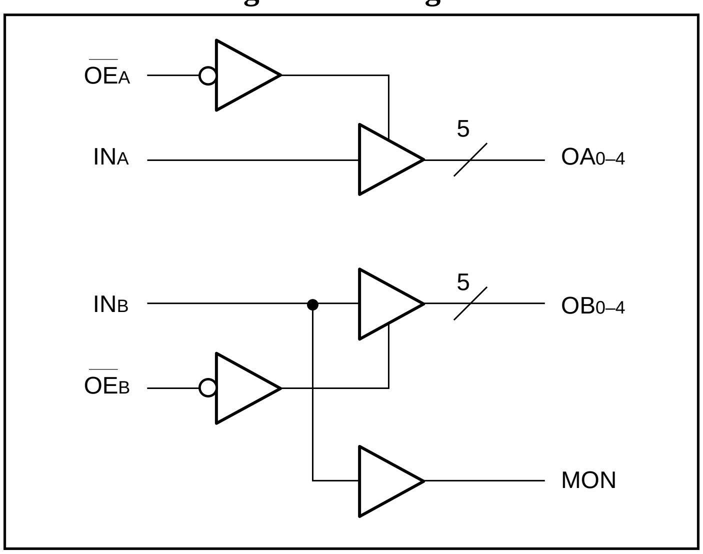
- Low output skew: <300ps
- Switching frequency of 100 MHz
- Fast output rise/fall time <1.2ns
- Low propagation delay <3.0ns
- Low input capacitance <4.0pF
- Internal 20 Ohm resistor version
- 5V I/O Tolerant input
- Rail-to-Rail CMOS outputs
- Industrial Temperature: –40°C to +85°C
- 3.3V ±10% operation
- Packages available:
  - –20-pin 300-mil wide SOIC (S)
  - –20-pin 150-mil wide QSOP (Q)
  - –20-pin 209-mil wide SSOP (H)

Description

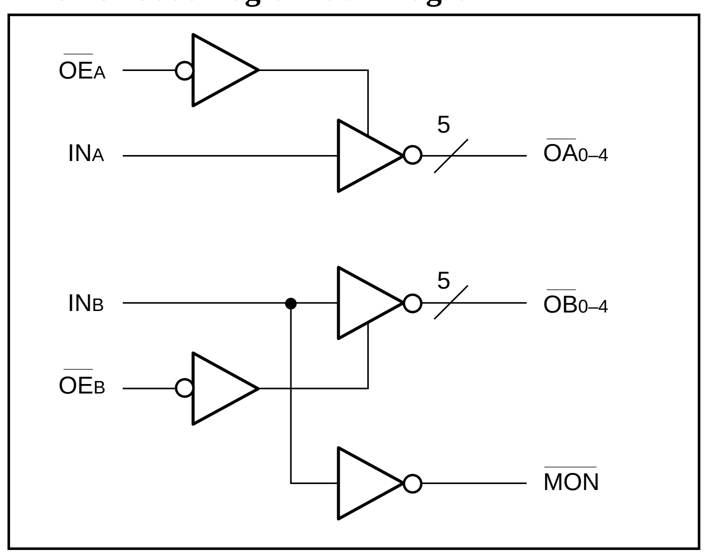
Pericom Semiconductor's PI49FCT series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology to achieve fast speed, low skew, fast slew rate, and low propagation delay for most computing and communication applications.

The PI49FCT3805 is a non-inverting driver, whereas the PI49FCT3806 is an inverting driver. The outputs are configured into 2 groups of 1-in, 5-out with independent output enable. Group B has an extra MON output. Excellent output signals to power and ground ratio minimize power and ground noise, and also improves output performance.

PI49FCT3805 Logic Block Diagram



PI49FCT3806 Logic Block Diagram



Product Pin Description

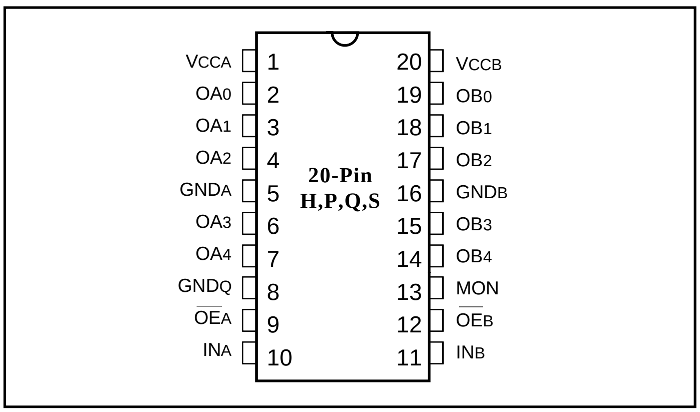
Pin Name	Description
$\overline{OE}_A$, $\overline{OE}_B$	Hi-Z State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs
MON	Monitor Output
GND	Ground
V_{CC}	Power

PI49FCT3805 Truth Table(1)

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_N, OB_N	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Note:
1. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance

PI49FCT3805 Product Pin Configuration

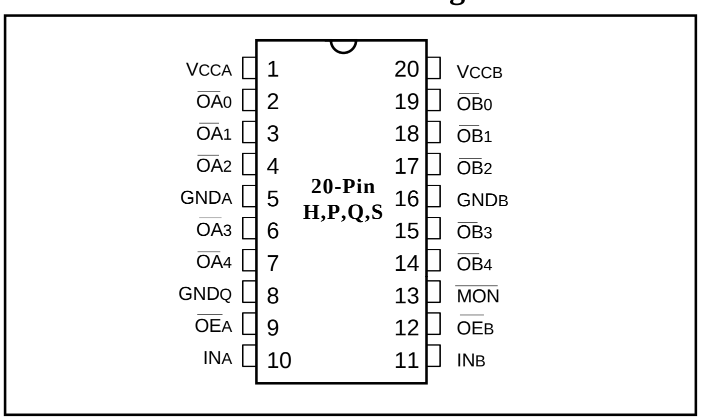


PI49FCT3806 Truth Table(1)

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	$\overline{OA}_N$, $\overline{OB}_N$	$\overline{MON}$
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

Note:
1. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance

PI49FCT3806 Product Pin Configuration



Capacitance (T_A = 25°C, f = 1 MHz)

Parameters(1)	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Note:
1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Ambient Temperature = –40°C to +85°C
Vcc = 3.3V ± 0.3V

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 0.1mA I_{OH} = – 8mA	V_{CC}–0.2 2.4[3]	— 3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA I_{OL} = 16mA I_{OL} = 24mA	— — —	— 0.2 0.3	0.2 0.4 0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level (Input Pins)		2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level (Input Pins)		–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC} (Input Pins)	—	—	1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND (Input & Output Pins)	—	—	–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = V_{CC}	—	—	1	µA
I_{OZL}	Output Current	(3-State Output pins)	V_{OUT} = GND	—	—	–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		–35	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		50	90	200	mA
I_{OS}	Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND[5]		–60	–135	–240	mA
V_H	Input Hysteresis			—	150	—	mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. V_{OH} = V_{CC} – 0.6V at rated current.
4. This parameter is determined by device characterization but is not production tested.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	3	30	µA
ΔI_{CC}	Supply Current per Inputs @ TTL HIGH	V_{CC} = Max.	$V_{IN} = V_{CC} - 0.6V$[3]	—	2.0	300	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.08	0.16	mA/ MHz
I_C		V_{CC} = Max., Outputs Open f_O = 10 MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Mon. Outputs Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	—	3.3	9.0[5]	mA
			$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	3.3	10.0[5]	
		V_{CC} = Max., Outputs Open f_O = 2.5 MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Eleven Outputs Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	—	1.8	6.0[5]	
			$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	1.8	7.0[5]	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$

   I_{CC} = Quiescent Current

   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

   f_O = Output Frequency

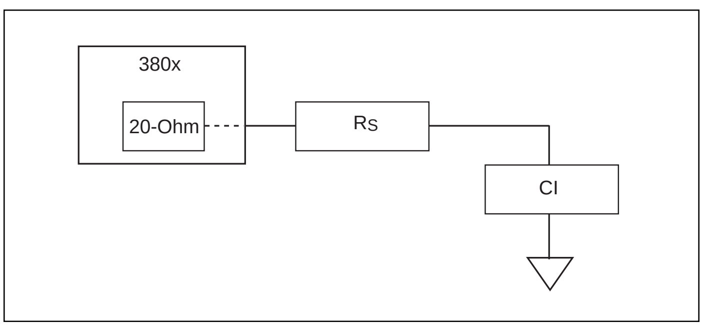
   N_O = Number of Outputs at f_O

   All currents are in milliamps and all frequencies are in megahertz.

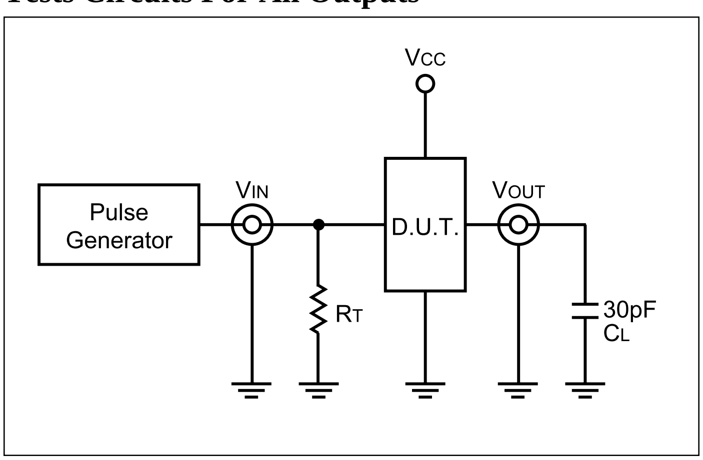
Switching Characteristics over Operating Range

Symbol	Description	Condition	3280x Max.	380xD Max.	380xC Max.	380xB Max.	380xA Max.	380x Max.	Units
t_{PLH} t_{PHL}	Propagation Delay A to Bn(4)	10pF(1) 30pF, <100MHz 50pF, <67MHz	3.0 3.5 4.0	3.0 3.5 4.0	3.5	3.8	4.0	4.5	ns
t_R/t_F	Rise/Fall Time(3)	0.8V –2.0V	1.2	1.2	1.5	1.5	1.5	1.5	
$t_{SK(o)}$	Output Skew (same Pkg.)(3)	10pF(1) 30pF, <100MHz 50pF, <67MHz	0.15 0.30 0.50	0.15 0.30 0.50	0.35	0.35	0.50	0.50	
$t_{SK(t)}$	Output Skew (different Pkg.)(3)	10pF(1) 30pF, <100MHz 50pF, <67MHz	0.30 0.50 0.70	0.30 0.50 0.70	0.75	0.75	1.00	1.00	
F_{IN}	Input Frequency		125	150	110	100	80	67	MHz

Notes:
1. 50-Ohm AC terminated or 50-Ohm to $V_{CC}/2$.
2. Other loading condition is shown in Figure........
3. These parameters are guaranteed by design.
4. Minimum propagation delay of 1.5ns is guaranteed by design.



Tests Circuits For All Outputs(1)



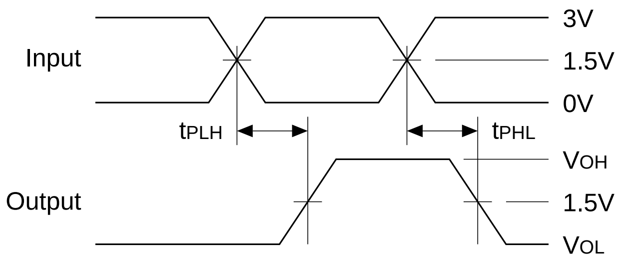
Switch Position

Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

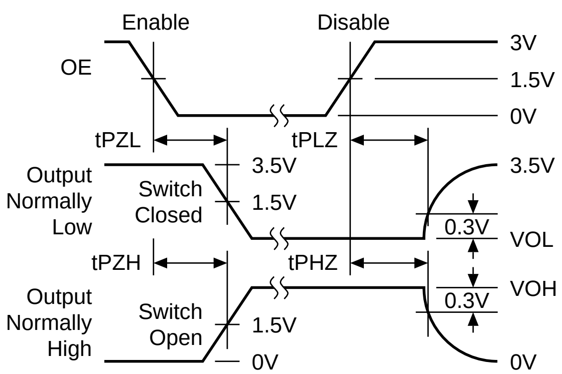
DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SWITCHING WAVEFORMS

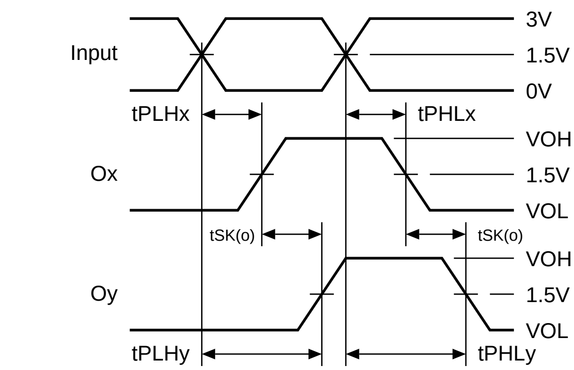
Propagation Delay



Enable and Disable Times

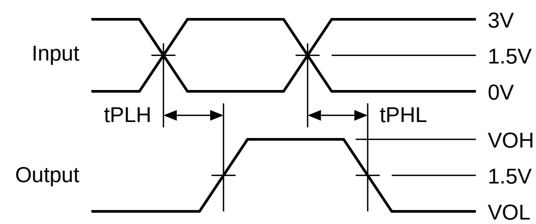


Output Skew – tSK(o)



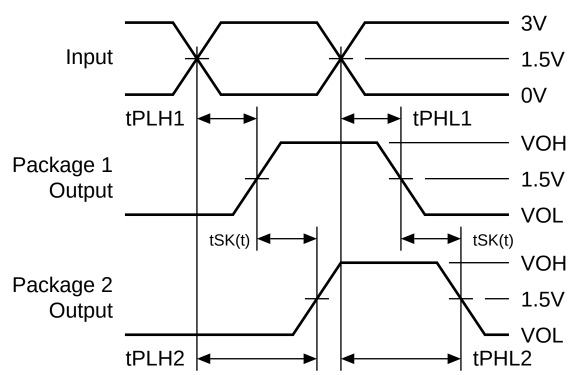
tSK(o) = | tPLHy – tPLHx | or | tPHLy – tPHLx |

Pulse Skew – tSK(p)



tSK(p) = | tPHL – tPLH |

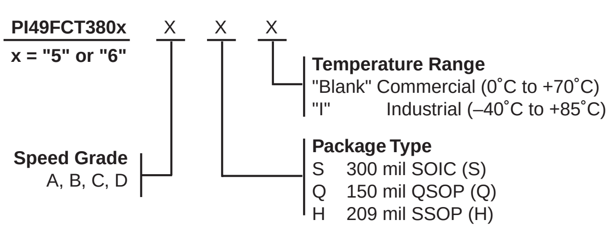
Package Skew – tSK(t)



tSK(t) = | tPLH2 – tPLH1 | or | tPHL2 – tPHL1 |

Ordering Information

Part Number	Package Type
PI49FCT3805-S20	20-pin 300 mil wide SOIC
PI49FCT3805-Q20	20-pin 150 mil wide QSOP
PI49FCT3805-H20	20-pin 209 mil wide SSOP
PI49FCT3806-S20	20-pin 300 mil wide SOIC
PI49FCT3806-Q20	20-pin 150 mil wide QSOP
PI49FCT3806-H20	20-pin 209 mil wide SSOP



Market Information