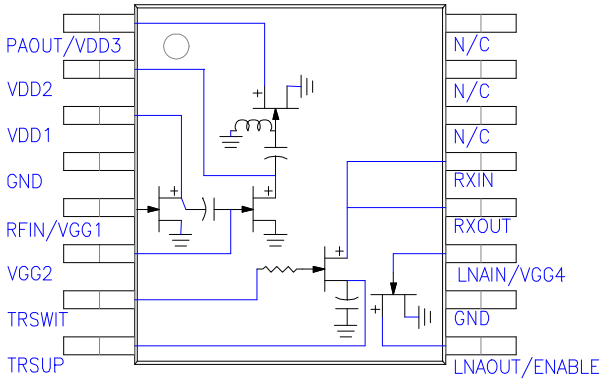
2.4V Integrated DECT Front-End
ITT1201GF

PRELIMINARY

FEATURES

- 2.4V Operation
- Single Positive Supply
- 50% Power Added Efficiency
- 100% Duty Cycle
- 1.6 dB LNA Noise Figure
- 16 Pin TSSOP Full Downset Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process



Note: Full Downset Paddle Soldered to Board Ground

Description

The ITT1201GF is an integrated DECT front-end based on GaAsTEK's GaAs Self-Aligned MSAG® MESFET Process. This product has an integrated power amplifier, low noise amplifier, and switch in one surface mount package.

Maximum Ratings (T_S = 31 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	4	Vdc
RF Input Power, RF_{IN}	P_{IN}	3	mW
RF Input Power, LNA_{IN}	P_{IN}	1	mW
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD}= 2.4V, TR_{SUP}=2.4V, T_s =31 °C (Note 1), Output externally matched to 50 Ω

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	1880	—	1930	MHz
Transmit Path (PA + T/R Switch) $V_{DD1,2,3}$=2.4V, P_{IN}= -2 dBm, TR_{SWIT}=2.4V, LNA_{ENABLE}=0.0V, f=1900 MHz					
Load Power (at Ant)	P_{OUT}		25		dBm
Current Consumption	$I_{DD1,2,3}$		344		mA
Input VSWR				2:1	
Harmonics	—		-39		dBc
Duty Cycle	—			100	%
Forward Isolation (RF_{IN} to Ant) Power Amplifier inactive	—		52		dB
Receive Path (T/R Switch + LNA) $V_{DD1,2,3}$=0.0V, LNA_{ENABLE}=2.4V, TR_{SWIT}=0.0V, f=1900 MHz					
Current Consumption	LNA_{ENABLE}		4.5		mA
Noise Figure (Ant to LNA_{OUT})	NF		2.3		dB
Gain (Ant to LNA_{OUT})	G		15.3		dB
Third-Order Input Intercept Point	IIP_3		3.5		dBm
Switch:					
Reverse Isolation (LNA_{OUT} to ANT) LNA active	—		18		dB
Forward Isolation (RF_{IN} to LNA_{OUT}) LNA inactive	—		35		dB

Note 1: T_S is the temperature measured at the soldering point of the downset paddle on the bottom of the IC, mounted on 10 mil FR4 evaluation board in a free air condition with ambient room temperature T_A=25 °C. The electrical data presented herein was taken with the evaluation board shown in Figure 7, under room temperature conditions and CW operation, unless otherwise specified.

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TYPICAL CHARACTERISTICS

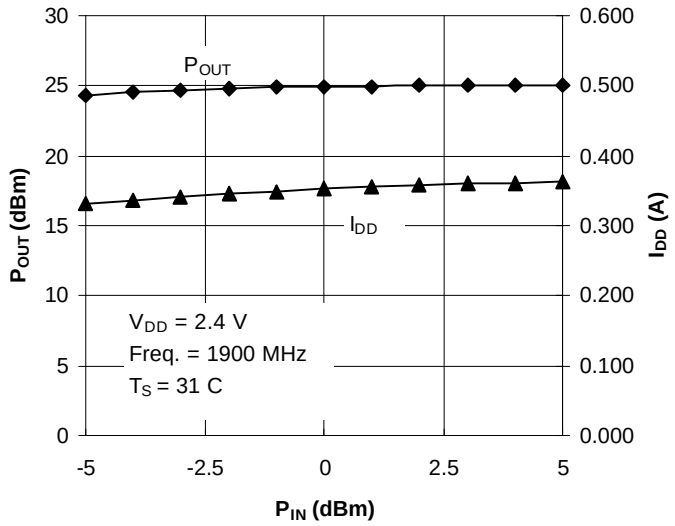

Figure 1. Output power and drain current vs. input power

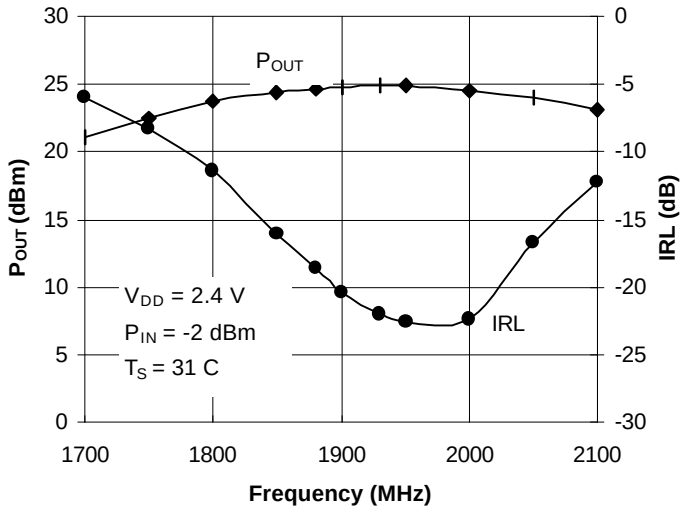

Figure 2. Output power and input return loss vs. frequency.

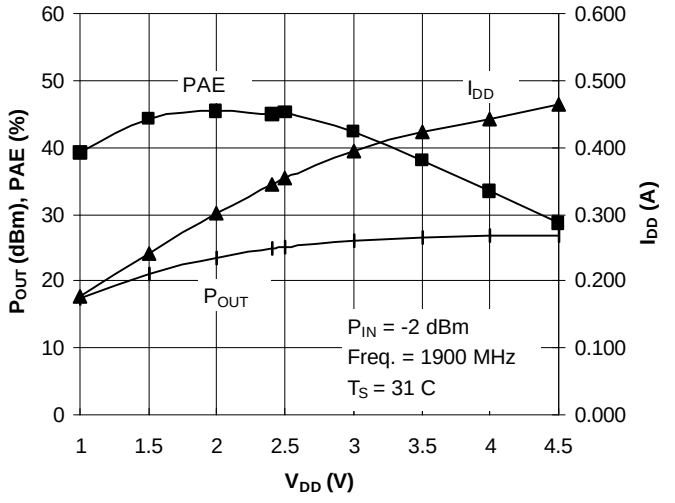

Figure 3. Output power, drain current and efficiency vs. supply voltage

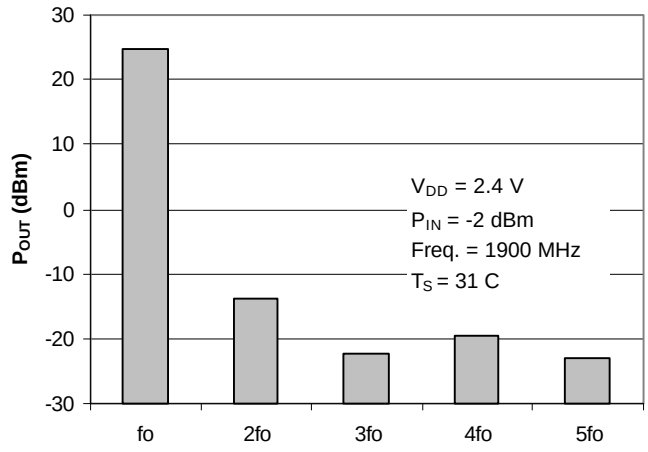

Figure 4. Harmonics

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TYPICAL CHARACTERISTICS (CONT)

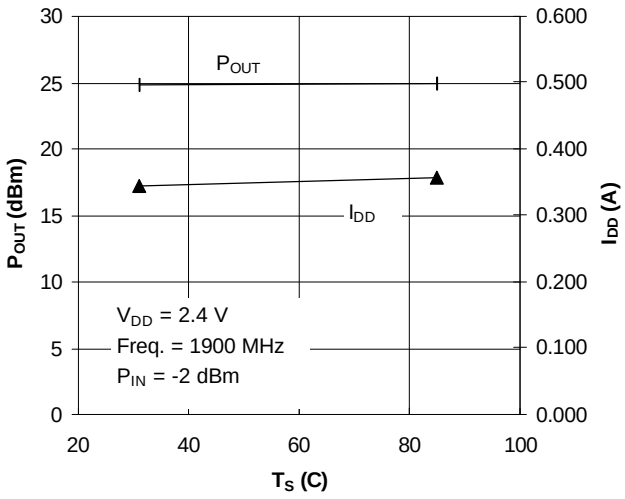

Figure 5. Output power and drain current vs. temperature

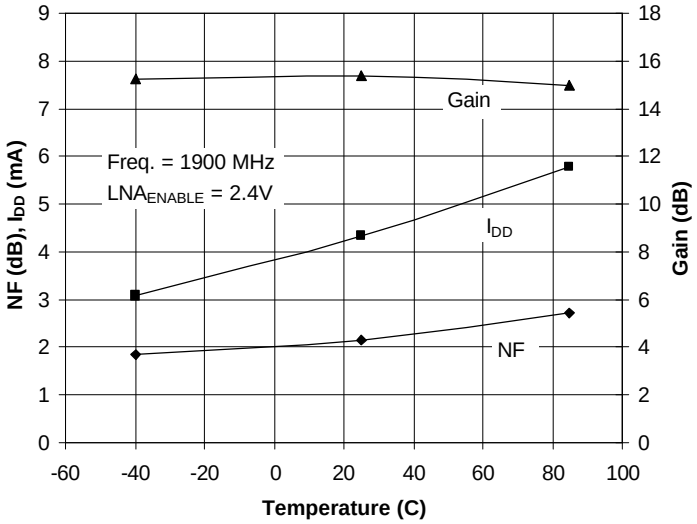

Figure 6. Noise figure, gain and drain current vs. temperature

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APPLICATION INFORMATION

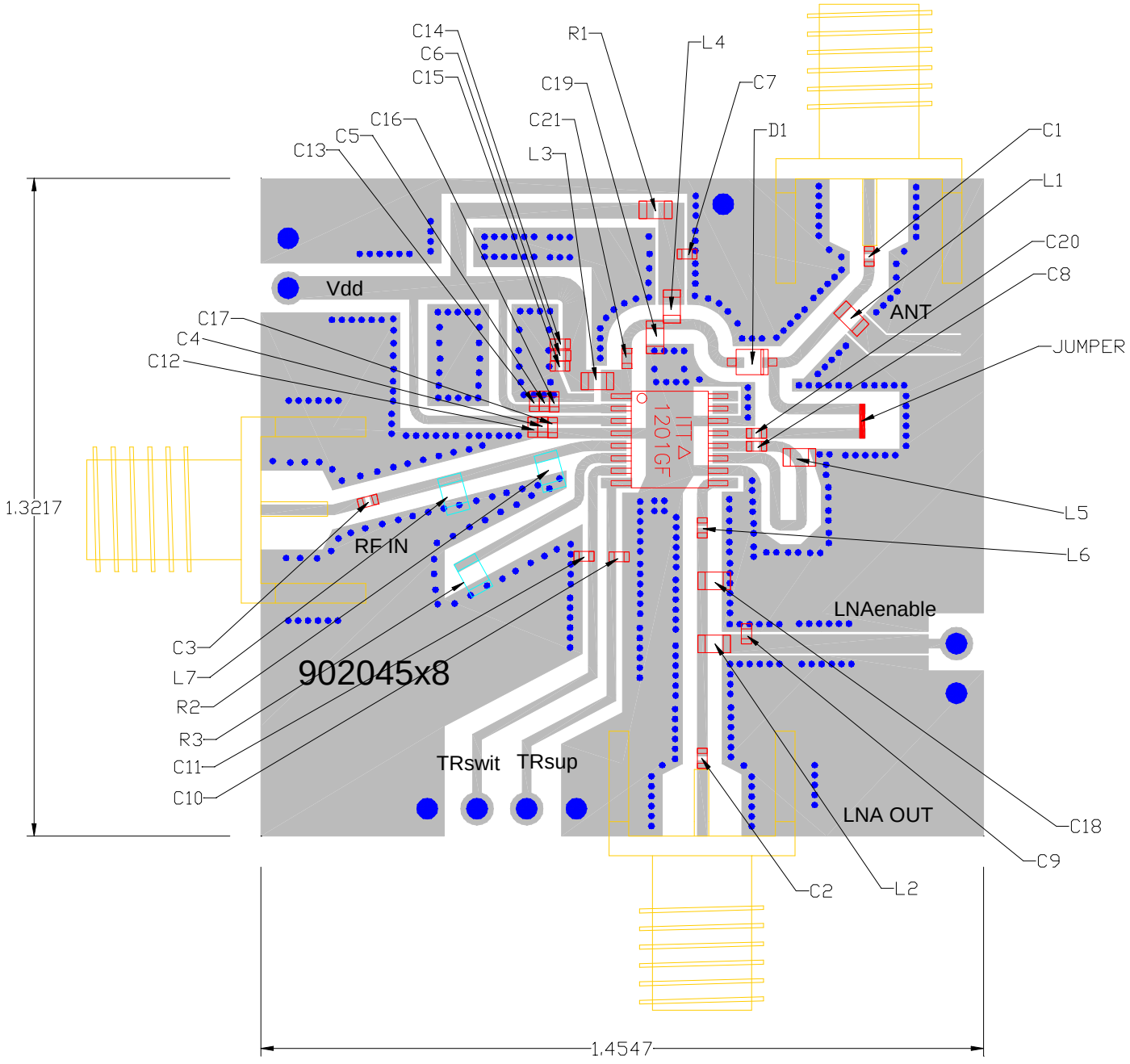

Figure 7. Component layout and printed circuit drawing for evaluation board.

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APPLICATION INFORMATION (CONT)

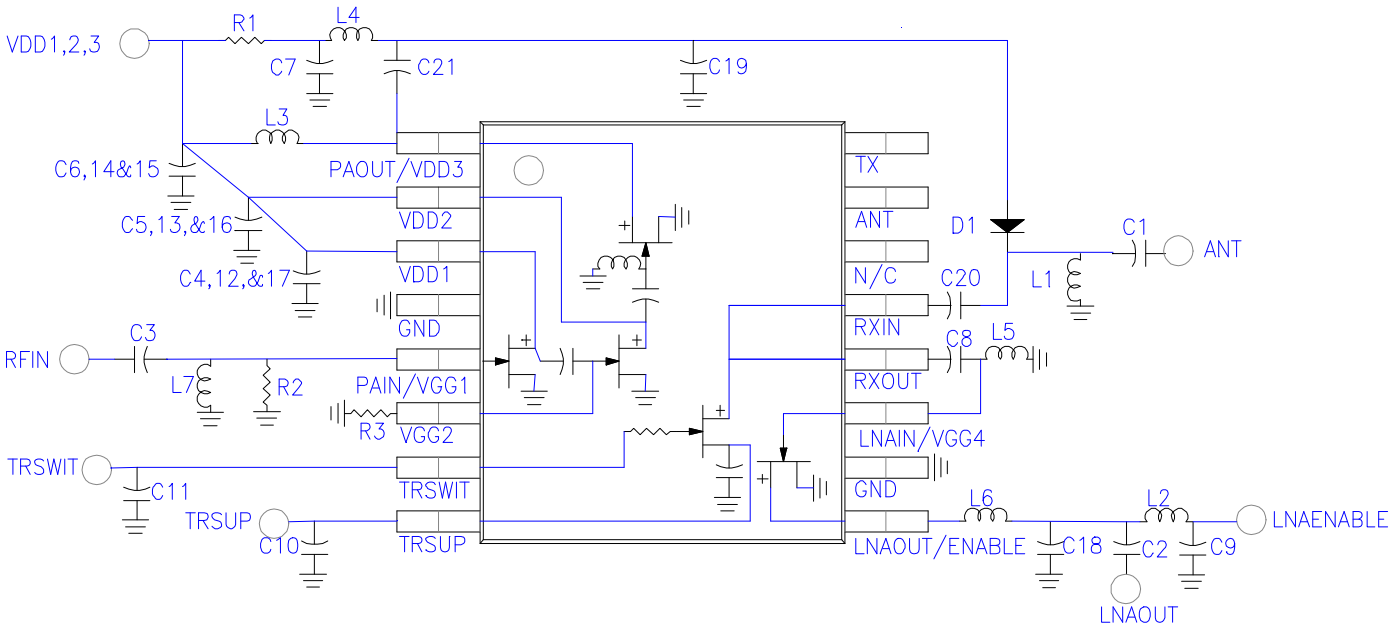

Figure 8. Evaluation Board Schematic

External components:

C1 – C11	MuRata 100 pF 0402 GRM36C0G101J50
C12 – C14	MuRata 0.1 µF 0402 GRM36Y5V104Z1
C15 – C17	MuRata 33 pF 0402 GRM36C0G330J50
C18 – C19	Dielectric Labs 2.2 pF 0603 C06CF2R2B5UL
C20	MuRata 22 pF 0402 GRM36C0G220G50
C21	MuRata 3 pF 0402 GRM36C0G030G50
L1 – L4	Coilcraft 27 nH 0603 0603CS-27NXJBB
L5	Toko 3.3 nH 0603 LL1608-F3N3K
L6	Coilcraft 7.5 nH 0402 0402 0402CS-7N5XJB
L7	Toko 2.7 nH 0805 LL2012-F2N7S
R1	Panasonic 150 Ω 0603 ERJ-3EKF1500
R2	Panasonic 301Ω 0603 ERJ-3EKF3010
R3	Panasonic 10 Ω 0603 ERJ-3EKF10R0V
D1	Siemens PIN Diode BAR6303W

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ITT GaAsTEK TEST SET UPS

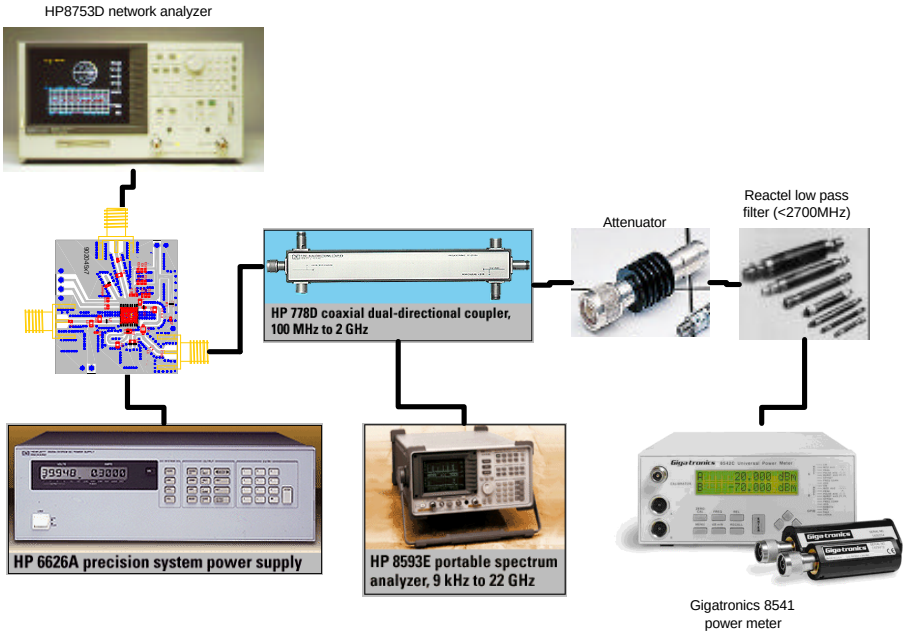

Figure 9. Transmit path power, current, and spurious.

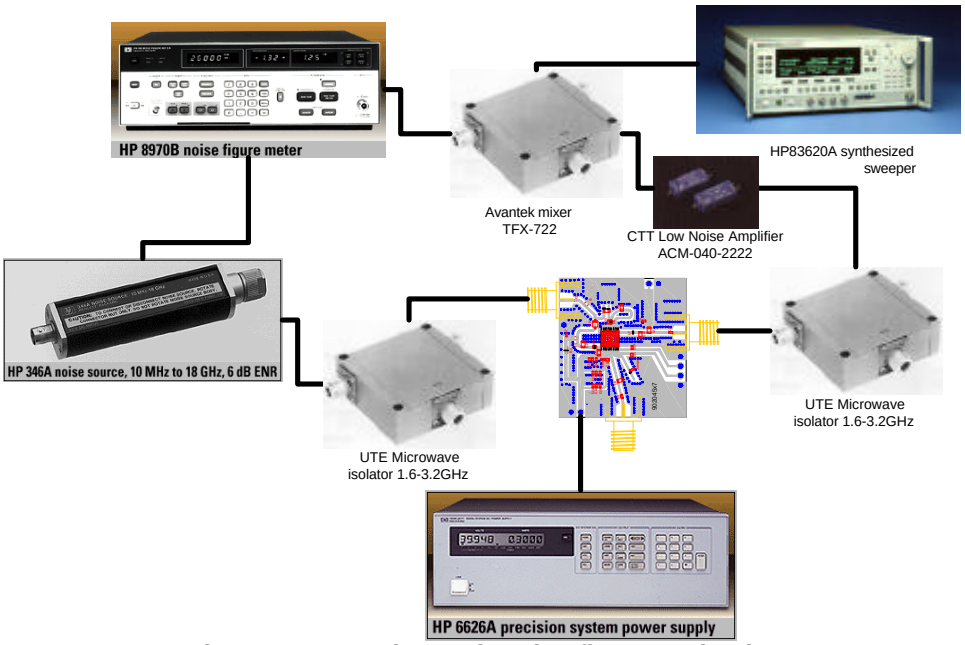

Figure 10. Receive path noise figure and gain.

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