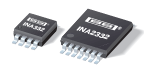
INA332
INA2332



SBOS216 – SEPTEMBER 2001

Low-Power, Single-Supply, CMOS INSTRUMENTATION AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- HIGH GAIN ACCURACY: G = 5, 0.07%, 2ppm/°C
- GAIN SET WITH EXT. RESISTORS FOR > 5V/V
- HIGH CMRR: 73dB DC, 50dB at 45kHz
- LOW BIAS CURRENT: 0.5pA
- BANDWIDTH, SLEW RATE: 2.0MHz, 5V/µs
- RAIL-TO-RAIL OUTPUT SWING: (V+) – 0.02V
- WIDE TEMPERATURE RANGE: –55°C to +125°C
- LOW QUIESCENT CURRENT: 490µA max/chan
- SHUT DOWN: 0.01µA
- MSOP-8 SINGLE AND TSSOP-14 DUAL PACKAGES

APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS: Bridge, RTD, Thermocouple, Position
- PHYSIOLOGICAL AMPLIFIERS: ECG, EEG, EMG
- A/D CONVERTER SIGNAL CONDITIONING
- DIFFERENTIAL LINE RECEIVERS WITH GAIN
- FIELD UTILITY METERS
- PCMCIA CARDS
- AUDIO AMPLIFIERS
- COMMUNICATION SYSTEMS
- TEST EQUIPMENT
- AUTOMOTIVE INSTRUMENTATION

DESCRIPTION

The INA332 and INA2332(1) are rail-to-rail output, low-power CMOS instrumentation amplifiers that offer wide range, single-supply and bipolar-supply operation. Using a special manufacturing flow, the INA332 family provides the lowest cost available, while still acheiving low-noise amplification of differential signals with low quiescent current of 415µA (dropping to 1µA when shutdown). Returning to normal operation within microseconds, this INA can be used for battery or multi-channel applications.

Configured internally for gain of 5V/V, the INA332 offers flexibility in higher gains by choosing external resistors.

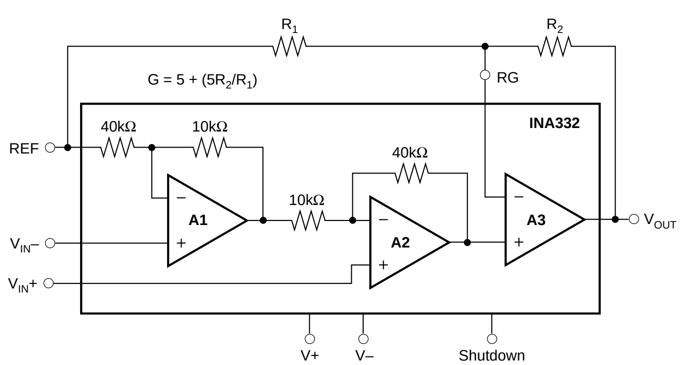
The INA332 rejects line noise and its harmonics because common-mode error remains low even at higher frequencies.

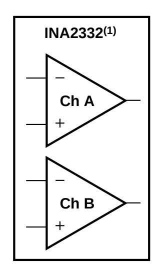
High bandwidth and slew rate make the INA332 ideal for directly driving sampling Analog-to-Digital (A/D) converters as well as general-purpose applications.

With high precision, low cost, and small packages, the INA332 outperforms discrete designs.

Additionally, because they are specified for wide temperature range of –55°C to +125°C and operating range of –65°C to +150°C, the INA331 family can be used in demanding industrial and automotive environments.

NOTE: (1) INA2332 available0 Q4 2001.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	7.5V
Signal Input Terminals, Voltage(2)	(V–) – 0.5V to (V+) + 0.5V
Current(2)	10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

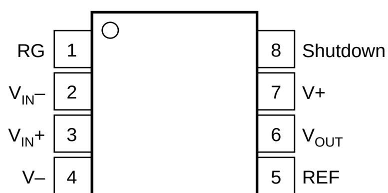
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE	SPECIFIED PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Single						
INA332AIDGK	MSOP-8	DGK	–55°C to +125°C	B32	INA332AIDGKT	Tape and Reel, 250
"	"	"	"	"	INA332AIDGKR	Tape and Reel, 2500
Dual						
INA2332AIPW(1)	TSSOP-14	PW	–55°C to +125°C	2332A	INA2332AIPWT	Tape and Reel, 250
"	"	"	"	"	INA2332AIPWR	Tape and Reel, 2500

NOTE: (1) Shaded product will be available Q4 2001.

PIN CONFIGURATION

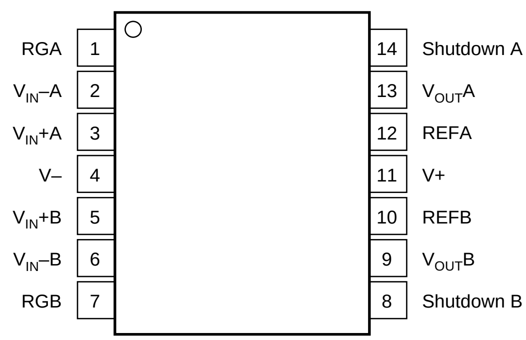
Top View

INA332



MSOP-8 (DGK)

INA2332(1)



Dual, TSSOP-14 (PW)

ELECTRICAL CHARACTERISTICS: V_S = +2.7V TO +5.5V

BOLDFACE limits apply over the specified temperature range, **T_A = –55°C TO 125°C**

At T_A = +25°C, R_L = 10kΩ, G = 25, and V_{CM} = V_S/2, unless otherwise noted.

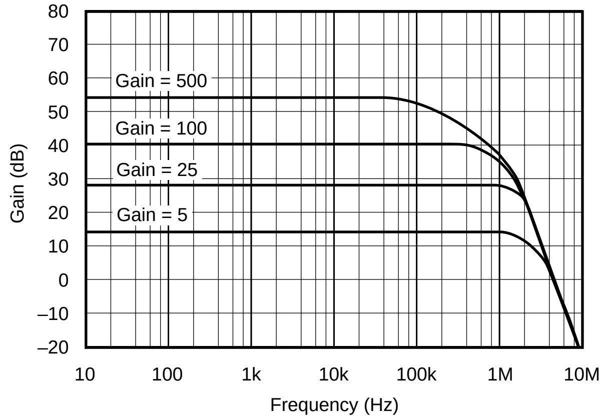
PARAMETER	CONDITION	INA332AIDGK INA2332AIPW(1) MIN	TYP	MAX	UNITS
INPUT					
Input Offset Voltage, RTI	V_S = +5V		±2	±8	mV
Over Temperature **V_{OS}**				**±9**	**mV**
vs Temperature **dV_{OS}/dT**			**±5**		**μV/°C**
vs Power Supply PSRR	V_S = +2.7V to +5.5V		±50	±250	μV/V
Over Temperature				**±260**	**μV/V**
Long-Term Stability			±0.4		μV/month
Input Impedance			10^{13} || 3		Ω || pF
Input Common-Mode Range	V_S = 2.7V	0.35		1.5	V
	V_S = 5V	0.55		3.8	V
Common-Mode Rejection CMRR	V_S = 5V, V_{CM} = 0.55V to 3.8V	60	73		dB
Over Temperature	**V_S = 5V, V_{CM} = 0.55V to 3.8V**	**60**			**dB**
	V_S = 2.7V, V_{CM} = 0.35V to 1.5V		73		dB
Crosstalk, Dual			110		dB
INPUT BIAS CURRENT	V_{CM} = V_S/2				
Bias Current I_B			±0.5	±10	pA
Offset Current I_{OS}			±0.5	±10	pA
NOISE, RTI	R_S = 0Ω				
Voltage Noise: f = 10Hz			280		nV/√Hz
f = 100Hz			96		nV/√Hz
f = 1kHz			46		nV/√Hz
f = 0.1Hz to 10Hz			7		μVp-p
Current Noise: f = 1kHz			0.5		fA/√Hz
GAIN(2)					
Gain Equation, Externally Set	G > 5		G = 5 + 5(R2/R1)		
Range of Gain		5		1000	V/V
Gain Error			±0.07	±0.4	%
vs Temperature	**G = 5**		**±2**	**±10**	**ppm/°C**
Nonlinearity	G = 25, V_S = 5V, V_O = 0.05 to 4.95		±0.001	±0.010	% of FS
Over Temperature			**±0.002**	**±0.04**	**% of FS**
OUTPUT					
Output Voltage Swing from Rail(3)	G ≥ 10	50	25		mV
Over Temperature		**50**			**mV**
Capacitance Load Drive			See Typical Characteristics(4)		pF
Short-Circuit Current I_{SC}			±40		mA
FREQUENCY RESPONSE					
Bandwidth, –3dB BW	G = 25		2.0		MHz
Slew Rate SR	V_S = 5V, G = 25		5		V/μs
Settling Time, 0.1% t_S	G = 25, C_L = 100pF, V_O = 2V step		1.7		μs
0.01%			2.5		μs
Overload Recovery	50% Input Overload G = 25		2		μs
POWER SUPPLY					
Specified Voltage Range		+2.7		+5.5	V
Operating Voltage Range			+2.5 to +5.5		V
Quiescent Current per Channel I_Q	V_{SD} > 2.5(5)		415	490	μA
Over Temperature				**600**	**μA**
Shutdown Quiescent Current/Chan I_{SD}	V_{SD} < 0.8(5)		0.01	1	μA
TEMPERATURE RANGE					
Specified Range		–55		+125	°C
Operating/Storage Range		–65		+150	°C
Thermal Resistance θ_{JA}	MSOP-8, TSSOP-14 Surface Mount		150		°C/W

NOTES: (1) Available Q4 2001. (2) Does not include errors from external gain setting resistors (3) Output voltage swings are measured between the output and power-supply rails. Output swings to rail only if G ≥ 10. Output does not swing to positive rail if gain is less than 10. (4) See typical characteristic "Percent Overshoot vs Load Capacitance." (5) See typical characteristic "Shutdown Voltage vs Supply Voltage."

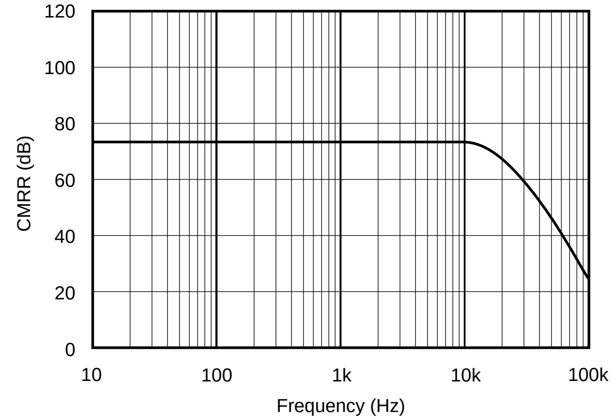
TYPICAL CHARACTERISTICS

At $T_A = +25°C$, $V_S = 5V$, $V_{CM} = V_S/2$, $R_L = 10k\Omega$, and $C_L = 100pF$, unless otherwise noted.

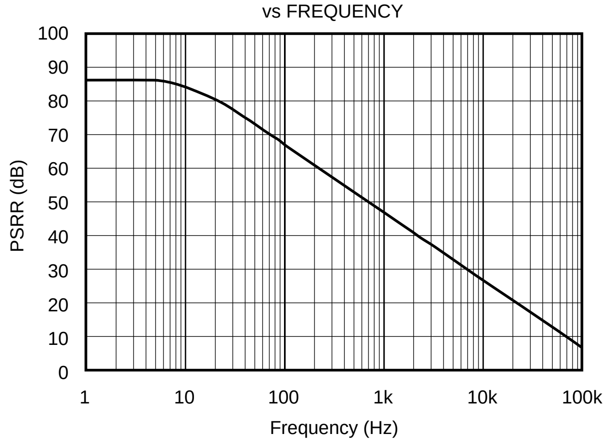
GAIN vs FREQUENCY



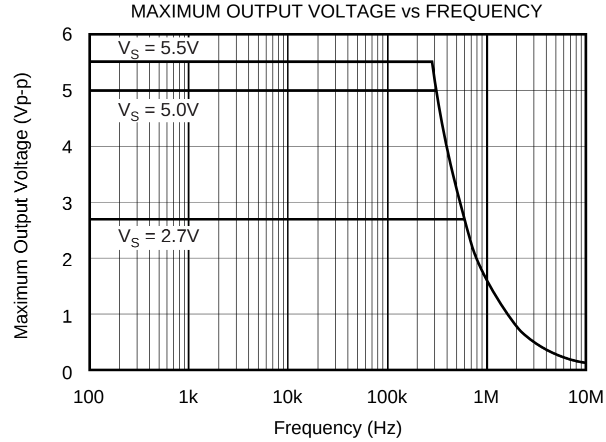
COMMON-MODE REJECTION RATIO
vs FREQUENCY



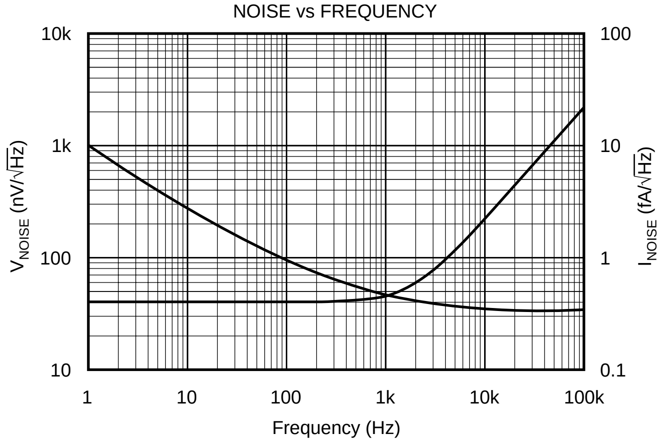
POWER-SUPPLY REJECTION RATIO
vs FREQUENCY



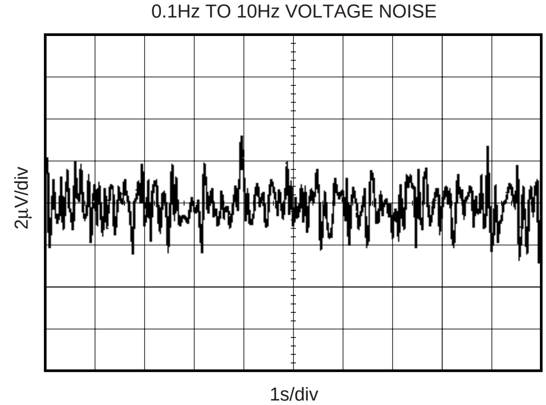
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



NOISE vs FREQUENCY

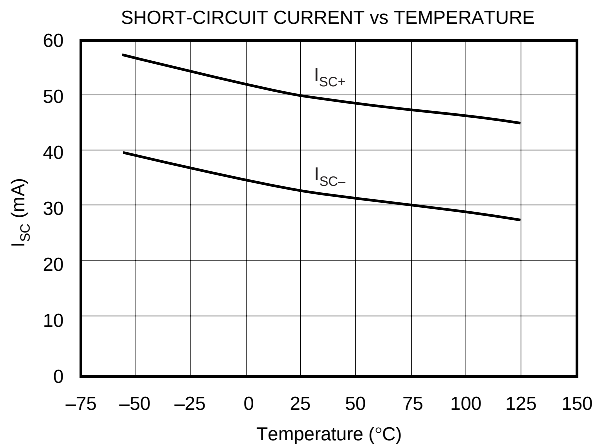


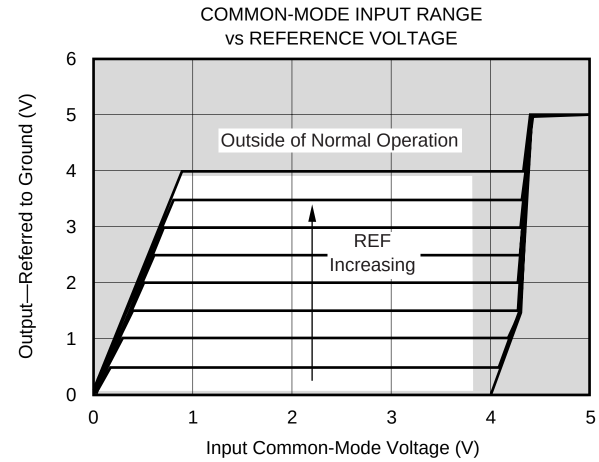
0.1Hz TO 10Hz VOLTAGE NOISE

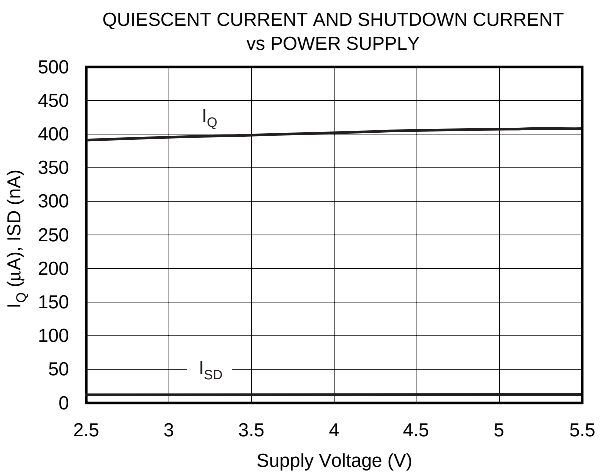


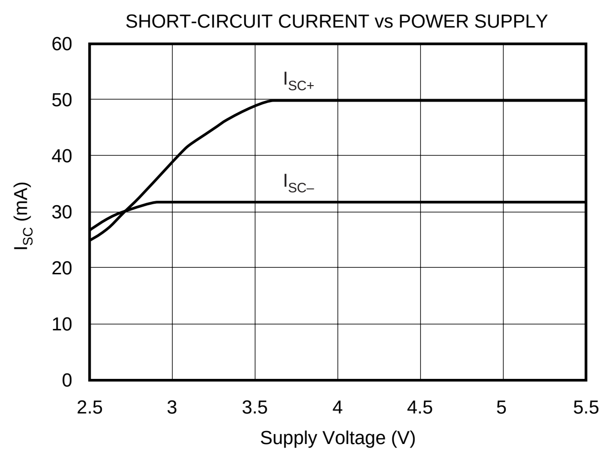
TYPICAL CHARACTERISTICS (Cont.)

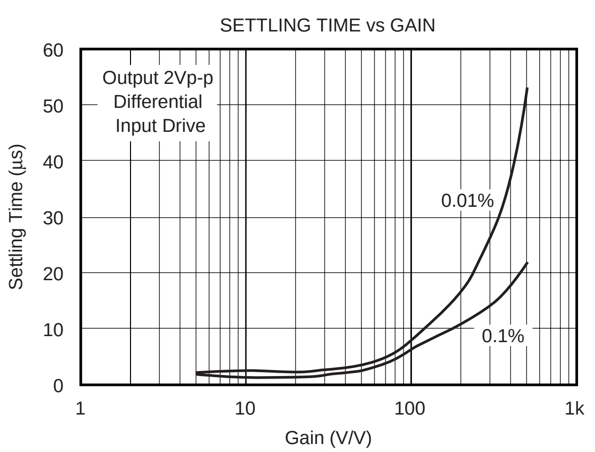
At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

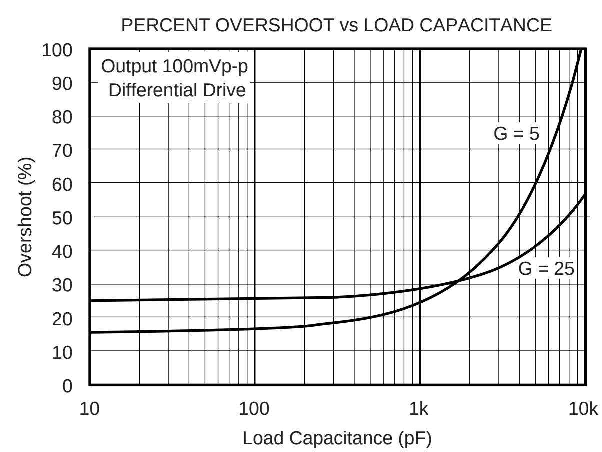








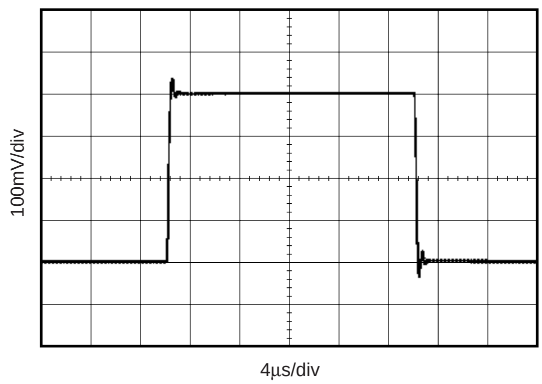




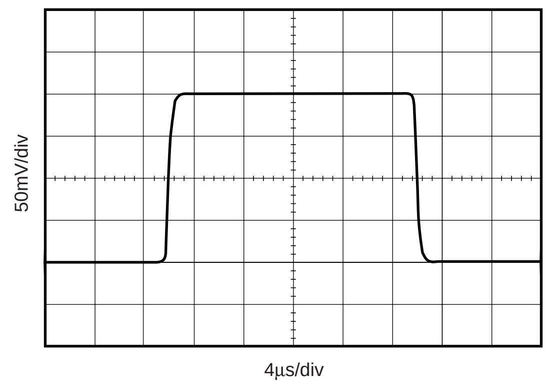
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

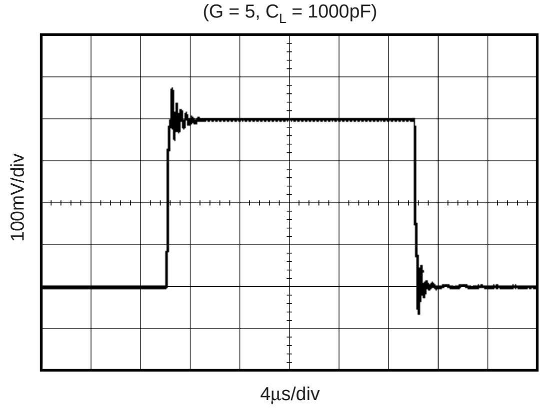
SMALL-SIGNAL STEP RESPONSE (G = 5)



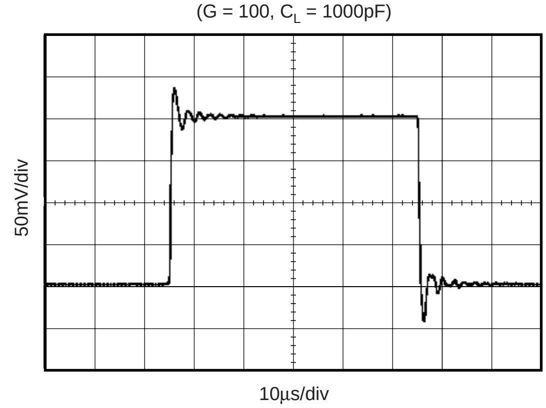
SMALL-SIGNAL STEP RESPONSE (G = 100)



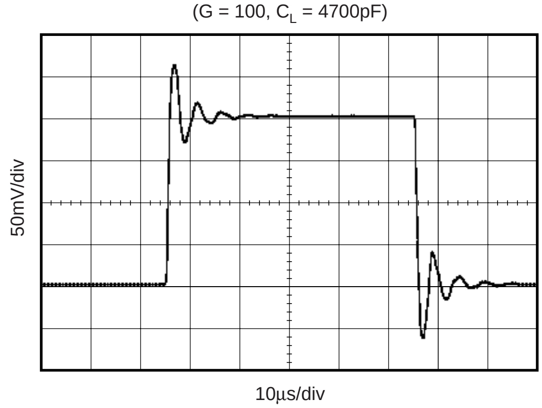
SMALL-SIGNAL STEP RESPONSE
(G = 5, C_L = 1000pF)



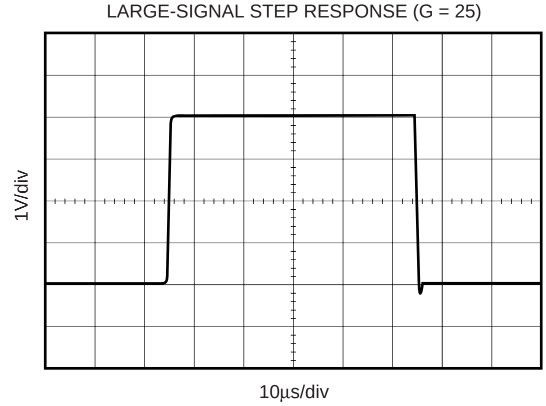
SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 1000pF)



SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 4700pF)

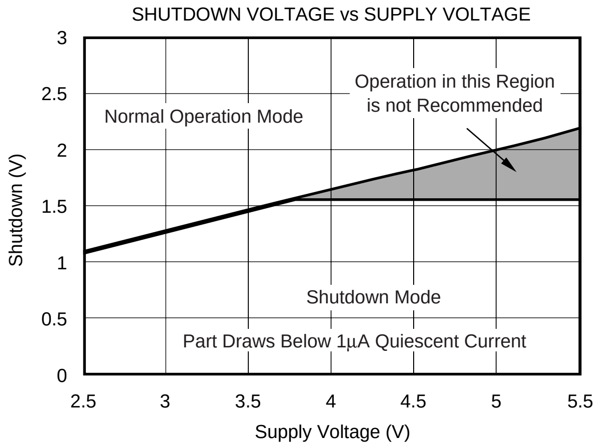


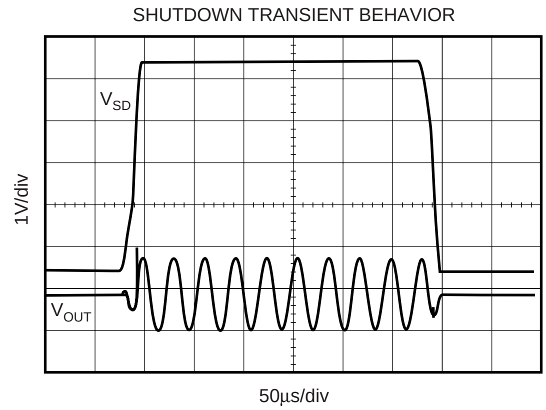
LARGE-SIGNAL STEP RESPONSE (G = 25)

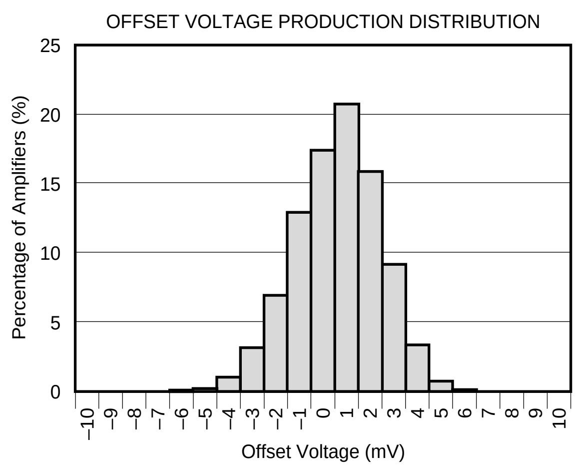


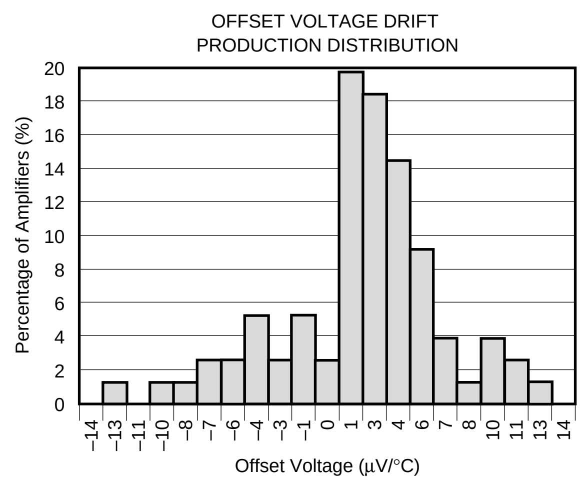
TYPICAL CHARACTERISTICS (Cont.)

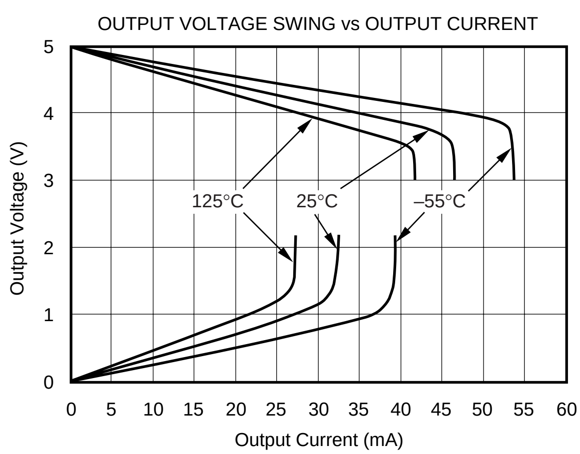
At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

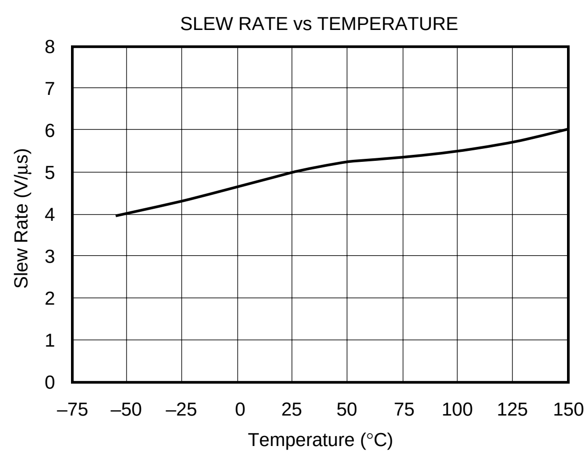












APPLICATIONS INFORMATION

The INA332 is a modified version of the classic "two op amp" instrumentation amplifier, with an additional gain amplifier.

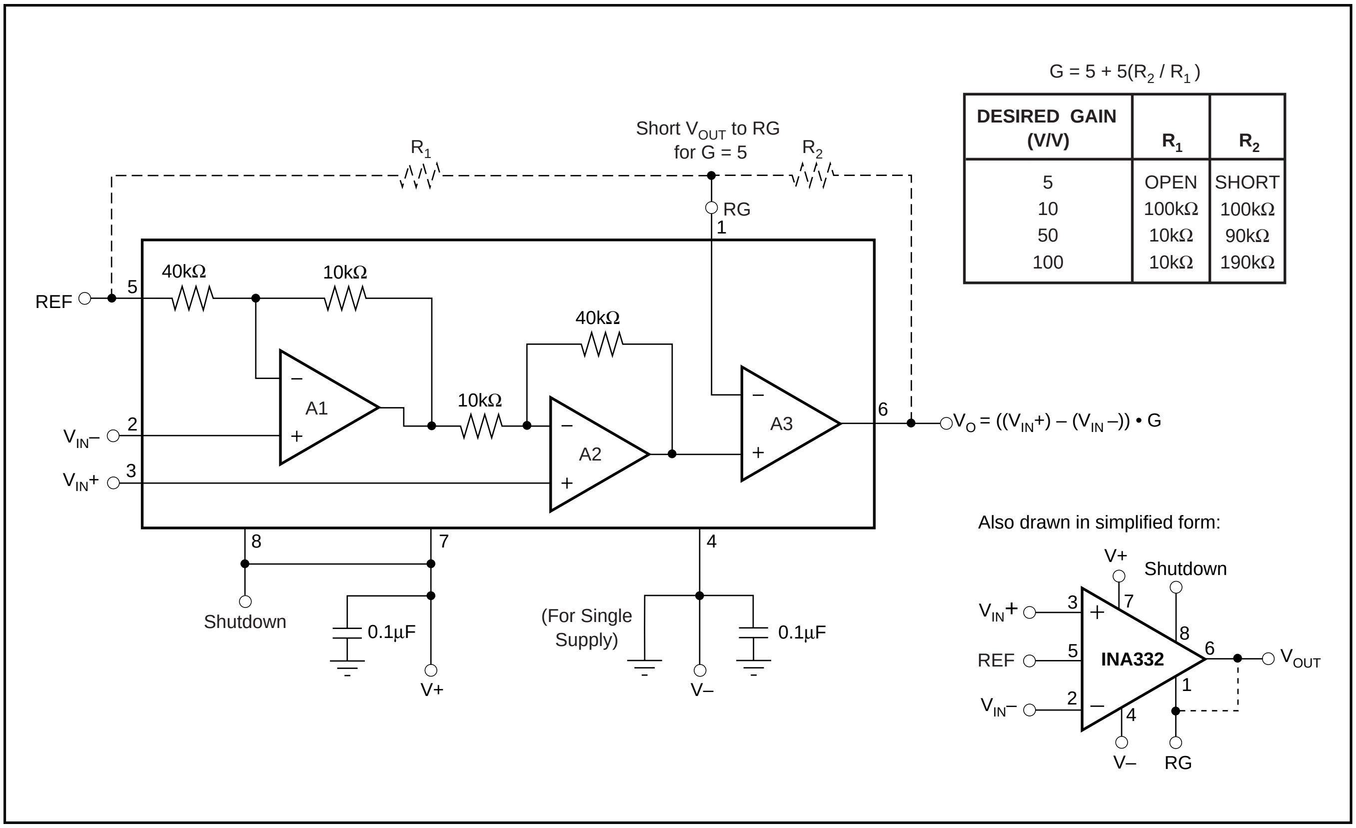
Figure 1 shows the basic connections for the operation of the INA332 and INA2332. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA332 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

OPERATING VOLTAGE

The INA332 family is fully specified and guaranteed over a supply range of +2.7V to +5.5V, with key parameters guaranteed over the temperature range of –55°C to +125°C. Parameters that vary significantly with operating conditions, such as load conditions or temperature, are shown in the Typical Characteristics.

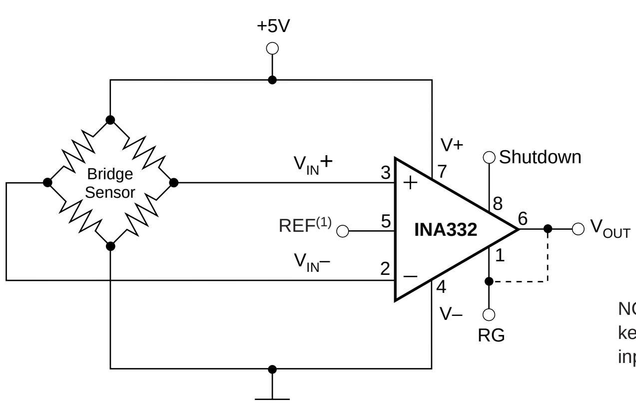
The INA332 may be operated on a single supply. Figure 2 shows a bridge amplifier circuit operated from a single +5V supply. The bridge provides a small differential voltage riding on an input common-mode voltage.



$G = 5 + 5(R_2 / R_1)$

DESIRED GAIN (V/V)	R_1	R_2
5	OPEN	SHORT
10	100kΩ	100kΩ
50	10kΩ	90kΩ
100	10kΩ	190kΩ

FIGURE 1. Basic Connections.



NOTE: (1) REF should be adjusted for the desired output level, keeping in mind that the value of REF affects the common-mode input range. See Typical Characteristics.

FIGURE 2. Single-Supply Bridge Amplifier.

SETTING THE GAIN

The ratio of R_2 to R_1, or the impedance between pins 1, 5, and 6, determines the gain of the INA332. With an internally set gain of 5, the INA332 can be programmed for gains greater than 5 according to the following equation:

$$G = 5 + 5(R_2/R_1)$$

The INA332 is designed to provide accurate gain, with gain error guaranteed to be less than 0.1%. Setting gain with matching TC resistors will minimize gain drift. Errors from external resistors will add directly to the guaranteed error, and may become dominant error sources.

COMMON-MODE INPUT RANGE

The upper limit of the common mode input range is set by the common-mode input range of the second amplifier, A2, to 1.2V below positive supply. Under most conditions, the amplifier operates beyond this point with reduced performance. The lower limit of the input range is bounded by the output swing of amplifier A1, and is a function of the reference voltage according to the following equation:

$$V_{OA1} = 5/4\ V_{CM} - 1/4\ V_{REF}$$

(See typical characteristic "Common-Mode Input Range vs Reference Voltage").

REFERENCE

The reference terminal defines the zero output voltage level. In setting the reference voltage, the common mode input of A3 should be considered according to the following equation:

$$V_{OA2} = V_{REF} + 5(V_{IN}+ - V_{IN}-)$$

For guaranteed operation, V_{OA2} should be less than $V_{DD} - 1.2V$.

The reference pin requires a low-impedance connection. As little as 160Ω in series with the reference pin will degrade the CMRR to 80dB. The reference pin may be used to compensate for the offset voltage (see Offset Trimming section). The reference voltage level also influences the common-mode input range (see Common-Mode Input Range section).

INPUT BIAS CURRENT RETURN

With a high input impedance of $10^{13}\Omega$, the INA332 is ideal for use with high-impedance sources. The input bias current of less than 10pA makes the INA332 nearly independent of input impedance and ideal for low-power applications.

For proper operation, a path must be provided for input bias currents for both inputs. Without input bias current paths, the inputs will "float" to a potential that exceeds common-mode range and the input amplifier will saturate. Figure 3 shows how bias current path can be provided in the cases of microphone applications, thermistor applications, ground returns, and dc-coupled resistive bridge applications.

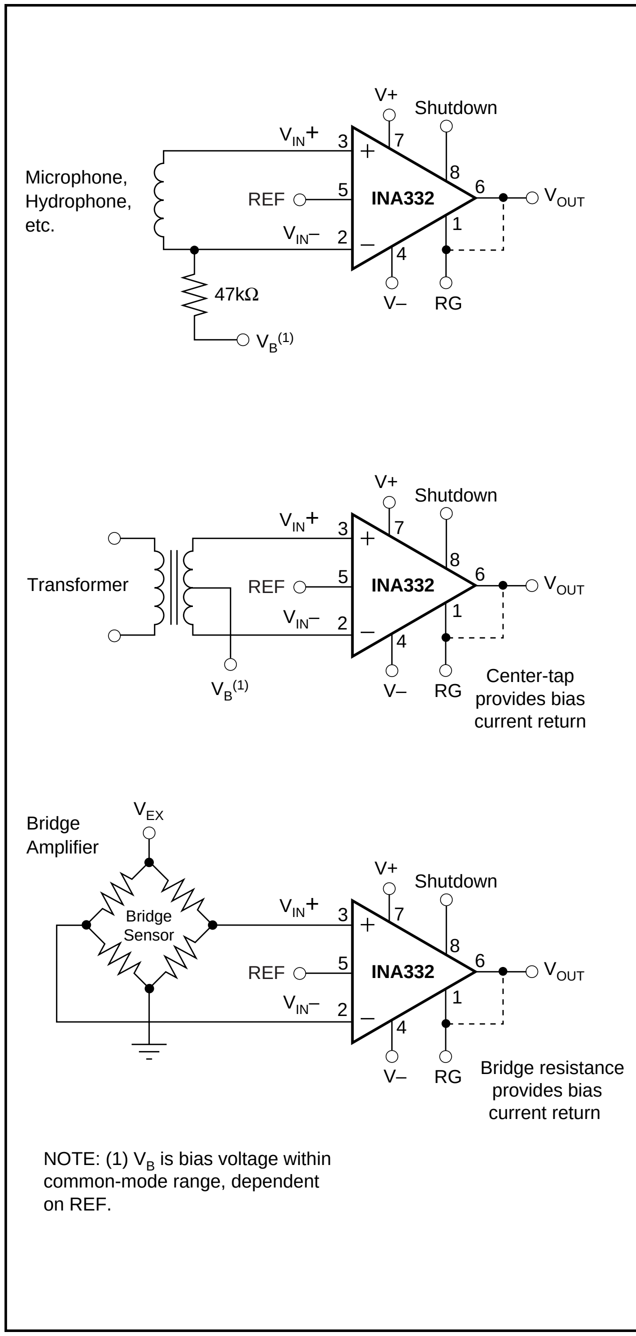


FIGURE 3. Providing an Input Common-Mode Path.

When differential source impedance is low, the bias current return path can be connected to one input. With higher source impedance, two equal resistors will provide a balanced input. The advantages are lower input offset voltage due to bias current flowing through the source impedance and better high-frequency gain.

SHUTDOWN MODE

The shutdown pin of the INA332 is nominally connected to V+. When the pin is pulled below 0.8V on a 5V supply, the INA332 goes into sleep mode within nanoseconds. For actual shutdown threshold, see typical characteristic "Shutdown Voltage vs Supply Voltage". Drawing less than 2µA of current, and returning from sleep mode in microseconds, the shutdown feature is useful for portable applications. Once in 'sleep-mode' the amplifier has high output impedance, making the INA332 suitable for multiplexing.

RAIL TO RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output for gains of 10 or greater. For resistive loads greater than 10kΩ, the output voltage can swing to within 25mV of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical characteristic "Output Voltage Swing vs Output Current." The INA332's low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 4.

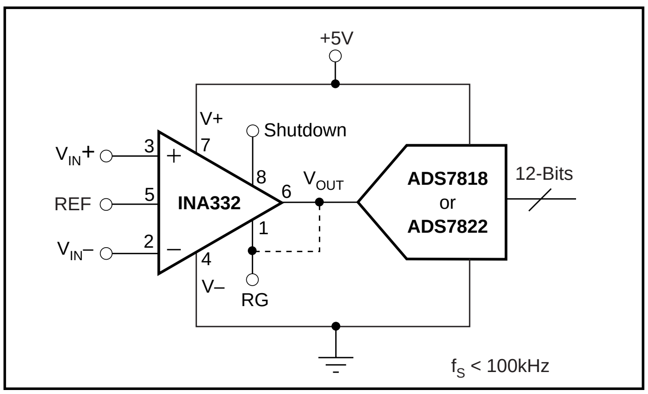


FIGURE 4. INA332 Directly Drives Capacitive-Input, High-Speed A/D Converter.

OUTPUT BUFFERING

The INA332 is optimized for a load impedance of 10kΩ or greater. For higher output current the INA332 can be buffered using the OPA340, as shown in Figure 5. The OPA340 can swing within 50mV of the supply rail, driving a 600Ω load. The OPA340 is available in the tiny MSOP-8 package.

OFFSET TRIMMING

The INA332 is laser trimmed for low offset voltage. In the event that external offset adjustment is required, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 6 shows an optional circuit for trimming offset voltage. The voltage applied to the REF terminal is added to the output signal. The gain from REF to V_{OUT} is +1. An op-amp buffer is used to provide low impedance at the REF terminal to preserve good common-mode rejection.

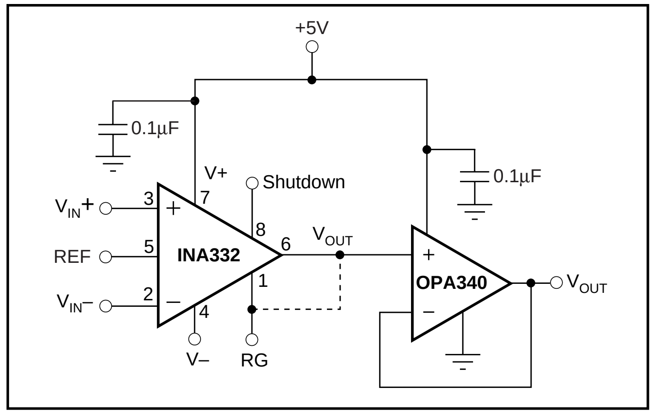


FIGURE 5. Output Buffering Circuit. Able to drive loads as low as 600Ω.

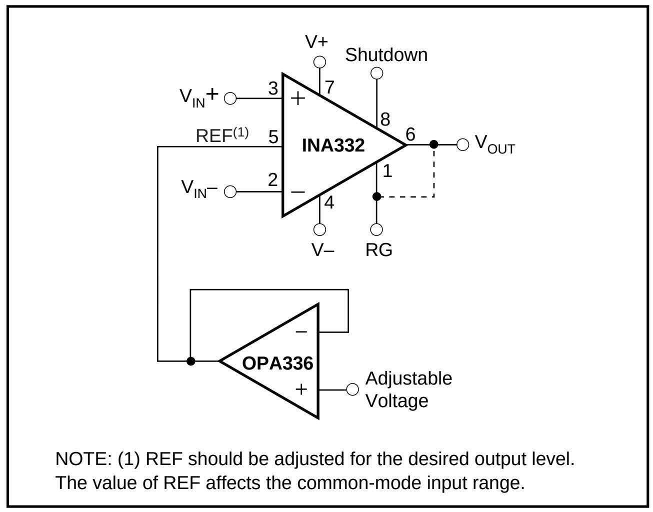


FIGURE 6. Optional Offset Trimming Voltage.

INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current through the input pins is limited to 10mA. This is easily accomplished with input resistor R_{LIM}, as shown in Figure 7. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

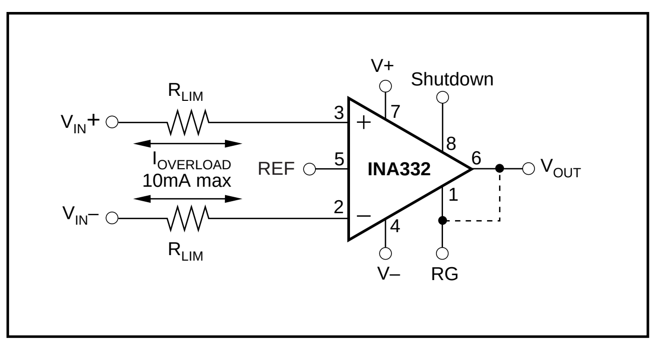


FIGURE 7. Sample Output Buffering Circuit.

OFFSET VOLTAGE ERROR CALCULATION

The offset voltage (V_{OS}) of the INA332AIDGK is specified at a maximum of 500µV with a +5V power supply and the common-mode voltage at $V_S/2$. Additional specifications for power-supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case expected offset under the conditions of a given application.

Power Supply Rejection Ratio (PSRR) is specified in µV/V. For the INA332, worst case PSRR is 200µV/V, which means for each volt of change in power supply, the offset may shift up to 200µV. Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to µV/V using the following equation:

$$\text{CMRR (in } \mu\text{V/V)} = 10^{[(\text{CMRR in dB})/-20]} \cdot 10^6$$

For the INA332, the worst case CMRR over the specified common-mode range is 60dB (at G = 25) or about 30µV/V This means that for every volt of change in common-mode, the offset will shift less than 30µV.

These numbers can be used to calculate excursions from the specified offset voltage under different application conditions. For example, an application might configure the amplifier with a 3.3V supply with 1V common-mode. This configuration varies from the specified configuration, representing a 1.7V variation in power supply (5V in the offset specification versus 3.3V in the application) and a 0.65V variation in common-mode voltage from the specified $V_S/2$.

Calculation of the worst-case expected offset would be as follows:

$$\begin{aligned}\text{Adjusted } V_{OS} = &\text{ Maximum specified } V_{OS} + \\ &\text{(power-supply variation)} \cdot \text{PSRR} + \\ &\text{(common-mode variation)} \cdot \text{CMRR}\end{aligned}$$

$$\begin{aligned}V_{OS} &= 0.5\text{mV} + (1.7\text{V} \cdot 200\mu\text{V}) + (0.65\text{V} \cdot 30\mu\text{V}) \\ &= \pm 0.860\text{mV}\end{aligned}$$

However, the typical value will be smaller, as seen in the Typical Characteristics.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 8. This capacitor compensates for the zero created by the feedback network impedance and the INA332's RG-pin input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks. Also, R_X and C_L can be added to reduce high-frequency noise.

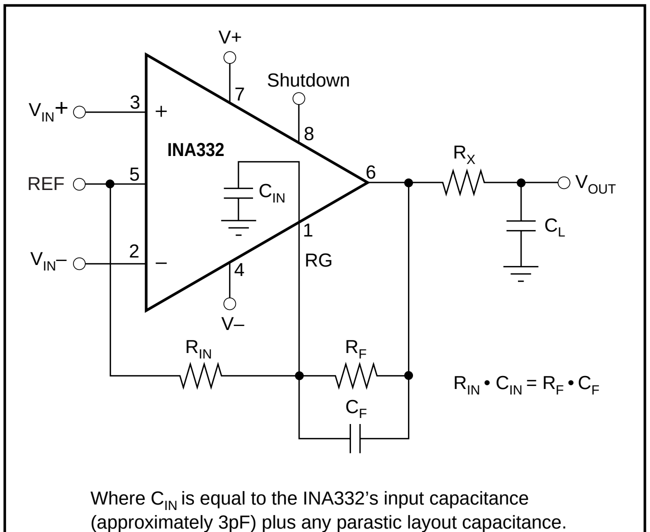


FIGURE 8. Feedback Capacitor Improves Dynamic Performance.

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between instrumentation amplifiers, and layout capacitance is difficult to determine. For the circuit shown in Figure 8, the value of the variable feedback capacitor should be chosen by the following equation:

$$R_{IN} \cdot C_{IN} = R_F \cdot C_F$$

Where C_{IN} is equal to the INA332's RG-pin input capacitance (typically 3pF) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

APPLICATION CIRCUITS

MEDICAL ECG APPLICATIONS

Figure 9 shows the INA332 configured to serve as a low-cost ECG amplifier, suitable for moderate accuracy heart-rate applications such as fitness equipment. The input signals are obtained from the left and right arms of the patient. The common-mode voltage is set by two 2MΩ resistors. This potential through a buffer, provides optional right leg drive. Filtering can be modified to suit application needs by changing the capacitor value of the output filter.

LOW-POWER, SINGLE-SUPPLY DATA ACQUISITION SYSTEMS

Refer to Figure 4 to see the INA332 configured to drive an ADS7818. Functioning at frequencies of up to 500kHz, the INA332 is ideal for low-power data acquisition.

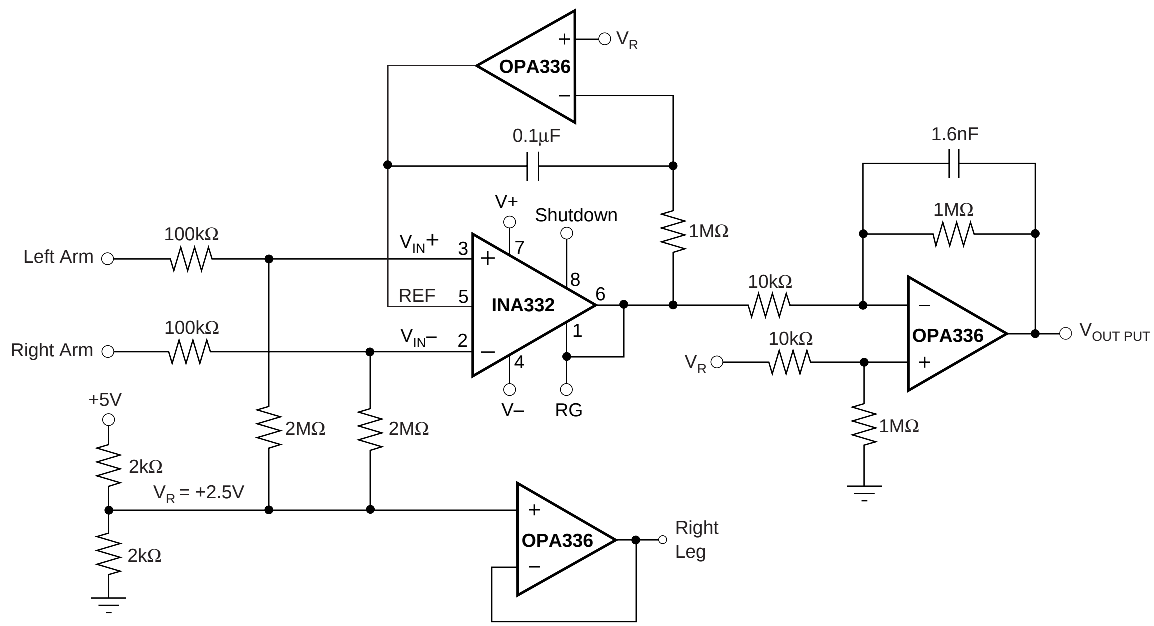
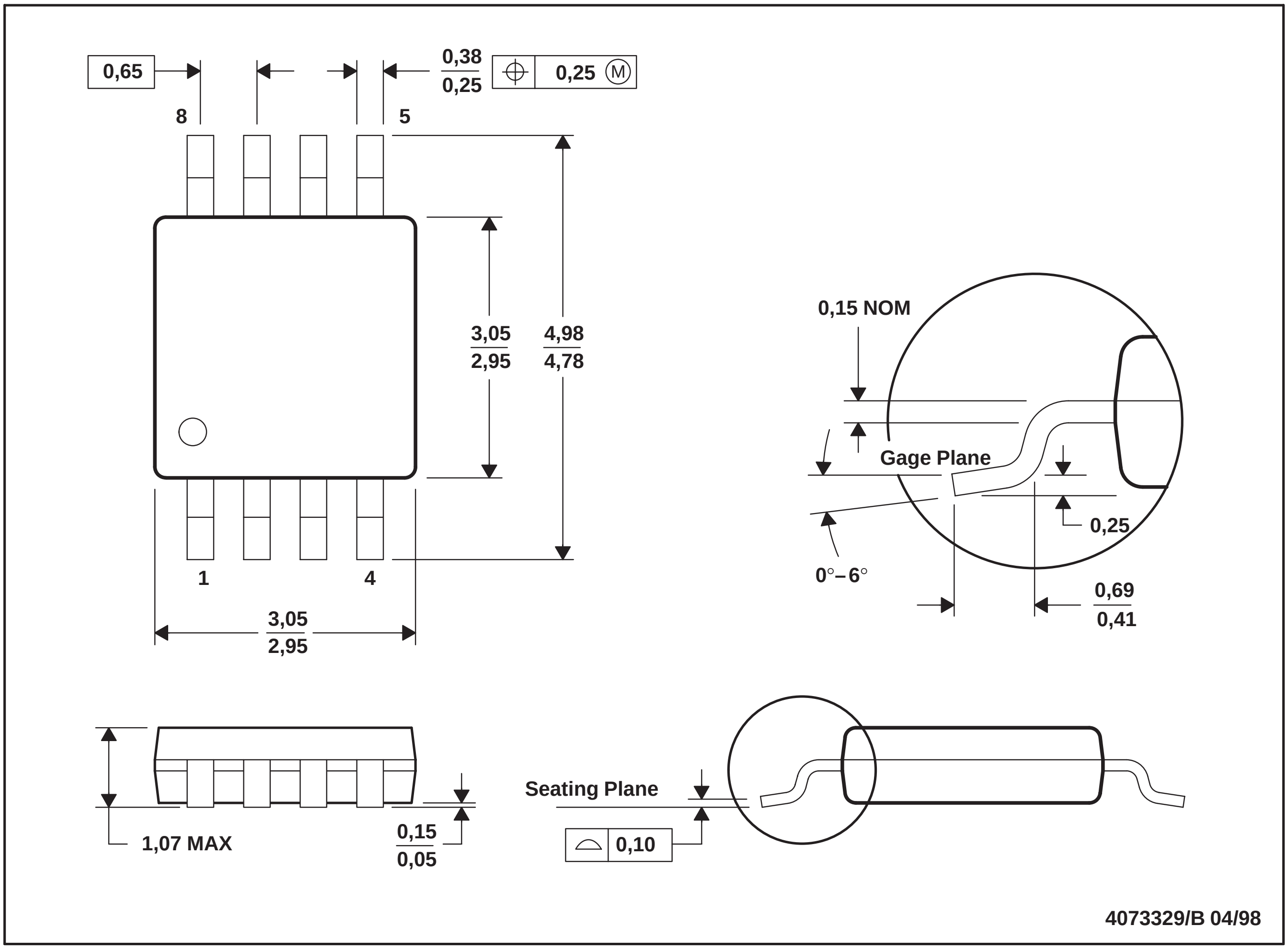


FIGURE 9. Simplified ECG Circuit for Medical Applications.

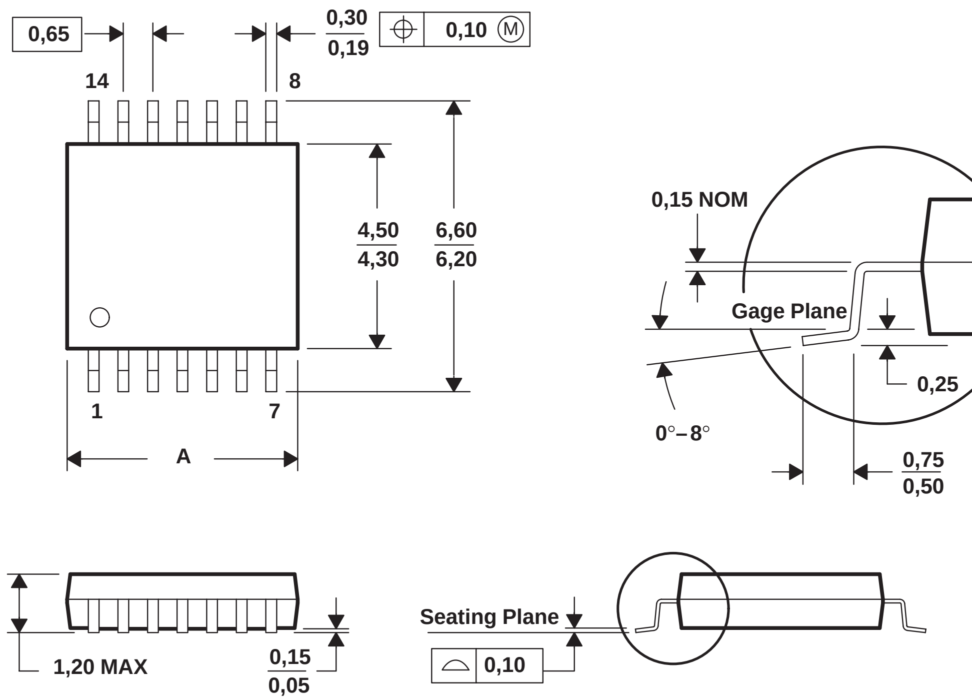
DGK (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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