256K X 36, 512K X 18 3.3V Synchronous SRAMs 2.5V I/O, Burst Counter Flow-Through Outputs, Single Cycle Deselect

Advance Information

IDT71V67702

IDT71V67902

Features

- **256K x 36, 512K x 18 memory configurations**
- **Supports fast access times:**
  - *7.5ns up to 117MHz clock frequency*
  - *8.0ns up to 100MHz clock frequency*
  - *8.5ns up to 87MHz clock frequency*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **2.5V I/O supply (V_{DDQ})**
- **Packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).**

Description

The IDT71V67702/7902 are high-speed SRAMs organized as 256K x 36/512K x 18. The IDT71V67702/7902 SRAMs contain write, data, address and control registers. There are no registers in the data output path (flow-through architecture). Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V67702/7902 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will flow-through from the array after a clock-to-data access time delay from the rising clock edge of the same cycle. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V67702/7902 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

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NOTE:

1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V67902.

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Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combi-nation of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O_{0-7}, I/O_{P1}, $\overline{BW_2}$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V67702/7902. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the inter-leaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	2.5V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	1	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V67702/7902 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

NOTE:
5317t tbl 02

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration – 256K x 36, 119 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{DDQ}
B	NC	CS_0(4)	A3	$\overline{ADSC}$	A9	A17	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O_{16}	I/OP_3	V_{SS}	NC	V_{SS}	I/OP_2	I/O_{15}
E	I/O_{17}	I/O_{18}	V_{SS}	$\overline{CE}$	V_{SS}	I/O_{13}	I/O_{14}
F	V_{DDQ}	I/O_{19}	V_{SS}	$\overline{OE}$	V_{SS}	I/O_{12}	V_{DDQ}
G	I/O_{20}	I/O_{21}	$\overline{BW_3}$	$\overline{ADV}$	$\overline{BW_2}$	I/O_{11}	I/O_{10}
H	I/O_{22}	I/O_{23}	V_{SS}	$\overline{GW}$	V_{SS}	I/O_9	I/O_8
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	I/O_{24}	I/O_{26}	V_{SS}	CLK	V_{SS}	I/O_6	I/O_7
L	I/O_{25}	I/O_{27}	$\overline{BW_4}$	NC	$\overline{BW_1}$	I/O_4	I/O_5
M	V_{DDQ}	I/O_{28}	V_{SS}	$\overline{BWE}$	V_{SS}	I/O_3	V_{DDQ}
N	I/O_{29}	I/O_{30}	V_{SS}	A_1	V_{SS}	I/O_2	I/O_1
P	I/O_{31}	I/OP_4	V_{SS}	A_0	V_{SS}	I/O_0	I/OP_1
R	NC	A_5	$\overline{LBO}$	V_{DD}	V_{SS}(1)	A_{13}	NC
T	NC	NC	A_{10}	A_{11}	A_{14}	NC	$\overline{ZZ}$(2)
U	V_{DDQ}	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	V_{DDQ}

5317 drw 02c

Top View

Pin Configuration – 512K x 18, 119 BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	$\overline{ADSP}$	A8	A16	V_{DDQ}
B	NC	CS_0(4)	A3	$\overline{ADSC}$	A9	A_{18}	NC
C	NC	A7	A2	V_{DD}	A_{13}	A17	NC
D	I/O_8	NC	V_{SS}	NC	V_{SS}	I/O_7	NC
E	NC	I/O_9	V_{SS}	$\overline{CE}$	V_{SS}	NC	I/O_6
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	I/O_5	V_{DDQ}
G	NC	I/O_{10}	$\overline{BW_2}$	$\overline{ADV}$	V_{SS}	NC	I/O_4
H	I/O_{11}	NC	V_{SS}	$\overline{GW}$	V_{SS}	I/O_3	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	I/O_{12}	V_{SS}	CLK	V_{SS}	NC	I/O_2
L	I/O_{13}	NC	V_{SS}	NC	$\overline{BW_1}$	I/O_1	NC
M	V_{DDQ}	I/O_{14}	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	I/O_{15}	NC	V_{SS}	A_1	V_{SS}	I/O_0	NC
P	NC	I/OP_2	V_{SS}	A_0	V_{SS}	NC	I/OP_1
R	NC	A_5	$\overline{LBO}$	V_{DD}	V_{SS}(1)	A_{12}	NC
T	NC	A_{10}	A_{15}	NC	A_{14}	A_{11}	$\overline{ZZ}$(2)
U	V_{DDQ}	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	V_{DDQ}

5317 drw 02d

Top View

NOTES:
1. R5 does not have to be directly connected to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. T7 can be left unconnected and the device will always remain in active mode.
3. DNU= Do not use; these signals can either be left unconnected or tied to Vss.
4. On future 18M device CS_0 will be removed, B2 will be used for address expansion.

Pin Configuration – 256K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(3)	A7	$\overline{CE}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	NC
B	NC	A6	CS0	$\overline{BW_4}$	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(3)
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VSS(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(2)
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	NC	NC(3)	NC	VSS	VDDQ	NC	I/OP1
P	NC	NC(3)	A5	A2	DNU(4)	A1	DNU(4)	A10	A13	A14	A17
R	$\overline{LBO}$	NC(3)	A4	A3	DNU(4)	A0	DNU(4)	A11	A12	A15	A16

5317tbl 17a

Pin Configuration – 512K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(3)	A7	$\overline{CE}$	$\overline{BW_2}$	NC	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	A10
B	NC	A6	CS0	NC	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(3)
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VSS(1)	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(2)
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	NC	NC(3)	NC	VSS	VDDQ	NC	NC
P	NC	NC(3)	A5	A2	DNU(4)	A1	DNU(4)	A11	A14	A15	A18
R	$\overline{LBO}$	NC(3)	A4	A3	DNU(4)	A0	DNU(4)	A12	A13	A16	A17

5317 tbl 17b

NOTES:
1. H1 does not have to be directly connected to VSS, as long as the input voltage is ≤ VIL.
2. H11 can be left unconnected and the device will always remain in active mode.
3. Pin N6, B11, A1, R2 and P2 are reserved for 18M, 36M, 72M, and 144M and 288M respectively.
4. DNU= Do not use; these signals can either be left unconnected or tied to Vss.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +6mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -6mA, V_{DD} = Min.	2.0	—	V

5317 tbl 08

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ in will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range [1]

Symbol	Parameter	Test Conditions	7.5ns	8ns	8.5ns	Unit
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	265	210	190	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	50	50	50	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX} [2,3]	145	140	135	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	50	50	50	mA

5317 tbl 09

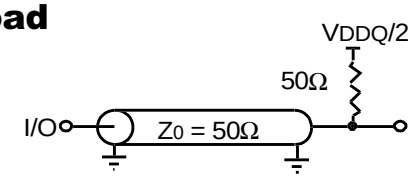
NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 2.5V)

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	(V_{DDQ}/2)
Output Timing Reference Levels	(V_{DDQ}/2)
AC Test Load	See Figure 1

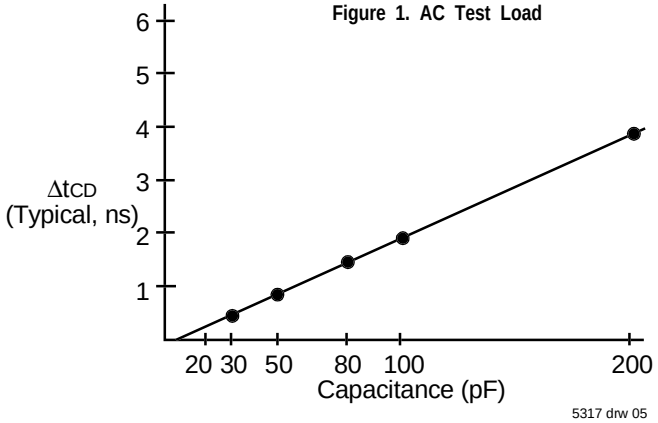
5317 tbl 10

AC Test Load



5317 drw 03

Figure 1. AC Test Load



5317 drw 05

Figure 2. Lumped Capacitive Load, Typical Derating

Datasheet Document History

12/31/99		Created Datasheet from 71V677 and 71V679 Datasheets
		For 3.3V I/O offering, see 71V67703 and 71V67903 Datasheets
04/26/00	Pg. 4	Add capacitance for BGA package; Insert clarification note to Absolute Max Ratings and Recommended Operating Temperature tables.
	Pg. 7	Replace Pin U6 with $\overline{TRST}$ pin in BGA pin configuration; Add pin description note in pinout
	Pg. 18	Inserted 100 pin TQFP Package Diagram Outline
05/24/00	Pg. 1,4,8,21 22	Add new package offering, 13 x 15 fBGA
	Pg. 5,6,7,8	Correct note 2 on BGA and TQFP pin configuration
	Pg. 20	Correction in the 119 BGA Package Diagram Outline
07/12/00	Pg. 5,6,8	Remove note from TQFP and BQ165 pinout
	Pg. 7	Add/Remove reference note from BG119 pinout
	Pg. 20	Update BG119 package diagram outline dimensions
07/16/01	Pg. 9	Updated ISB2 levels for tcd = 7.5ns - 8.5ns
10/29/01	Pg. 1,2	Remove JTAG pins
	Pg. 7	Changed U2-U6 pins to DNU
	Pg. 8	Changed P5, P7, R5 & R7 pins to DNU
	Pg. 9	Raise specs on 7.5ns, 8ns & 8.5ns by 10mA

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