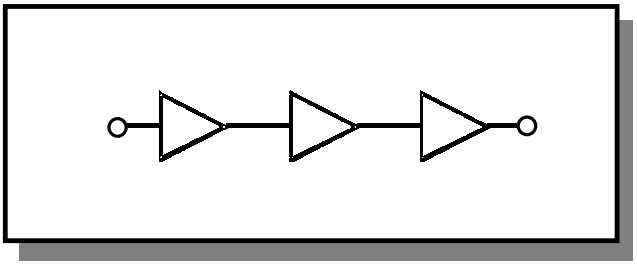
2.5W Power Amplifier Die (13.5 – 14.5 GHz)
ITT8502D

ADVANCED INFORMATION

FEATURES

- 15% Typical Power Added Efficiency
- High Linear Gain: 19 dB typical
- 50 Ω Input/Output Impedance
- Self-Aligned MSAG® MESFET Process



DESCRIPTION

The ITT8502D is a three stage MMIC power amplifier fabricated using GaAsTEK's mature GaAs Self-Aligned MSAG® MESFET Process. This product is fully matched to 50 ohms on both the input and the output.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

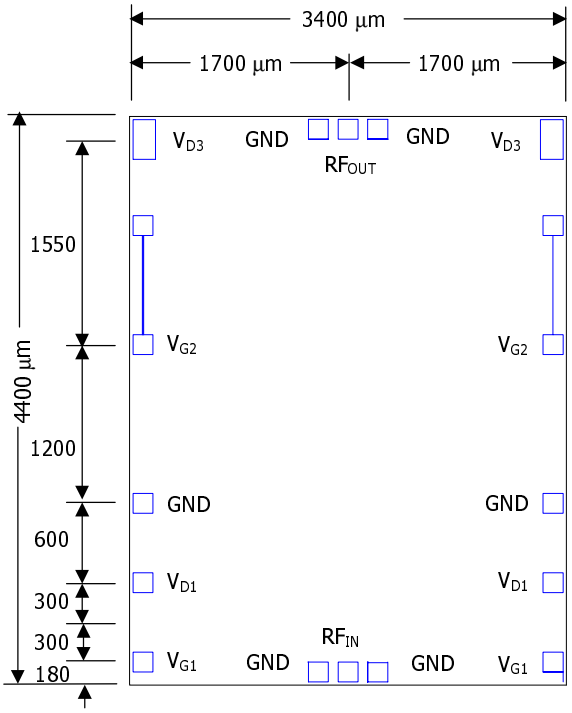
Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	12	Vdc
DC Gate Supply Voltage	V_{GG}	-4	Vdc
Power Dissipation (T_{BASE} = 70 °C)	P_{DISS}	-	W
RF Input Power	P_{IN}	200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-40 to +85	°C

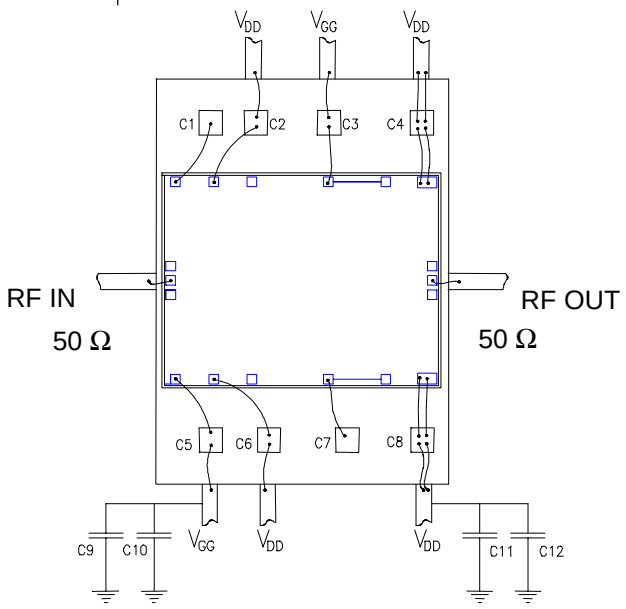
ELECTRICAL CHARACTERISTICS (V_{DD}=9.0 V, V_{GG}=-1.8 V, T_A=25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	13.5	—	14.5	GHz
Output Power, Saturated	P_{SAT}		34		dBm
Output Power, P_{1dB}	P_{1dB}		33		dBm
Power Gain (Linear)	G_P		19		dB
Gain Flatness Over Frequency	-		+/- 1.0		dB
Power Added Efficiency	η		15		%
Input VSWR	-		2:1		
Noise Figure	NF		11		
Harmonics	Nf_o			-20	dBc
Spurious	-			-60	dBc
Third-Order Intercept Point	TOI		40		dBm

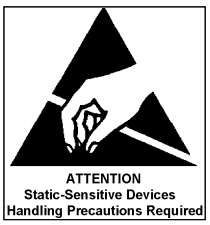
GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

LAYOUT AND BONDING DIAGRAMS





Pad Sizes: 150 X 150 microns for all except V_{D3} (150 X 300 microns).



List of components:
C1 thru C8 = 100pF single layer ceramic chip capacitor
C9 = C11 = 0.1 uF ceramic chip capacitor
C10 = C12 = 5000 pF capacitor

Assembly:

Chip dimensions: 4.4mm x 4.4mm, .003" thickness.
Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.
Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing:
1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616