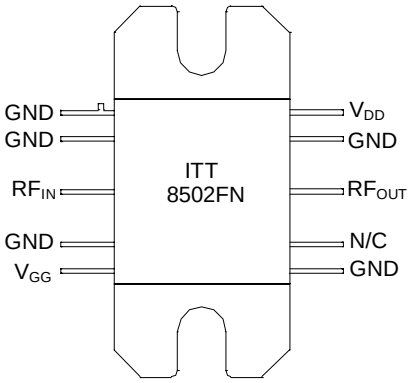
2W Power Amplifier (13 – 15 GHz)
ITT8502

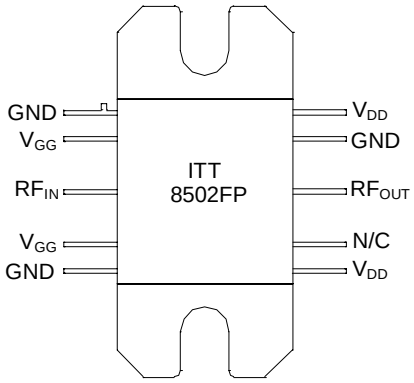
ADVANCED INFORMATION

FEATURES

- 24% Typical Power Added Efficiency
- 17.5 dB Typical Small Signal Gain
- 39.5 dBm Third Order Intercept Point
- Flange mount package designed for optimum electrical and thermal performance at Ku-band.
- Broadband design centered on Ku-band VSAT.
- Consistent Output Power and Gain makes fixed bias possible.



FN Package Pin Configuration



FP Package Pin Configuration

DESCRIPTION

The ITT8502 is a three stage MMIC power amplifier fabricated using GaAsTEK's Self-Aligned MSAG® MESFET Process. It is designed primarily for Ku-band VSAT applications, but is a broadband amplifier that can be used for other microwave applications as well. This product is fully matched to 50 ohms on both the input and the output.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	10	Vdc
DC Gate Supply Voltage	V_{GG}	-4	Vdc
Power Dissipation (T_{BASE} = 70 °C)	P_{DISS}	-	W
RF Input Power	P_{IN}	200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 9.0 V, P_{IN} = 17 dBm, V_{GG} = -2.2 V, T_A = 25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	13.75	—	14.5	GHz
Output Power, Saturated	P_{SAT}	—	33.5	—	dBm
Output Power, P_{1dB}	P_{1dB}	—	33	—	dBm
Gain at P_{1dB}	G_{1dB}	—	17	—	dB
Gain Flatness Over Frequency	-	—	+/- 1.0	—	dB
Power Added Efficiency	η	—	24	—	%
Drain Current @ P_{1dB}	$I_{D,1dB}$	—	1.1	—	A
Gate Current	I_{GG}	—	10	—	mA
Input VSWR	-	—	1.4:1	—	—
Harmonics (f_o=14.0 GHz, P_{OUT}=33 dBm)	$2f_o$	—	-48	-20	dBc
Third-Order Intercept Point	IP_3	—	39.5	—	dBm

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

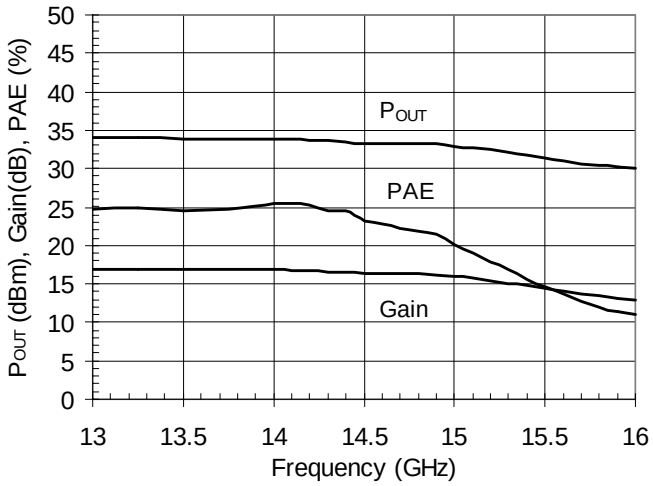


Figure 1. Saturated Output Power, Efficiency, and Input Return Loss vs. Frequency

Conditions: V_{DD} = 9V, V_{GG} = -2.2V, P_{IN} = 17 dBm

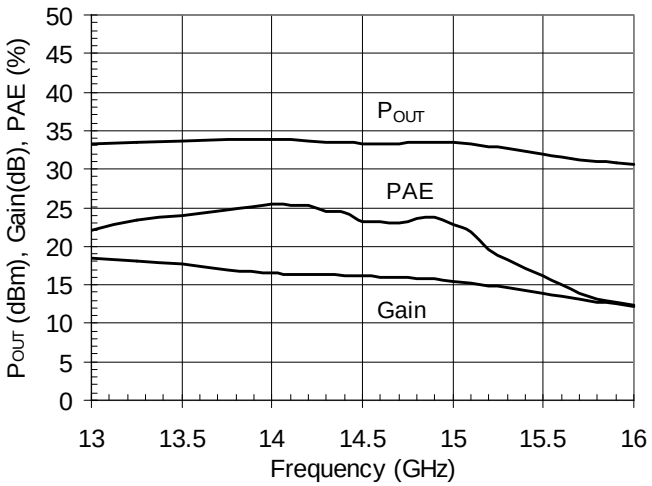


Figure 2. Output Power at P-1dB, Efficiency, and Gain vs. Frequency

Conditions: V_{DD} = 9V, V_{GG} = -2.2V, P_{IN} varies

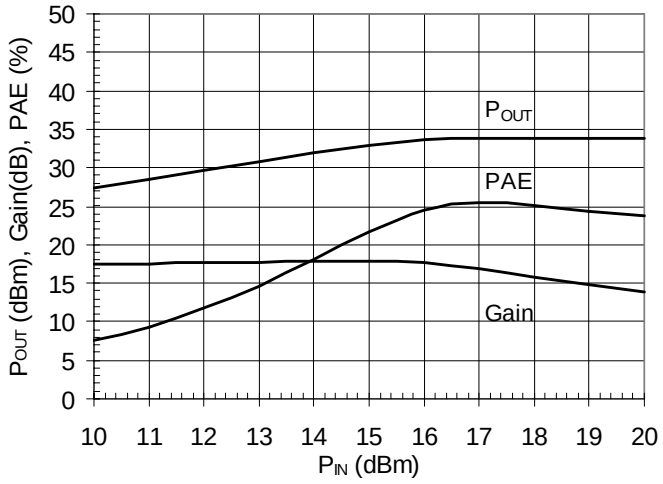


Figure 3. Output Power, Gain, and Efficiency vs. Input Power

Conditions: V_{DD} = 9V, V_{GG} = -2.2V, f = 14.0 GHz

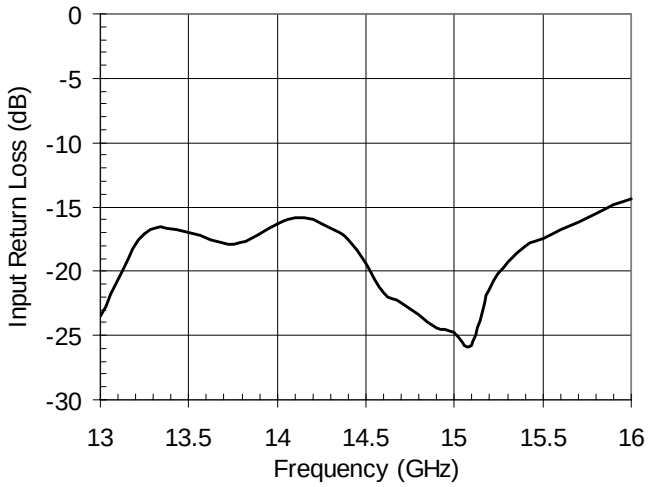


Figure 4. Input Return Loss vs. Frequency

Conditions: V_{DD} = 9V, V_{GG} = -2.2V, P_{IN} = 17 dBm

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

APPLICATION INFORMATION

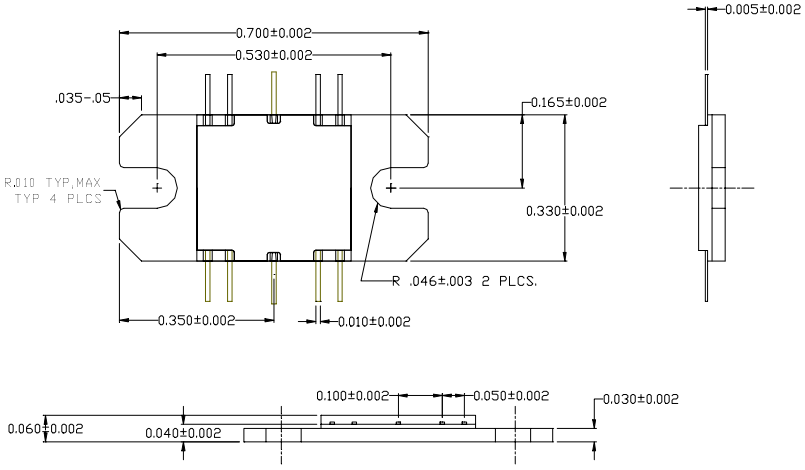


Figure 5. Package Dimensions (Not drawn to scale)

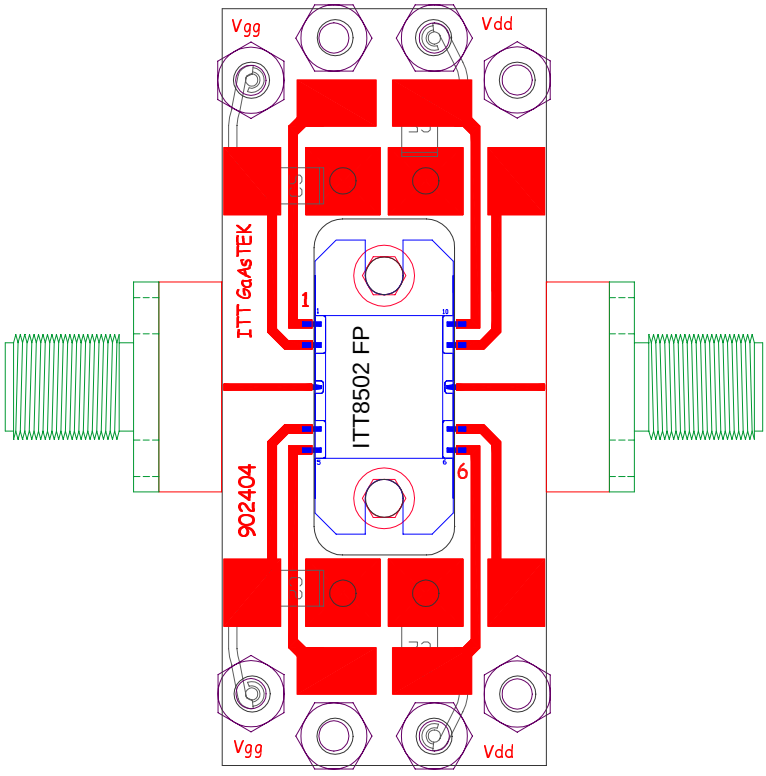


Figure 6. Demo Board diagram ('FP' pin-out)

List of components:

(4) 0.1 µF ceramic chip capacitors

Biasing:

1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.
2. Nominal bias is V_{GG}= -2.2 volts at +9.0 Volts on V_{DD}.
3. Only one V_{DD} and one V_{GG} must be connected to a power supply; each is internally connected to the other pin.

GaAsTEK
A UNIT OF ITT INDUSTRIES

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616