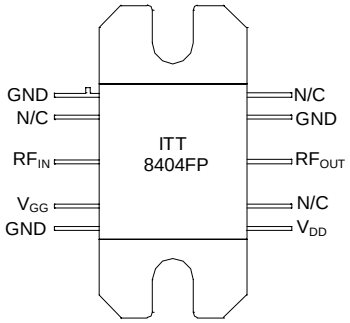
6W Power Amplifier (6.0 – 7.2 GHz)
ITT8404FP

ADVANCED INFORMATION

FEATURES

- 30% Typical Power Added Efficiency
- 16.5 dB Typical Small Signal Gain
- 43 dBm Third Order Intercept Point
- Flange mount package designed for optimum electrical and thermal performance.
- Consistent Output Power and Gain makes fixed bias possible.



FP Package
Pin Configuration

DESCRIPTION

The ITT8404 is a two stage MMIC power amplifier fabricated using GaAsTEK's Self-Aligned MSAG® MESFET Process. This product is fully matched to 50 ohms on both the input and the output.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	10	Vdc
DC Gate Supply Voltage	V_{GG}	-4	Vdc
Power Dissipation (T_{BASE} = 70 °C)	P_{DISS}	-	W
RF Input Power	P_{IN}	300	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS V_{DD}=9.0 V, V_{GG}=-2.2 V, T_A=25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	6.0	—	7.2	GHz
Output Power, saturated	P_{SAT}	—	38	—	dBm
Power Gain, saturated	G_{SAT}	—	15	—	dB
Power Added Efficiency, saturated	η_{SAT}		32		%
Output Power, P_{1dB}	P_{1dB}	—	37	—	dBm
Power Gain, P_{1dB}	G_{1dB}	—	16	—	dB
Power Added Efficiency, P_{1dB}	η_{1dB}		30		%
Third-Order Intercept Point	IP_3	–	43	–	dBm
Input Return Loss	IRL		-12		dB
Harmonics (f_o=6.25 GHz, P_{IN} = 21 dBm)	$2f_o$	–	-30	-25	dBc
Stability	All non-harmonically related outputs less than -45 dBc				

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TYPICAL CHARACTERISTICS

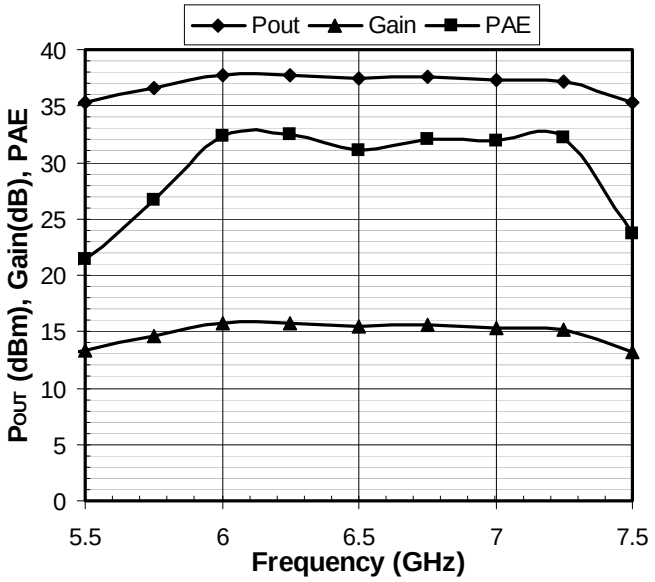

Figure 1. Saturated Output Power, Efficiency, and Input Return Loss vs. Frequency

Conditions: V_{DD} = 9V, V_{GG} varies, P_{IN} = 22 dBm

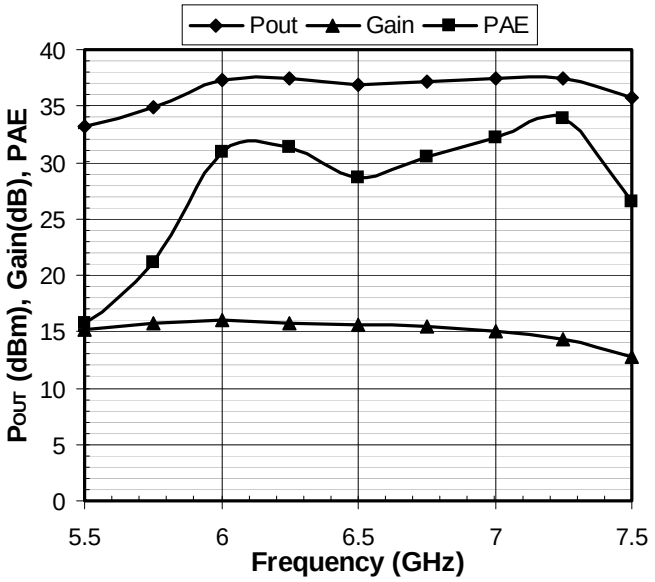

Figure 2. Output Power at P-1dB, Efficiency, and Gain vs. Frequency

Conditions: V_{DD} = 9V, V_{GG} varies, P_{IN} varies

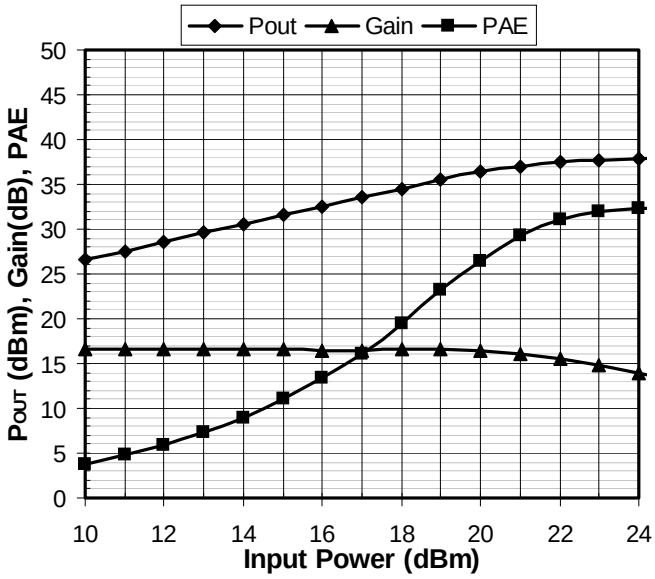

Figure 3. Output Power, Gain, and Efficiency vs. Input Power

Conditions: V_{DD} = 9V, V_{GG} varies, f = 6.5 GHz

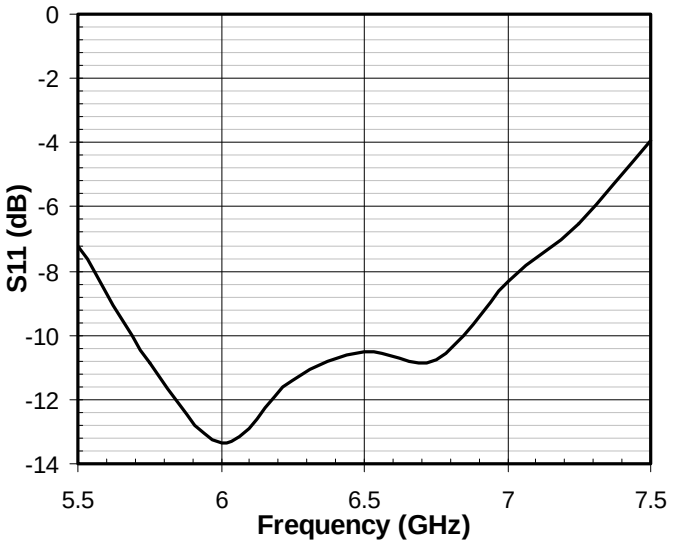

Figure 4. Input Return Loss vs. Frequency at P-1dB

Conditions: V_{DD} = 9V, V_{GG} varies, P_{IN} varies

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APPLICATION INFORMATION

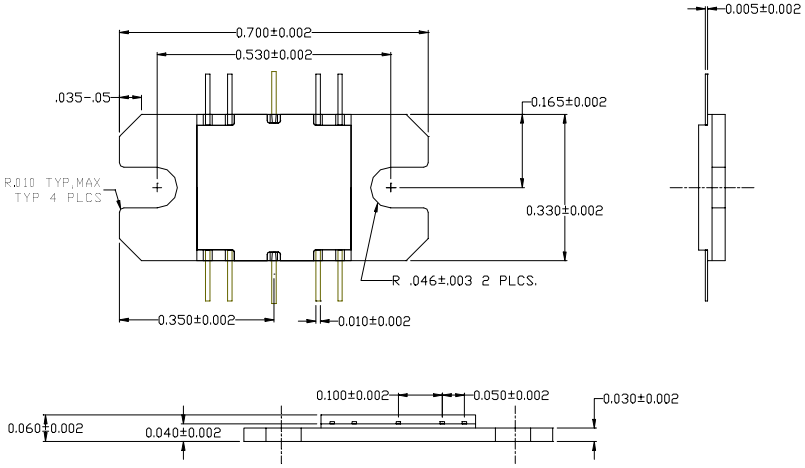

Figure 5. 'FP' Package Dimensions (Not drawn to scale)

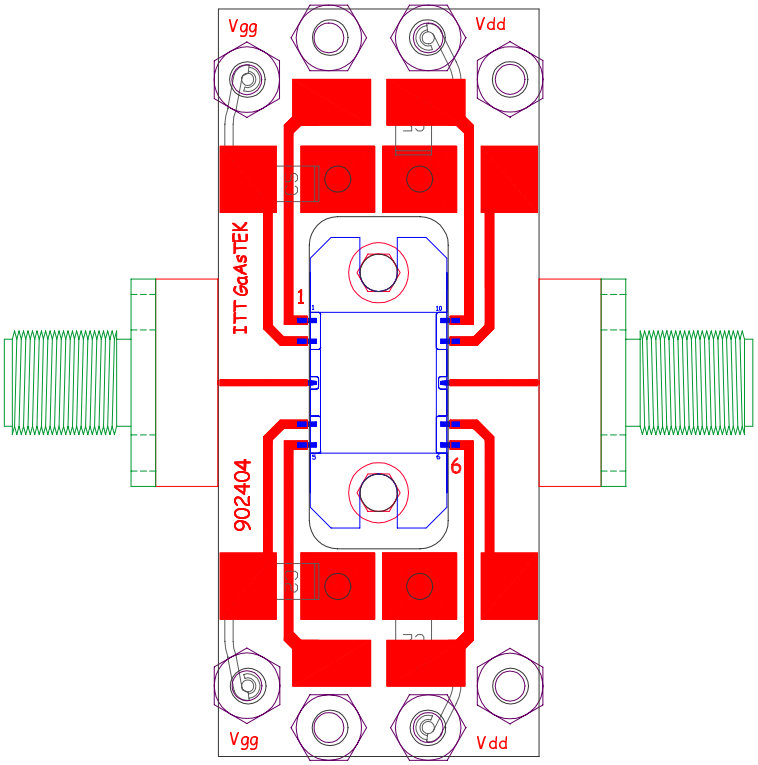

Figure 6. Demo Board diagram

List of components:

(4) 0.1 µF ceramic chip capacitors

Biasing:

1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.
2. Nominal bias is V_{GG}= -2.2 volts at +9.0 Volts on V_{DD}.
3. Only one V_{DD} and one V_{GG} must be connected to a power supply; each is internally connected to the other pin.

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