4W Power Amplifier Die (5.5 – 7.5 GHz) PRELIMINARY
ITT8403D

FEATURES

- Broadband Performance
- 20% Typical Power Added Efficiency
- High Linear Gain: 18 dB typical
- 50 Ω Input/Output Impedance
- Self-Aligned MSAG® MESFET Process

DESCRIPTION

The ITT8403D is a two stage MMIC power amplifier fabricated using GaAsTEK's mature GaAs Self-Aligned MSAG® MESFET Process. This product is fully matched to 50 ohms on both the input and the output.

MAXIMUM RATINGS T_A = 25 °C unless otherwise noted

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	12	Vdc
DC Gate Supply Voltage	V_{GG}	-4	Vdc
Power Dissipation (T_{BASE} = 70 °C)	P_{DISS}	-	W
RF Input Power	P_{IN}	500	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-40 to +85	°C

ELECTRICAL CHARACTERISTICS V_{DD} = 8.0 V, I_{DQ} = 1.2 A ($V_{GG} \approx$ -2.1V), T_A=25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	5.5	—	7.5	GHz
Output Power, Saturated (P_{IN} = 20 dBm)	P_{SAT}	—	37	—	dBm
Output Power, P_{1dB}	P_{1dB}	—	35.2	—	dBm
Power Gain, P_{1dB}	G_{1dB}	—	19.5	—	dB
Gain Flatness Over Frequency	-	—	+/- 0.5	—	dB
Power Added Efficiency, P_{1dB}	η		38		%
Drain Current at P_{1dB}	$I_{DS, 1dB}$	–	1.0	–	A
Third-Order Intercept Point	IP_3	–	45	–	dBm
Input Return Loss	IRL		-12		dB
Harmonics (f_o=6.5 GHz, P_{OUT}=34.5 dBm)	$2f_o$	–	-35	–	dBc
Gate Bias Voltage (No RF Input)	V_{GG}	–	-2.1	–	V
Gate Current	I_{GG}	–	2	5	A
Thermal Resistance (Junction to die attach)	R_{TH}	–	9.4	–	°C/W
Stability	All non-harmonically related outputs less than -45 dBc				

GaAsTEK
A UNIT OF ITT INDUSTRIES

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949
(USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

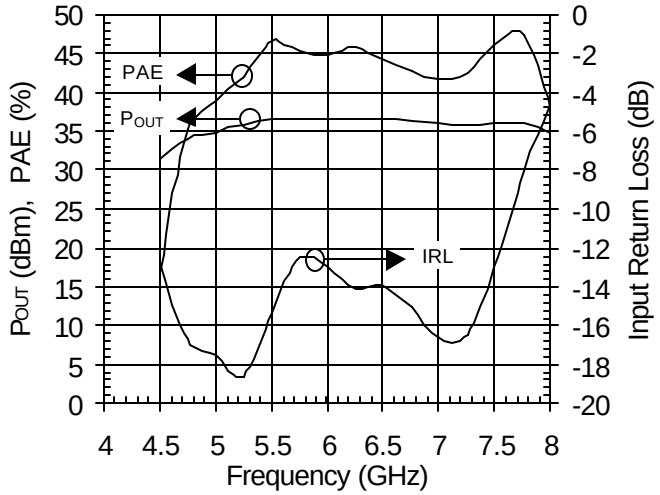


Figure 1. Saturated Output Power, Efficiency, and Input Return Loss vs. Frequency

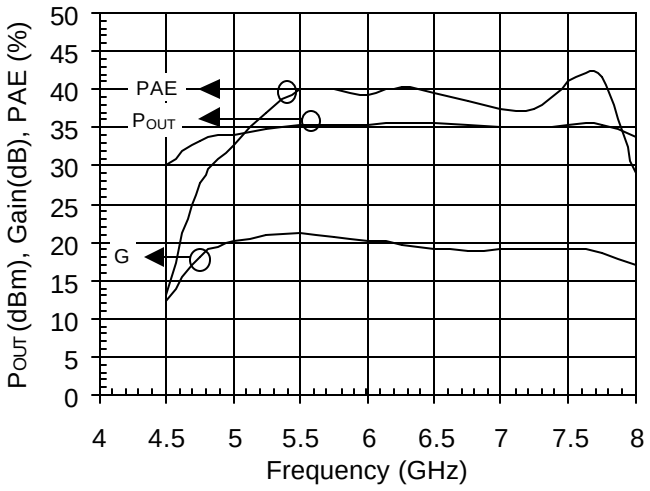


Figure 2. Output Power at P-1dB, Efficiency, and Gain vs. Frequency

Conditions for Figure 1:
V_{DD} = 8V, I_{DQ} = 1.2 A (no RF), P_{IN} = 20 dBm

Conditions for Figure 2:
V_{DD} = 8V, I_{DQ} = 1.2 A (no RF), P_{IN} varies

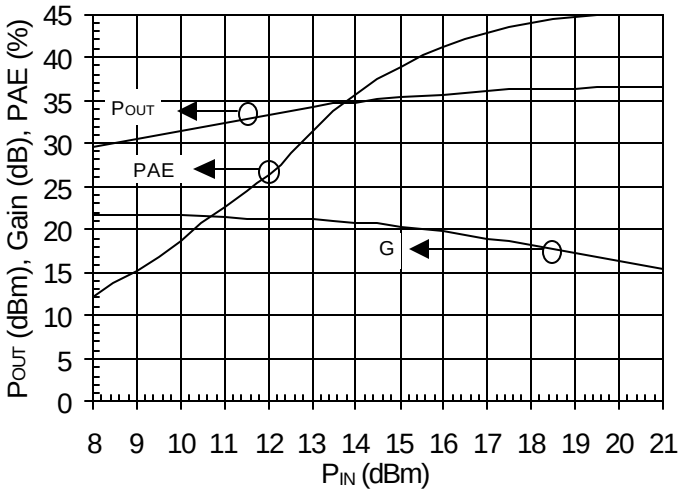


Figure 3. Output Power, Gain, and Efficiency vs. Input Power

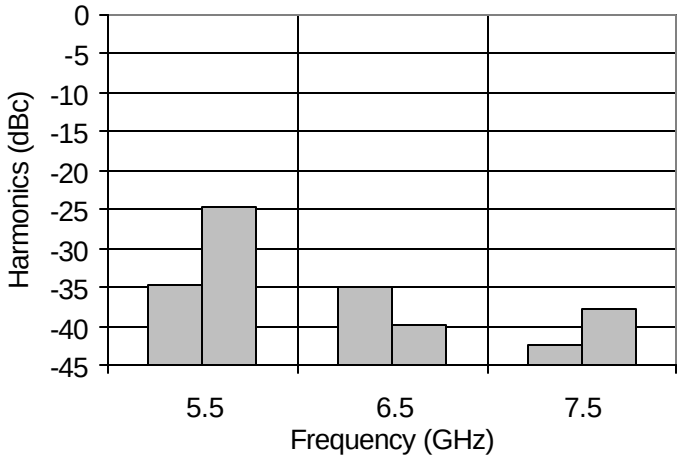


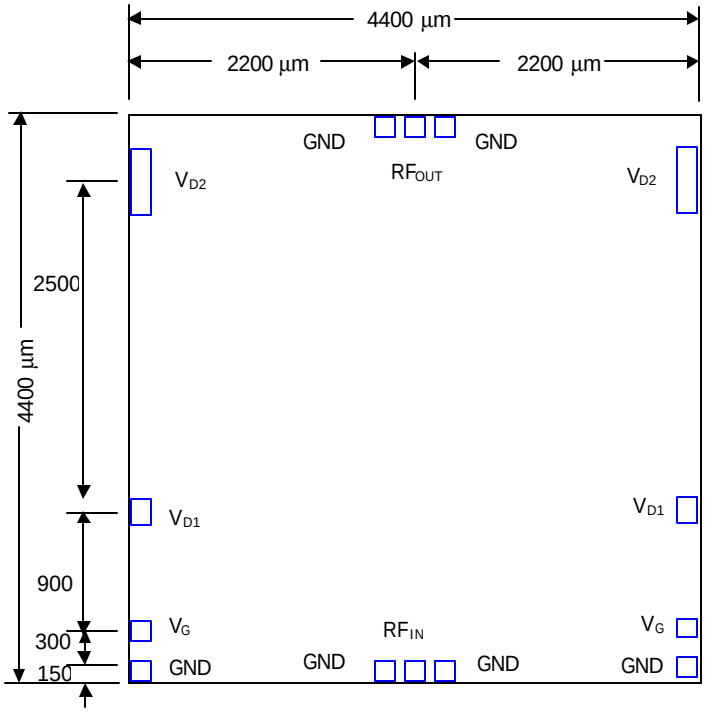
Figure 4. Second and Third Harmonics vs. Frequency

Conditions for Figure 3:
V_{DD} = 8V, I_{DQ} = 1.2 A (no RF), f = 6.0 GHz

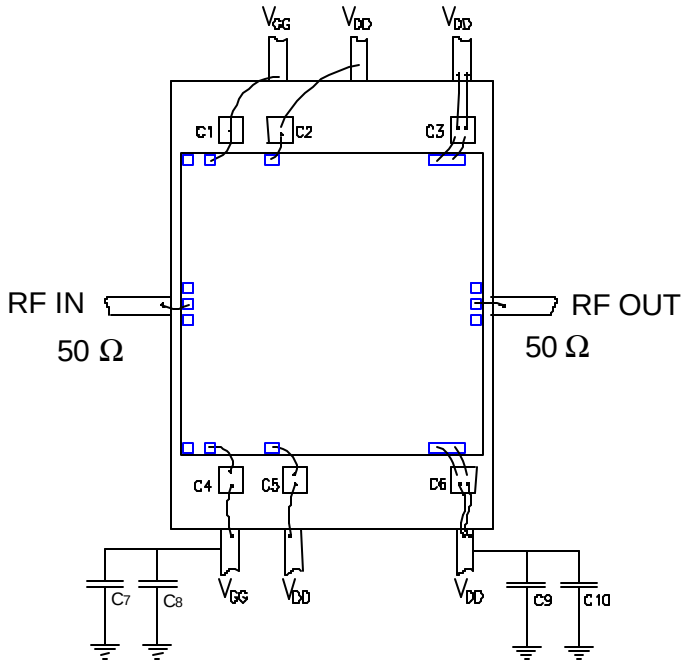
Conditions for Figure 4:
V_{DD} = 8V, I_{DQ} = 1.2 A (no RF), P_{IN} = 15 dBm

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949
(USA)
Fax: 1-540-563-8616

LAYOUT AND BONDING DIAGRAMS



Pad Sizes:
V_G: 150 X 150 microns
V_{D1}: 200 X 150 microns
V_{D2}: 500 X 150 microns



List of components:
C1 thru C6 = 100pF single layer ceramic chip capacitor
C7 = C9 = 0.1 uF ceramic chip capacitor
C8 = C10 = 5000 pF capacitor

Assembly:

Chip dimensions: 4.4mm x 4.4mm, .003" thickness.
Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.
Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing:
1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949
(USA)
Fax: 1-540-563-8616