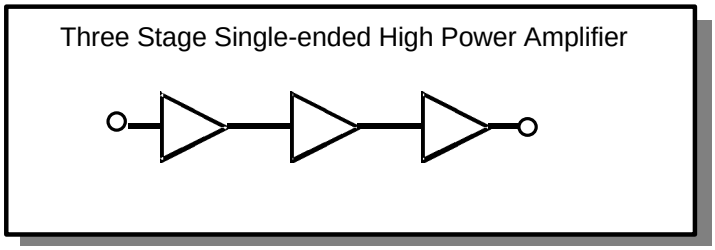
10W Power Amplifier Die (8.0 – 11.0 GHz)
ITT338509D

ADVANCED INFORMATION

FEATURES

- Broadband Performance
- 35% Typical Power Added Efficiency
- 50 Ω Input/Output Impedance
- Self-Aligned MSAG® MESFET Process



Description

The ITT338509D is a three stage MMIC power amplifier fabricated using GaAsTEK's mature GaAs Self-Aligned MSAG® MESFET Process. This product is fully matched to 50 ohms on both the input and the output.

Maximum Ratings (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	V_{DD}	12	Vdc
DC Gate Supply Voltage	V_{GG}	-4	Vdc
Power Dissipation (T_{BASE} = 70 °C)	P_{DISS}	-	W
RF Input Power	P_{IN}	500	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 10.0 V, V_{GG} = -2 V, P_{IN} = 20 dBm, T_A = 25 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	8.0	—	11.0	GHz
Output Power, saturated	P_{SAT}		40		dBm
Power Gain, saturated	G_{SAT}		20		dB
Gain Flatness Over Frequency	-		+/- 1.0		dB
Power Added Efficiency (P_{OUT}=P_{SAT})	PAE		35		%
Return Loss	S_{11}		-6		dB
Harmonics	$2f_o$, $3f_o$			-20	dBc

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TYPICAL CHARACTERISTICS (V_{DD} = 10 V, V_{GG} = -2 V, P_{IN} = 20 dBm)

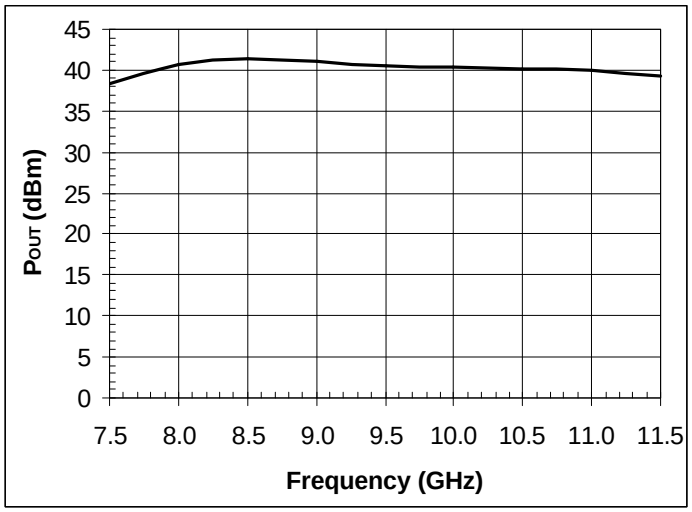

Figure 1. Output Power vs. Frequency

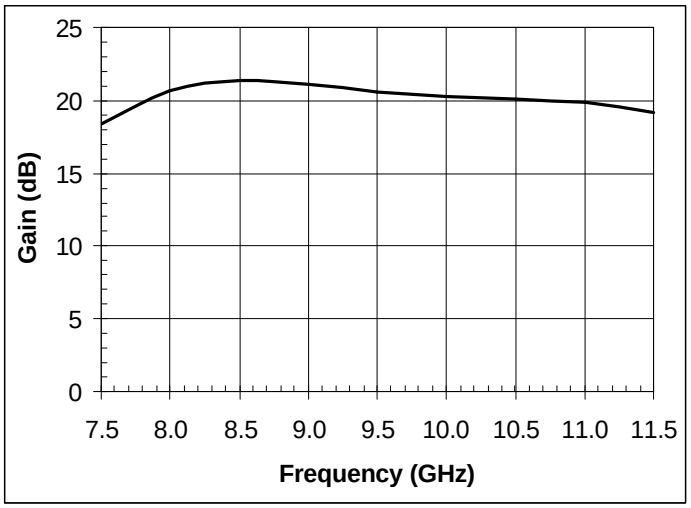

Figure 2. Gain vs. Frequency

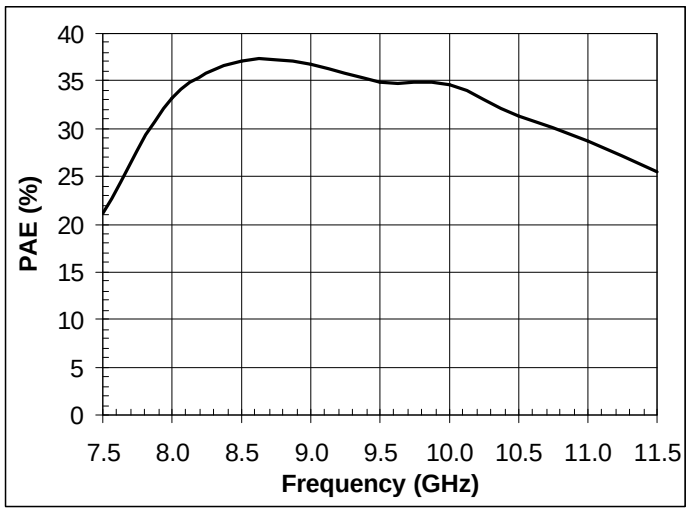

Figure 3. Power Added Efficiency vs. Frequency

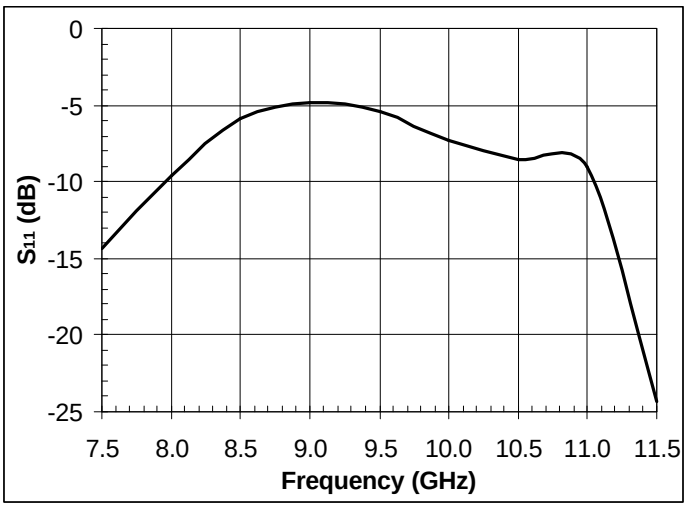

Figure 4. Input Return Loss vs. Frequency

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APPLICATION INFORMATION

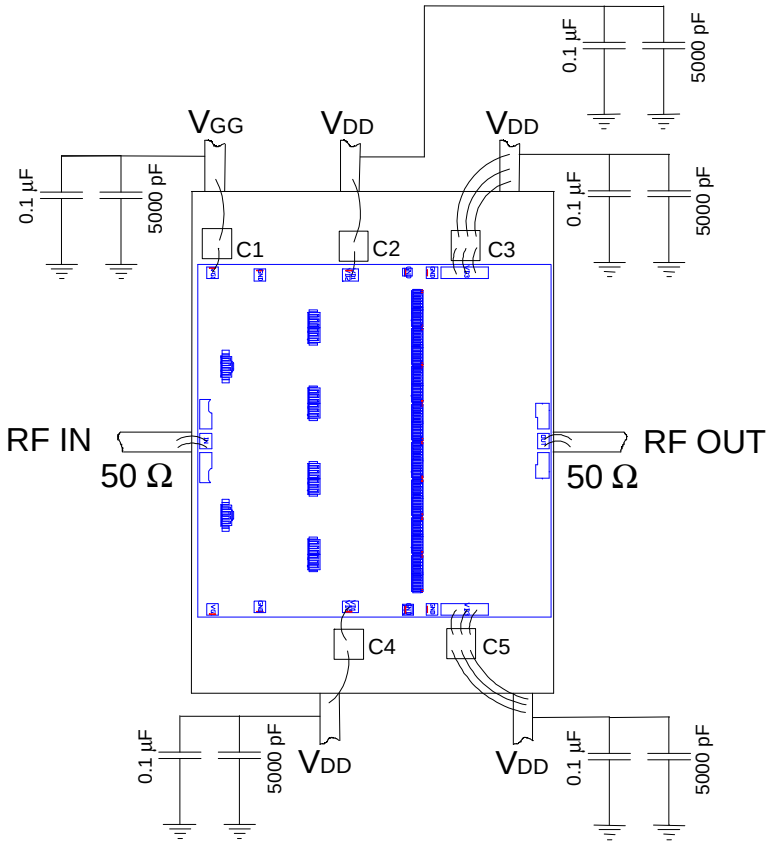

Figure 5. Recommended bonding diagram for pedestal mount

List of components:
C1 thru C5 = 100pF single layer ceramic chip capacitor

Assembly:

Chip dimensions: 4.6 mm x 4.6 mm, .003" thickness.

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing:

1. User must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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