

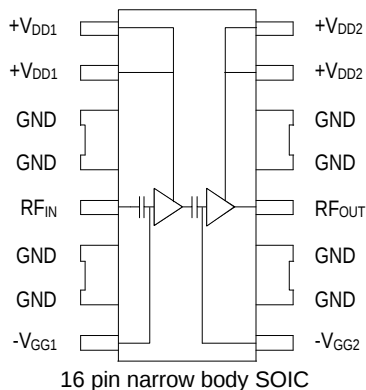
5.8V 1.2W RF Power Amplifier IC for AMPS ITT334103BD

Applications

AMPS Cellular Telephones
Cellular Digital Packet Data (CDPD)

Features

- Class AB Bias
- 800 to 875 MHz Operation
- 50 Ω Input Impedance
- Simple 2 Element Output Match
- Accommodates Battery Charging Conditions up to 8.5 Volts
- Small Size — 16 Pin Narrow Body SOIC Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process
- Guaranteed Stability and Ruggedness



Typical 5.8 Volt Performance

30.8 dBm Power Output
23.8 dB Power Gain
55% Power Added Efficiency
-35 dBc 2nd Harmonic
< -45 dBc 3rd & 4th Harmonics

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 1, 2,15,16)	V _{DD}	10	Vdc
DC Gate Bias Voltage (Pins 8, 9)	V _{GG}	-5	Vdc
RF Input Power	P _{IN}	15	mW
Junction Temperature (See maximum operating temperature chart in Fig. 11)	T _J	150	°C
Storage Temperature Range	T _{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD} = 5.8 V, P_{IN}=+7 dBm, T_S = 40 °C (See Note 1), 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range	—	824	849	MHz
Load Power (V _{GG} is adjusted for desired output power)	P _L	1.2	—	W
Power Gain (P _{OUT} = 30.8 dBm)	G _P	23.8	—	dB
Drain Current (P _{OUT} = 30.8 dBm)	I _{DD}	—	415	mA
Harmonics (P _{OUT} = 30.8 dBm)	2f ₀	—	-30	dBc
	3f ₀	—	-40	dBc
Input VSWR (P _{OUT} = 30.8 dBm), 50 Ω Ref.	—	—	2.0:1	—
Thermal Resistance (Junction of 2 nd stage FET to solder point of pin 11)	R _{TH J-S}	—	27	°C/W
Load Mismatch (V _{DD} = 8.5 V, VSWR = 10:1)	—	No Degradation in Power Output		
Stability (P _{IN} =-3 to +12 dBm, V _{DD} =0-8.5 V, 0 mW < P _{OUT} < 1.2 W, T _S =-40 to +100 °C, Load VSWR = 10:1)	—	All non-harmonically related outputs more than 60 dB below desired signal		

Note 1: T_S is the temperature measured at the soldering point of pin 11, mounted on 60 mil GETEK evaluation board in a free air condition with ambient room temperature T_A=25°C. The electrical data presented herein was taken with the evaluation board shown in Figures 1 & 12, under room temperature conditions, operating at 1.2 W of load power (V_{DD} = 5.8 V), unless otherwise specified.

Specifications Subject to Change Without Notice

900694 C, October 1998



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APPLICATION INFORMATION

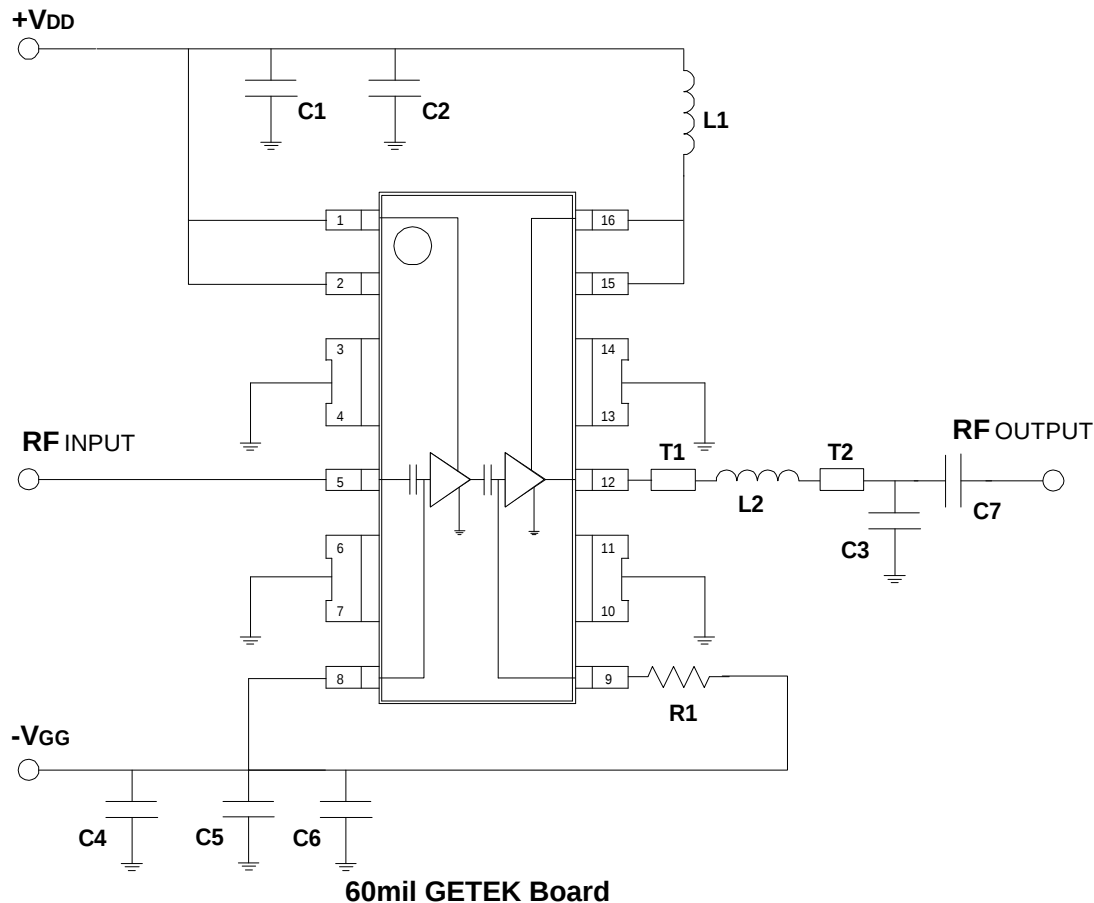


Figure 1. Evaluation Board Schematic

List of components:

- C1 = C4 = C5 = 4700 pF Kemet multilayer ceramic chip capacitor (C0805C472K5RAC)
- C2 = C6 = 0.1 μ F Kemet multilayer ceramic chip capacitor (C1206C104K5RAC)
- C3 = 5.1 pF DLI multilayer ceramic chip capacitor (C11AH5R1C5TXL)
- C7 = 100 pF DLI multilayer ceramic chip capacitor (DC Block; C11AH101K5TXL)
- L1 = 56 nH Coilcraft chip inductor (1008CS.560XKBB)
- L2 = 2.7 nH Toko chip inductor (TKS2362CTND)
- R1 = 300 Ω chip resistor
- T1 = T2 = 0.1" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)



Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 12.

Biasing: Gate bias voltage (V_{GG}) must be applied prior to RF input power and drain bias voltage (V_{DD}). Reverse the sequence when turning the part off — remove the RF input and drain bias before removing gate bias.

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TYPICAL CHARACTERISTICS

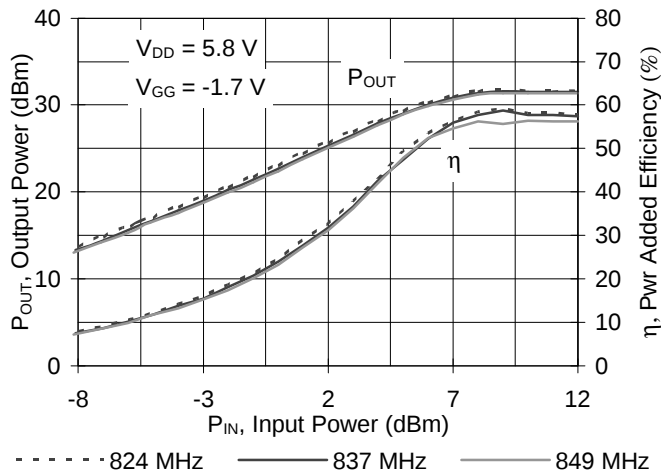


Figure 2. Output power and efficiency vs. input power

Conditions for Figure 2:

Gate bias (V_{GG}) is set for 1.2 W of output power when $P_{IN} = 7$ dBm.

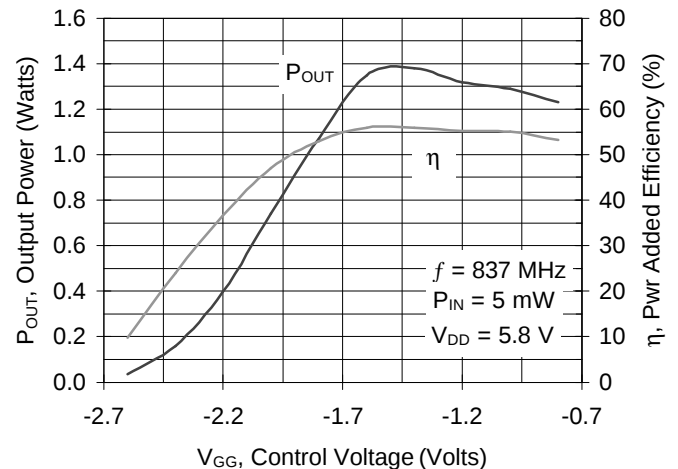


Figure 3. Output power and efficiency vs. control voltage

Conditions for Figure 3:

While keeping supply voltage constant ($V_{DD} = 5.8$ V), the output power is controlled by adjusting DC gate bias (V_{GG}).

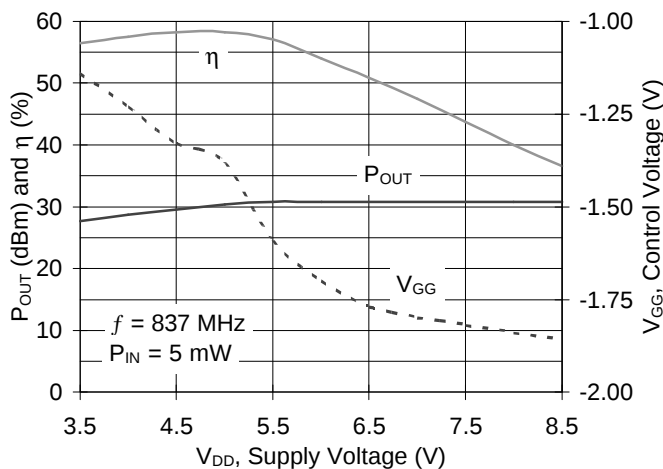


Figure 4. Output power, efficiency, and control voltage vs. supply voltage

Conditions for Figure 4:

Control voltage (V_{GG}) is adjusted for each supply voltage in an attempt to maintain 1.2 W output power.

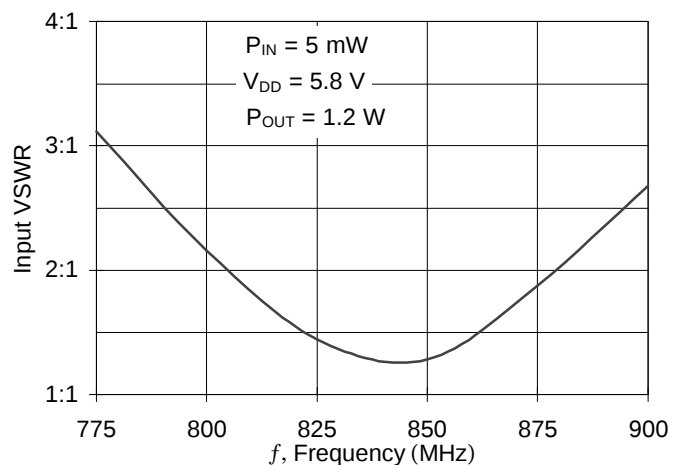


Figure 5. Input VSWR vs. frequency

Conditions for Figure 5:

Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

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TYPICAL CHARACTERISTICS

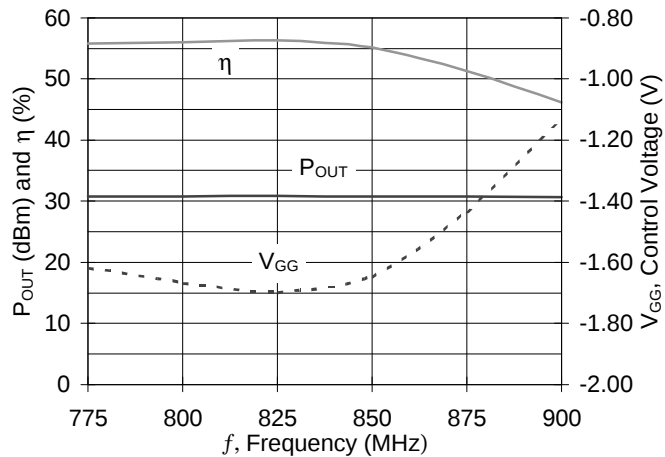


Figure 6. Output power, efficiency, and control voltage vs. frequency

Conditions for Figure 6:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

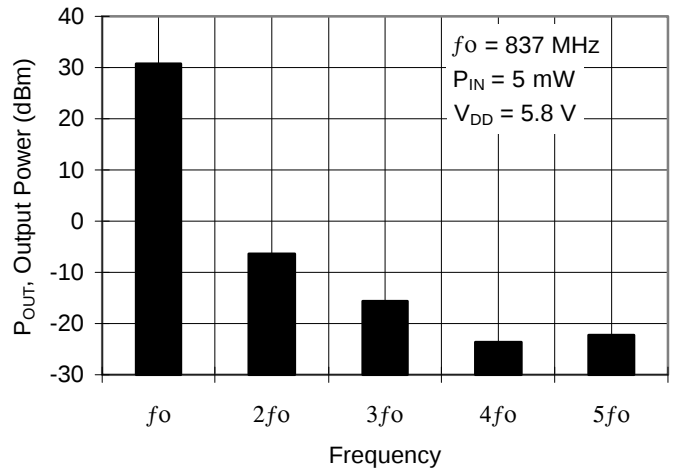


Figure 7. Harmonics

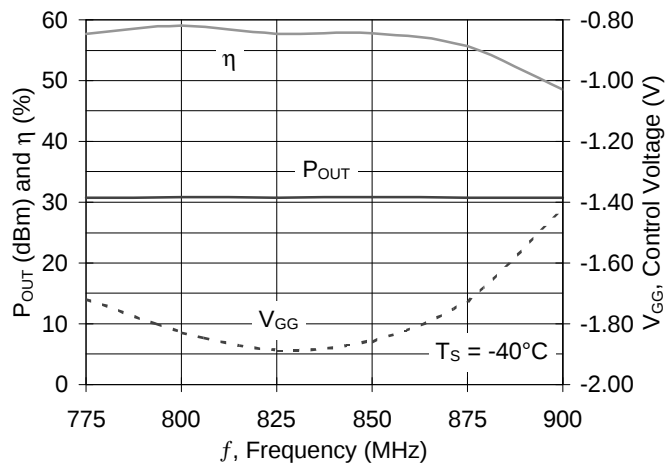


Figure 8. Output power, efficiency, and control voltage vs. frequency for $T_s = -40^\circ\text{C}$

Conditions for Figure 8:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

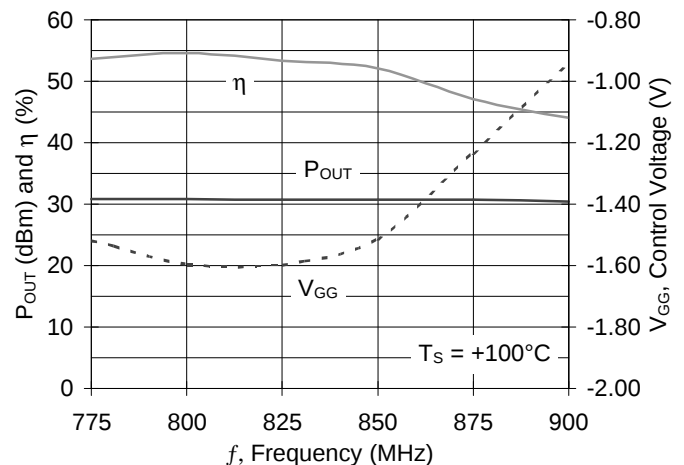


Figure 9. Output power, efficiency, and control voltage vs. frequency for $T_s = +100^\circ\text{C}$

Conditions for Figure 9:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

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TYPICAL CHARACTERISTICS

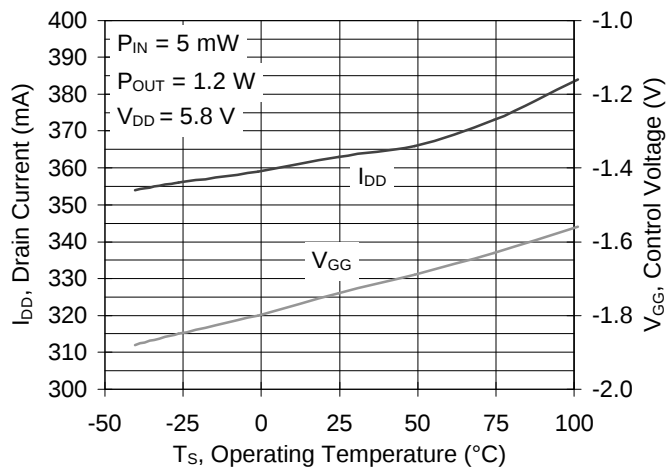


Figure 10. Drain current and control voltage vs. temperature

Conditions for Figure 10:

Control voltage is adjusted for each temperature to maintain 1.2 W output power. Data was taken at $f = 825 \text{ MHz}$.

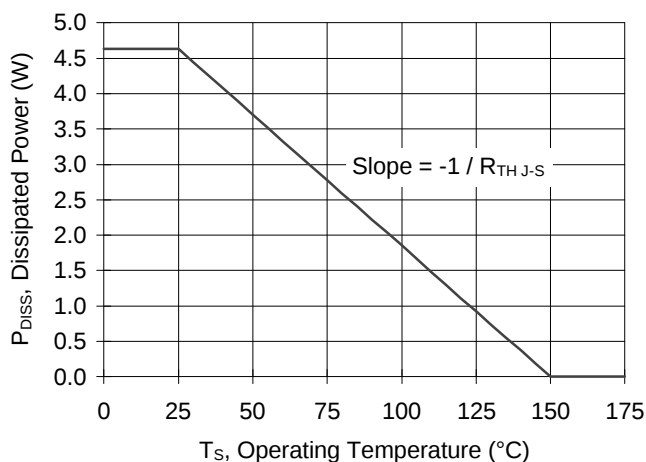


Figure 11. Maximum operating temperature chart

Conditions for Figure 11:

- $P_{DISS} = I_{DD2} \cdot V_{DD} - P_{OUT}$, which refers to the dissipated power in the hottest area of the IC (Stage 2 FET). Stage 1 power dissipation and Stage 2 input power have negligible effect on IC maximum temperature located in Stage 2.

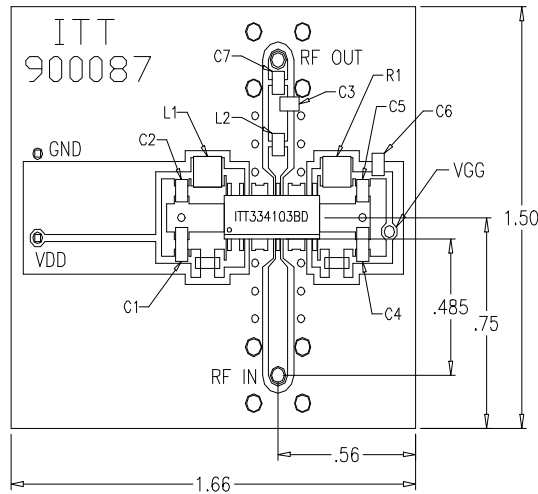
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- I_{DD2} is typically 90% of I_{DD} .

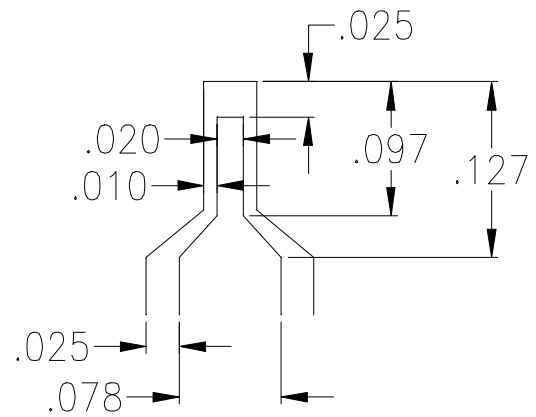


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MECHANICAL DATA



Top view



50Ω lead transition

Figure 12. Component layout and printed circuit drawing for evaluation board

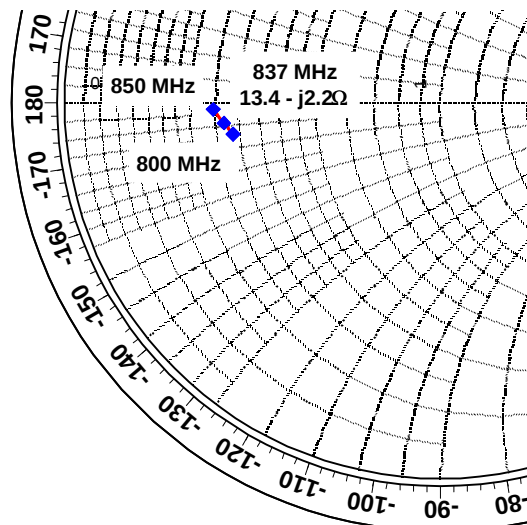


Figure 13. Output match impedance (as seen from pin 12)