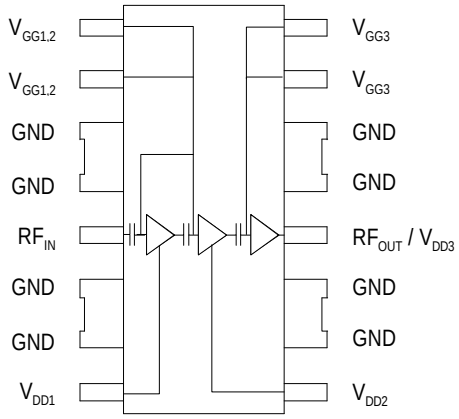
4.8V 3.0W RF Power Amplifier IC for GSM — PRELIMINARY
ITT3107BD

Applications

GSM Cellular Telephones
Wireless Modems
900 MHz ISM



16 pin narrow body SOIC

Features

- Class AB Bias
- 825 to 975 MHz Operation
- Single Element Output Match
- Small Size — 16 Pin Narrow Body SOIC Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process
- Guaranteed Stability and Ruggedness

Typical 4.8 Volt Performance

34.8 dBm Power Output
34.8 dB Power Gain
45% Power Added Efficiency
All Harmonics < -40 dBc

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 8, 9, 12)	V_{DD}	10	Vdc
DC Gate Bias Voltage (Pins 1, 2, 15, 16)	V_{GG}	-5	Vdc
RF Input Power	P_{IN}	10	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD}=4.8 V, P_{IN}=0 dBm, T_S=40 °C (Note 1), Input and output externally matched to 50 Ω System.

Characteristic	Symbol	Typical	Unit
Frequency Range	f	880 to 915	MHz
Output Power (V_{GG} adjusted for desired output power)	P_{OUT}	3.0	W
Power Gain (P_{OUT} = 34.8 dBm)	G_P	34.8	dB
Power Added Efficiency (P_{OUT} = 34.8 dBm)	η	45	%
Harmonics (P_{OUT} = 34.8 dBm)	$2f_o$ $3f_o$	–47 –42	dBc dBc
Input VSWR (P_{OUT} = 34.8 dBm), 50 Ω Ref.	—	1.3:1	—
Thermal Resistance (Junction of 3rd stage FET to solder point of pin 11)	$R_{TH\ J\text{-}S}$	18	°C/W
Load Mismatch (V_{DD} = 7.5V, VSWR = 10:1, P_{IN} = +3 dBm)	—	No Degradation in Power Output	
Stability (P_{IN} = -3 to +3 dBm, V_{DD} = 0 to 7.5 V, P_{OUT} < 34.8 dBm, T_S = -40 to +100 °C, Load VSWR = 10:1)	—	All non-harmonically related outputs more than 70 dB below desired signal	

Note 1: T_S is the temperature measured at the soldering point of pin 11, mounted on 60 mil GETEK evaluation board in a free air condition with ambient room temperature T_A=25 °C. The electrical data presented herein was taken with the evaluation board shown in Figures 1 and 9, under room temperature conditions and pulsed according to the GSM system specification.

GaAsTEK
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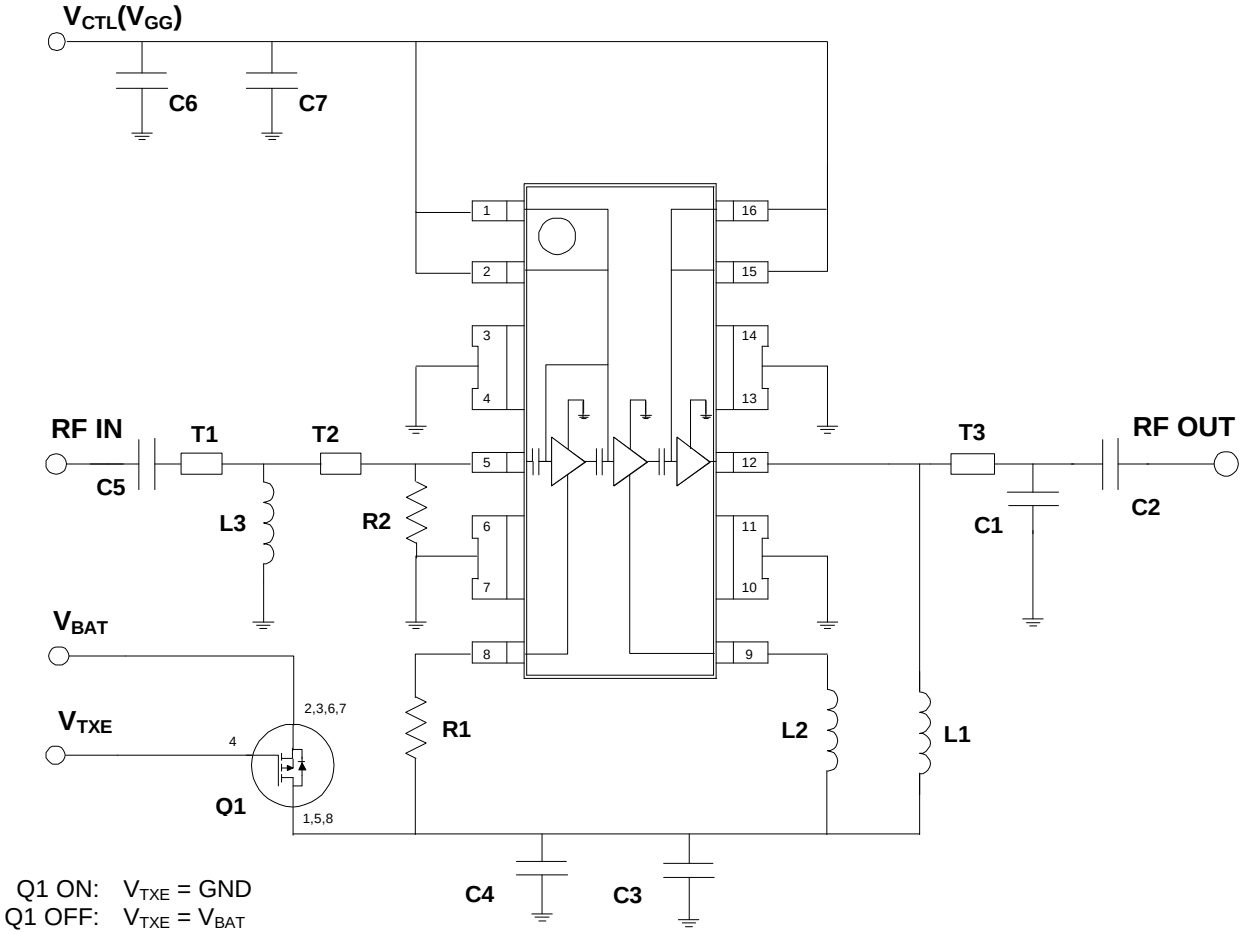
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

APPLICATION INFORMATION



60mil GETEK Board

Figure 1. Evaluation Board Schematic

List of components:

C1 = 9.1 pF DLI multilayer ceramic chip capacitor (C11AH9R1B5TXL)
C2 = 100 pF DLI multilayer ceramic chip capacitor (C11AH101K5TXL)
C3 = C7 = 4700 pF Kemet multilayer ceramic chip capacitor (C0805C472K5RAC)
C4 = C6 = 0.1 µF Kemet multilayer ceramic chip capacitor (C1206C104K5RAC)
C5 = 1.5 pF DLI multilayer ceramic chip capacitor (C11AH1R5B5TXL)
L1 = L2 = 39 nH Coilcraft chip inductor (1008CS.390XMBB)
L3 = 6.8 nH Coilcraft chip inductor (0805CS.060XMBB)
R1 = 10 Ω Chip Resistor
R2 = 300 Ω Chip Resistor
T1 = 0.13" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T2 = 0.14" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T3 = 0.14" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
Q1 = PMOSFET Switch (Siliconix Si6433DQ)

Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 9.

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Biasing: Gate bias voltage (V_{GG}) must be applied prior to RF input power and drain bias voltage (V_{TXE}=0). Reverse the sequence when turning the part off — remove the RF input and disable drain bias (V_{TXE}=V_{BAT}) before removing gate bias.

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TYPICAL CHARACTERISTICS

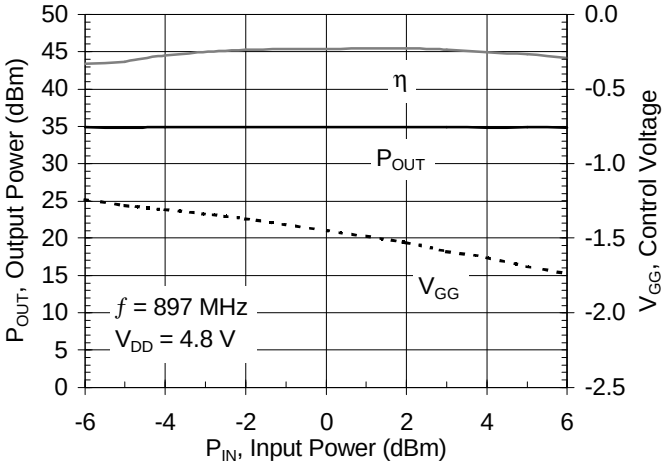

Figure 2. Output Power, Efficiency and Control Voltage vs. Input Power

Conditions for Figure 2: Control voltage (V_{GG}) is adjusted at each input power level to maintain 3.0 W output power.

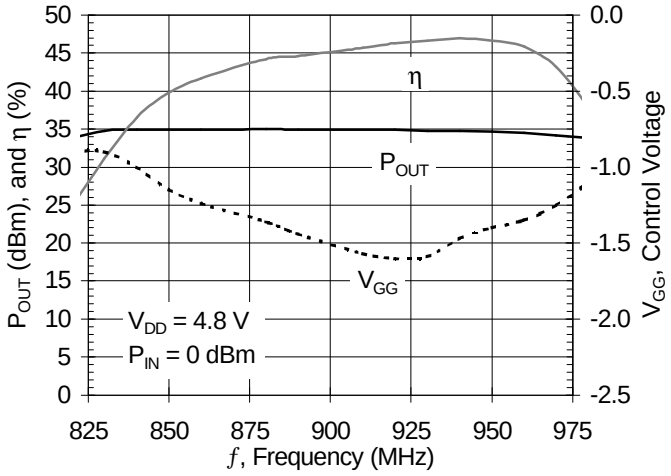

Figure 3. Output Power, Efficiency and Control Voltage vs. Frequency

Conditions for Figure 3: Control voltage (V_{GG}) is adjusted at each frequency to maintain 3.0 W output power.

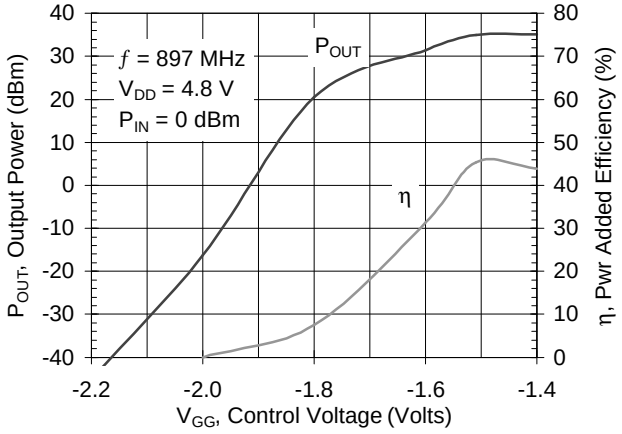

Figure 4. Output Power and Efficiency vs. Control Voltage

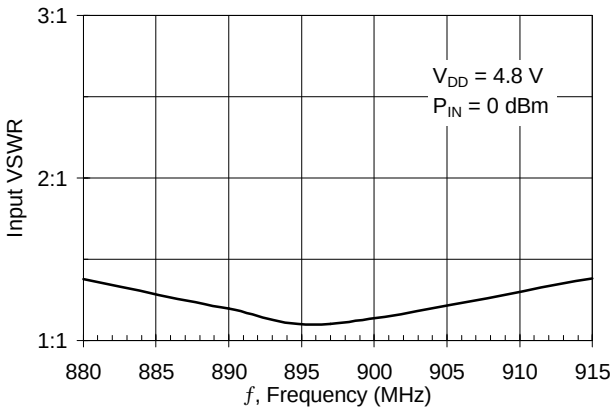

Figure 5. Input VSWR vs. Frequency

Conditions for Figure 5: Control voltage (V_{GG}) is adjusted at each frequency to maintain 3.0 W output power.

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Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

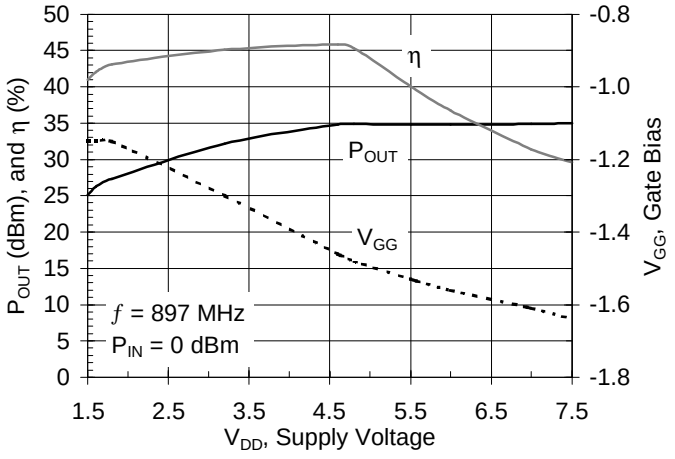

Figure 6. Output Power, Efficiency and Control Voltage vs. Supply Voltage

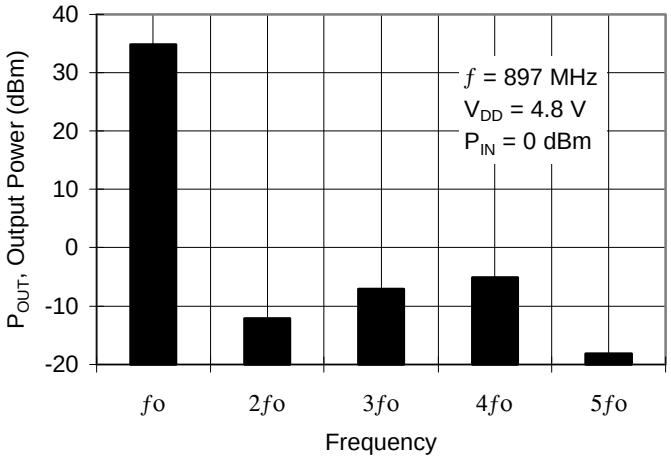

Figure 7. Harmonics

Conditions for Figure 6: Control Voltage (V_{GG}) is adjusted at each supply voltage to maintain 3.0 W output power.

MECHANICAL DATA

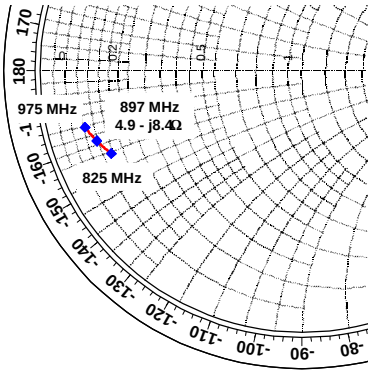

Figure 8. Output match impedance (as seen from pin 12)

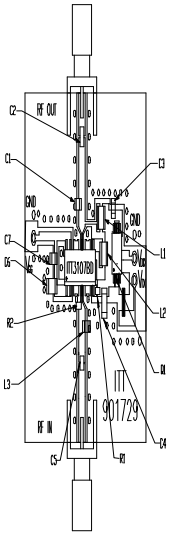

Figure 9. Component layout and printed circuit drawing for evaluation board (top view)

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