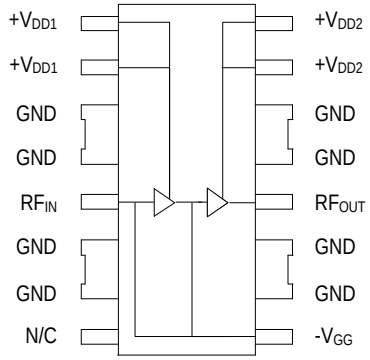
3.6V 1.1W RF Power Amplifier IC for N-PCS/ISM900 PRELIMINARY
ITT2106BD

Applications

Two-Way Paging
Wireless Modems
Cordless Telephones
Telemetry
900 MHz ISM

Features

- Class AB Bias
- 800 to 1000 MHz Operation
- Single Element Input Match
- Single Element Output Match
- Small Size — 16 Pin Narrow Body SOIC Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process
- Guaranteed Stability and Ruggedness



16 pin narrow body SOIC

Typical 3.6 Volt Performance

30.4 dBm Power Output
23.4 dB Power Gain
54% Power Added Efficiency
All Harmonics < -30 dBc

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 1, 2, 15, 16)	V_{DD}	10	Vdc
DC Gate Bias Voltage (Pin 9)	V_{GG}	-5	Vdc
RF Input Power	P_{IN}	15	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD}=3.6 V, P_{IN}=7 dBm, T_S=50 °C (Note 1), Output externally matched to 50 Ω System.

Characteristic	Symbol	Typical	Unit
Frequency Range	f	900 to 942	MHz
Output Power (P_{IN} = 7 dBm, V_{GG} adjusted for desired output power)	P_{OUT}	1.1	W
Power Gain (P_{OUT} = 30.4 dBm)	G_P	23.4	dB
Power Added Efficiency	η	54	%
Harmonics (P_{OUT} = 30.4 dBm)	$2f_o$ $3f_o$	–38 –31	dBc dBc
Input VSWR (P_{OUT} = 30.4 dBm), 50 Ω Ref.	—	1.3:1	—
Thermal Resistance (Junction of 2nd stage FET to solder point of pin 11)	$R_{TH\ J\text{-}S}$	24	°C/W
Load Mismatch (V_{DD} = 5V, VSWR = 10:1,)	—	No Degradation in Power Output	
Stability (P_{IN} =-3 to +10 dBm, V_{DD} = 0-5 V, 0 mW < P_{OUT}< 1.1 W, T_S = -40 to +100 °C, Load VSWR = 10:1)	—	All non-harmonically related outputs more than 60 dB below desired signal	

Note 1: T_S is the temperature measured at the soldering point of pin 11, mounted on 60 mil GETEK evaluation board in a free air condition with ambient room temperature T_A=25 °C. The electrical data presented herein was taken with the evaluation board shown in Figures 1 and 6, under room temperature conditions and CW operation, unless otherwise specified.

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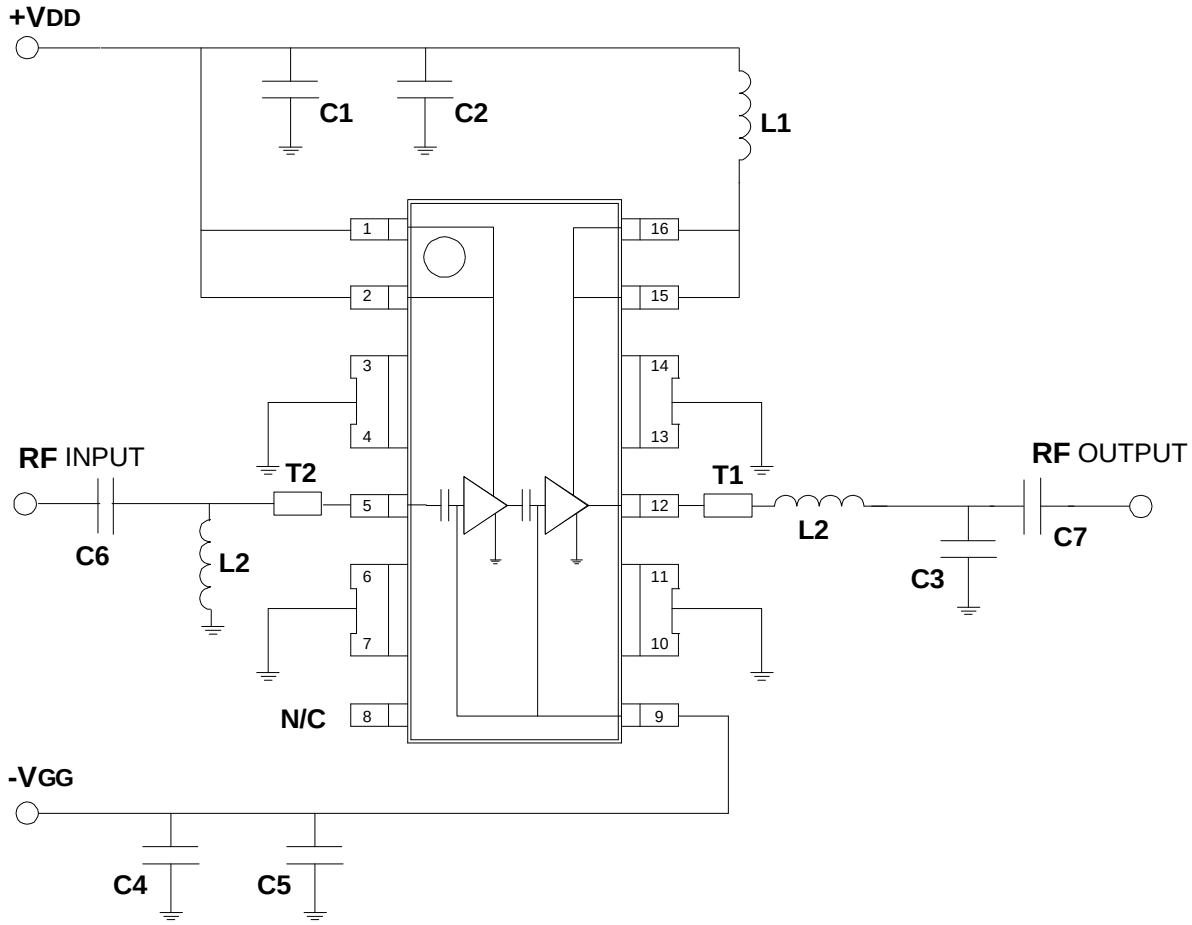
APPLICATION INFORMATION



60mil GETEK Board

Figure 1. Evaluation Board Schematic

List of components:

C1 = C4 = 0.1 µF Kemet multilayer ceramic chip capacitor (C1206C104K5RAC)
C2 = C5 = 4700 pF Kemet multilayer ceramic chip capacitor (C0805C472K5RAC)
C3 = 8.2 pF DLI multilayer ceramic chip capacitor (C11AH7R5B5TXL)
C6 = C7 = 100 pF DLI multilayer ceramic chip capacitor (DC Block; C11AH101K5TXL)
L1 = 39 nH Coilcraft chip inductor (1008CS.390XMBB)
L2 = 8.2 nH Coilcraft chip inductor (1008CT.080XKBB)
R1 = 100 Ω
T1 = 0.14" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T2 = 0.16" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)

Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 6.

Biasing:Gate bias voltage (V_{GG}) must be applied prior to RF input power and drain bias voltage (V_{DD}). Reverse the sequence when turning the part off — remove the RF input and drain bias before removing gate bias.

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TYPICAL CHARACTERISTICS

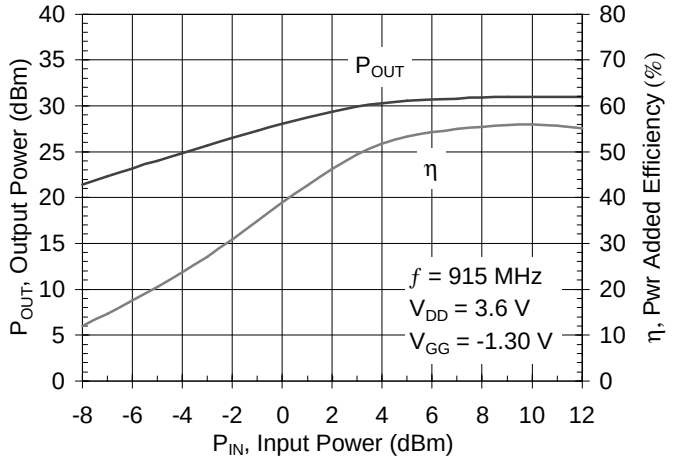

Figure 2. Output power and efficiency vs. input power for a fixed gate bias

Conditions for Figure 2:
Gate bias (V_{GG}) is set for 1.1 W of output power when P_{IN} = 7 dBm.

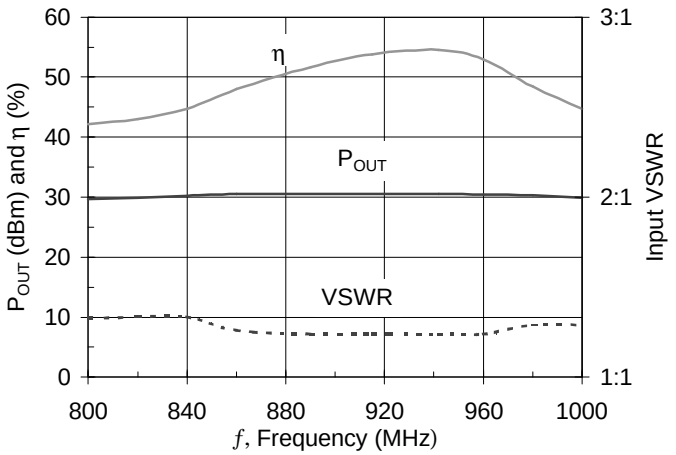

Figure 3. Output power, efficiency and input VSWR vs. frequency

Conditions for Figure 3:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.1 W output power. V_{DD} = 3.6V, P_{IN} = 7 dBm.

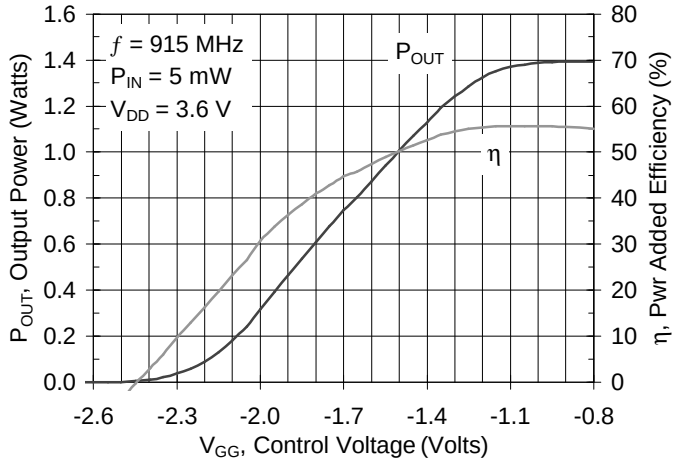

Figure 4. Output power and efficiency vs. control voltage

Conditions for Figure 4:
While keeping supply voltage constant (V_{DD} = 3.6 V), the output power is controlled by adjusting DC gate bias (V_{GG}).

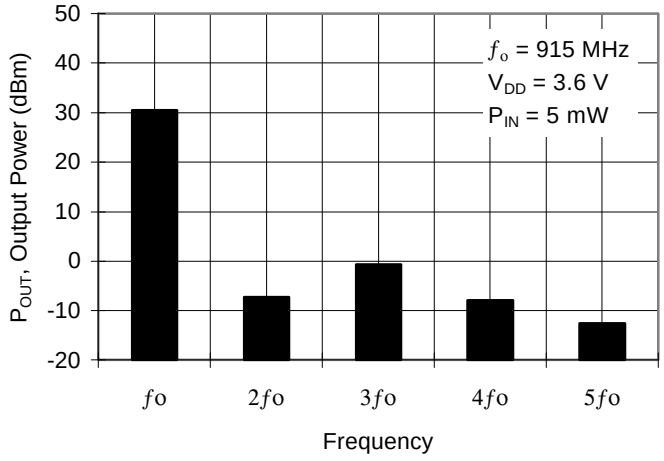

Figure 5. Harmonics

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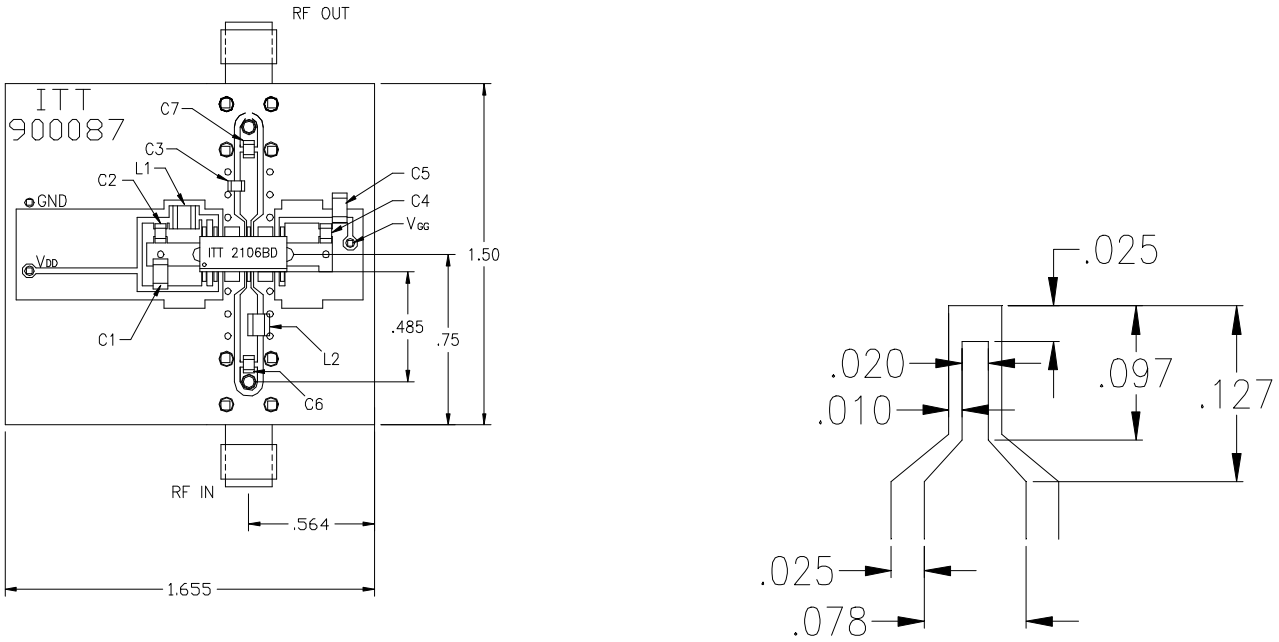
MECHANICAL DATA



Top view **50Ω lead transition**

Figure 6. Component layout and printed circuit drawing for evaluation board

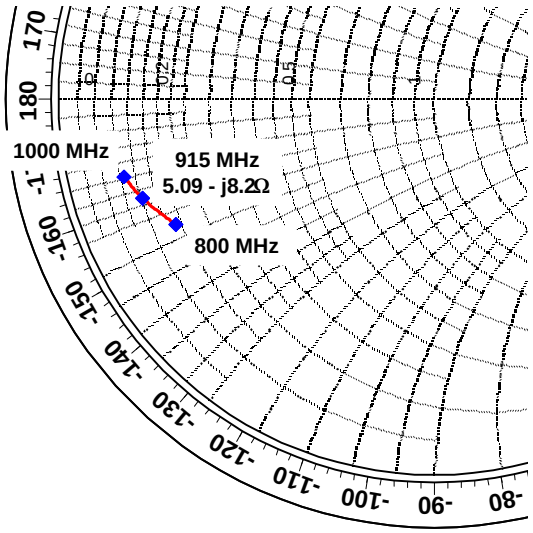


Figure 7. Output match impedance (as seen from pin 12)

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