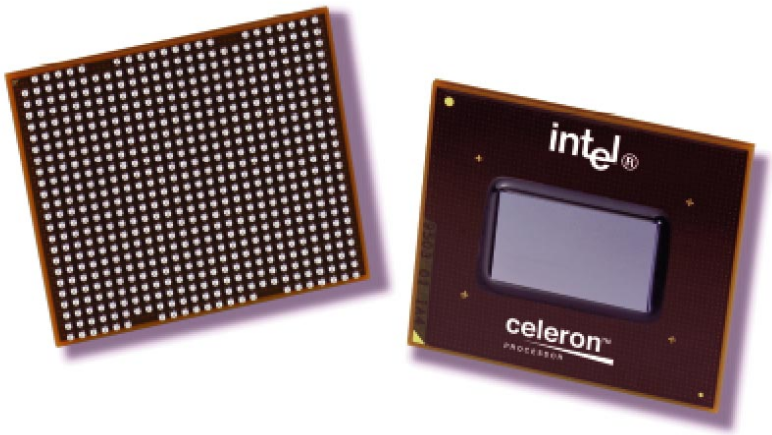
Intel® Celeron® Processor – Low Power/Ultra Low Power

300 MHz (ULP) and 400A MHz (LP) Processor in a BGA2 Package

Datasheet

Product Features

- 300/100 MHz processor core/bus speed at 1.1 V (Ultra Low Power)
- 400A/100 MHz processor core/bus speed at 1.35 V (Low Power)
- Supports the Intel Architecture with Dynamic Execution
- On-die primary 16-Kbyte instruction cache and 16-Kbyte write-back data cache
- On-die second level cache (128-Kbyte)
- Integrated GTL+ termination
- On-die thermal diode
- Integrated math co-processor
- Power Management Features
  - —Quick Start and Deep Sleep modes provide low-power dissipation
- Fully compatible with previous Intel microprocessors
  - —Binary compatible with all applications
  - —Support for MMX™ technology
  - —Support for Streaming SIMD Extensions
- BGA2 packaging technology
  - —Supports thin form factor designs
  - —Exposed die enables efficient heat dissipation



Document Number: 273509-001
October 2001

Contents

Figures

Tables

Revision History

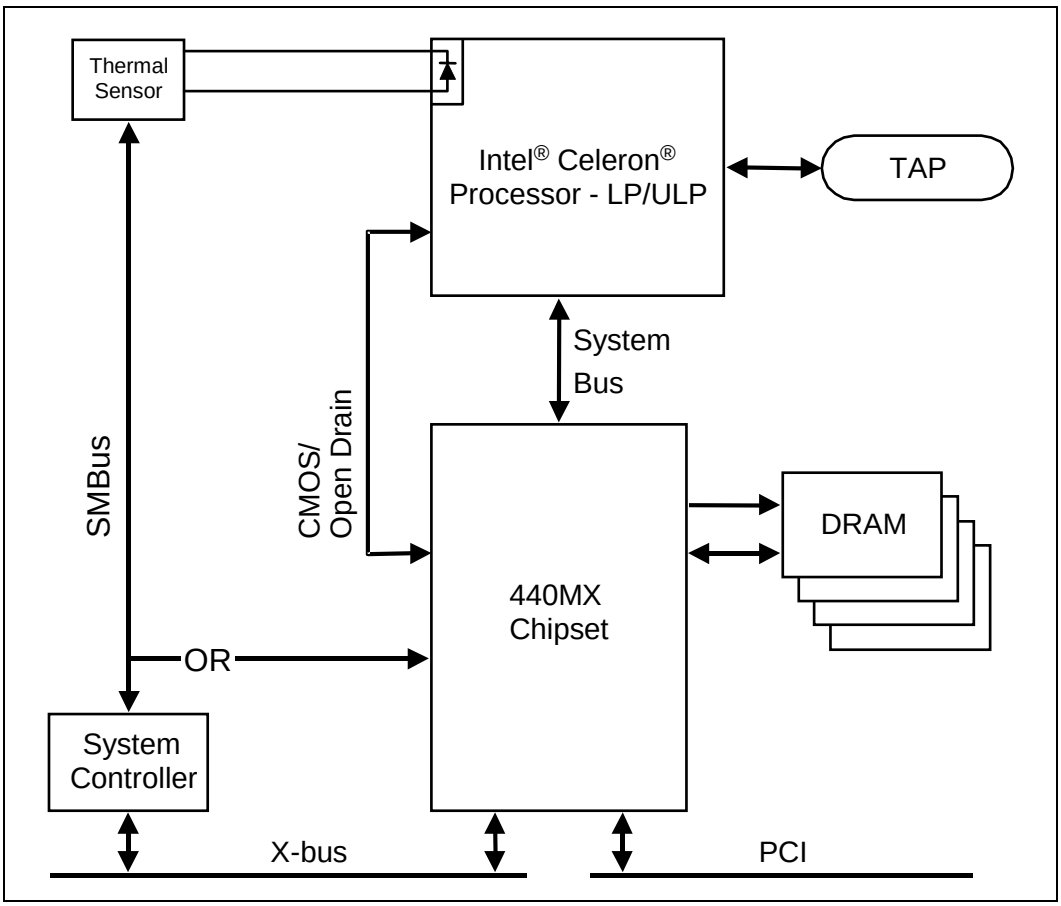
Date	Revision	Description
October, 2001	-001	First release of this document.

1.0 Introduction

The Intel® Celeron® Processor – Low Power is offered at 400A MHz with a system bus speed of 100 MHz. The Intel® Celeron® Processor – Ultra Low Power is offered at 300 MHz with a system bus speed of 100 MHz. Unless otherwise noted, the specifications provided in this document apply to both processors.

The integrated L2 cache is designed to help improve performance, and it complements the system bus by providing critical data faster and reducing total system power consumption. The processor's 64-bit wide Gunning Transceiver Logic (GTL+) system bus is compatible with the 440MX Chipset and provides a glue-less, point-to-point interface for an I/O bridge/memory controller. Figure 1 shows the various parts of a Celeron processor-based system and how the processor connects to them.

Figure 1. Signal Groups of an Intel® Celeron® Processor – LP/ULP System



1.1 Overview

- Performance features
  - — Supports the Intel Architecture with Dynamic Execution
  - — Supports Intel MMX™ technology
  - — Supports streaming SIMD extensions for enhanced video, sound, and 3D performance
  - — Integrated Intel Floating Point Unit compatible with the IEEE 754 standard
- On-die primary (L1) instruction and data caches
  - — 4-way set associative, 32-byte line size, 1 line per sector
  - — 16-Kbyte instruction cache and 16-Kbyte write-back data cache
  - — Cacheable range controlled by processor programmable registers
- On-die second level (L2) cache
  - — 4-way set associative, 32-byte line size, 1 line per sector
  - — Operates at full core speed
  - — 128-Kbyte, ECC protected cache data array
- GTL+ system bus interface
  - — 64-bit data bus, 100-MHz operation
  - — Uniprocessor, two loads only (processor and I/O bridge/memory controller)
  - — Integrated termination
- Processor clock control
  - — Quick Start for low power, low exit latency clock “throttling”
  - — Deep Sleep mode for lower power dissipation
- Thermal diode for measuring processor temperature

1.2 Terminology

In this document a “#” symbol following a signal name indicates that the signal is active low. This means that when the signal is asserted (based on the name of the signal) it is in an electrical low state. Otherwise, signals are driven in an electrical high state when they are asserted. In state machine diagrams, a signal name in a condition indicates the condition of that signal being asserted. If the signal name is preceded by a “!” symbol, then it indicates the condition of that signal not being asserted. For example, the condition “!STPCLK# and HS” is equivalent to “the active low signal STPCLK# is unasserted (i.e., it is at 1.5 V) *and* the HS condition is true.” The symbols “L” and “H” refer respectively to electrical low and electrical high signal levels. The symbols “0” and “1” refer respectively to logical low and logical high signal levels. For example, BD[3:0] = “1010” = “HLHL” refers to a hexadecimal “A,” and D[3:0]# = “1010” = “LHLH” also refers to a hexadecimal “A.” The symbol “X” refers to a “Don’t Care” condition, where a “0” or a “1” results in the same behavior.

1.3 References

Mobile Intel® Celeron® Processor in BGA2 and Micro-PGA2 Packages datasheet (Order Number 249563)

P6 Family of Processors Hardware Developer's Manual (Order Number 244001)

Intel® Architecture Software Developer's Manual (Order Number 243193)

Volume I: Basic Architecture (Order Number 243190)

Volume II: Instruction Set Reference (Order Number 243191)

Volume III: System Programming Guide (Order Number 243192)

Intel® Architecture Software Optimization Manual (Order Number 245127)

CK97 Clock Driver Specification (Contact your Intel Field Sales Representative)

Mobile Pentium® III Processor I/O Buffer Models, IBIS Format (Available in electronic form; Contact your Intel Field Sales Representative)

Mobile Pentium® III Processor GTL+ System Bus Layout Guideline (Contact your Intel Field Sales Representative)

Intel® Mobile Pentium® III Processor Thermal Specification Guideline (Contact your Intel Field Sales Representative)

2.0 Intel® Celeron® Processor – LP/ULP Features

2.1 Features in the Intel® Celeron® Processor – LP/ULP

2.1.1 On-die GTL+ Termination

The termination resistors for the GTL+ system bus are integrated onto the processor die. The RESET# signal does not have on-die termination and requires an external 56.2 Ω ±1% terminating resistor.

2.1.2 Streaming SIMD Extensions

The Intel Intel Celeron Processor – LP/ULP implements Streaming SIMD (single instruction, multiple data) extensions. Streaming SIMD extensions can enhance floating point, video, sound, and 3-D application performance.

2.2 Power Management

2.2.1 Clock Control Architecture

The Intel Celeron Processor – LP/ULP clock control architecture (Figure 2) has been optimized for leading edge low power designs. The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power and low exit latency clock state that can be used for hardware controlled "idle" computer states. The Deep Sleep state provides an extremely low-power state that can be used for "Power-On-Suspend" computer states, which is an alternative to shutting off the processor's power. Compared to the Pentium processor exit latency of 1 ms, the exit latency of the Deep Sleep state has been reduced to 30 µs in the Intel Celeron Processor – LP/ULP. Performing state transitions not shown in Figure 2 is neither recommended nor supported.

The Stop Grant and Quick Start clock states are mutually exclusive, i.e., a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. The Quick Start state is enabled by strapping the A15# signal to ground at Reset; otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state. The Stop Grant state has a higher power level than the Quick Start state and is designed for Symmetric Multi-Processing (SMP) platforms. The Quick Start state has a much lower power level, but it can only be used in uniprocessor platforms. Table 1 provides clock state characteristics, which are described in detail in the following sections.

2.2.2 Normal State

The Normal state of the processor is the normal operating mode where the processor's core clock is running and the processor is actively executing instructions.

2.2.3 Auto Halt State

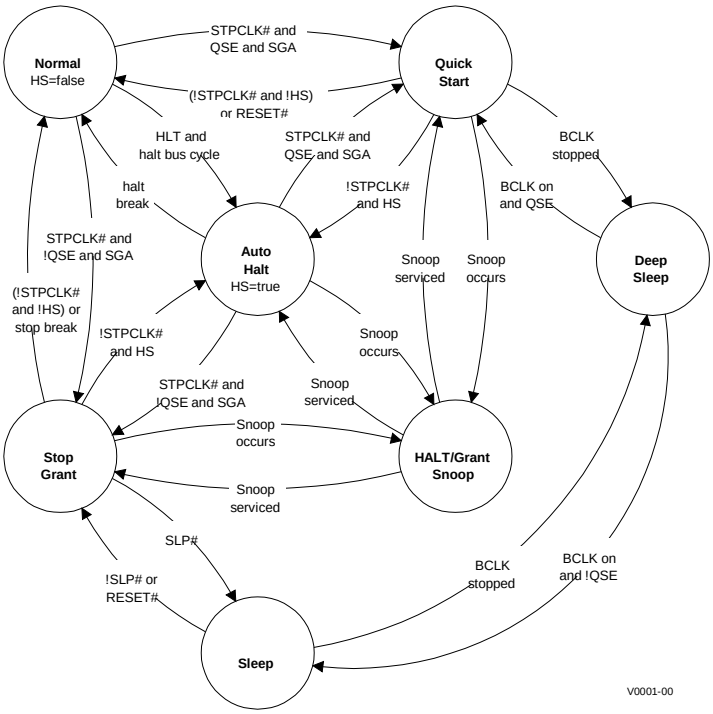
This is a low-power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant or Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from the System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

Figure 2. Clock Control States



NOTES:

halt break – A20M#, BINIT#, FLUSH#, INIT#, INTR, NMI, PREQ#, RESET#, SMI#
HLT – HLT instruction executed
HS – Processor Halt State
QSE – Quick Start State Enabled
SGA – Stop Grant Acknowledge bus cycle issued
stop break – BINIT#, RESET#

2.2.4 Stop Grant State

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal or the occurrence of a stop break event (a BINIT# or RESET# assertion).

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of FLUSH#, SMI#, INIT#, INTR, and NMI (or LINT[1:0]) will be latched by the processor. These latched events will not be serviced until the processor returns to the Normal state. Only one of each event will be recognized upon return to the Normal state.

2.2.5 Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a uniprocessor (UP) configuration.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

2.2.6 HALT/Grant Snoop State

The processor will respond to snoop transactions on the system bus while in the Auto Halt, Stop Grant, or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

2.2.7 Sleep State

The Sleep state is a very low-power state in which the processor maintains its context and the phase-locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state, the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal or Auto Halt states.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state, the processor can enter its lowest power state, the Deep Sleep state. Removing the processor’s input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

2.2.8 Deep Sleep State

The Deep Sleep state is the lowest power mode the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK input to the processor, while it is in the Sleep or Quick Start state. For proper operation, the BCLK input should be stopped in the Low state.

The processor will return to the Sleep or Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a delay of up to 30 µs after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior.

Table 1. Clock State Characteristics

Clock State	Exit Latency	Snooping?	System Uses
Normal	N/A	Yes	Normal program execution
Auto Halt	Approximately 10 bus clocks	Yes	S/W controlled entry idle mode
Stop Grant	10 bus clocks	Yes	H/W controlled entry/exit throttling
Quick Start	Through snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 8 bus clocks	Yes	H/W controlled entry/exit throttling
HALT/Grant Snoop	A few bus clocks after the end of snoop activity	Yes	Supports snooping in the low power states
Sleep	To Stop Grant state 10 bus clocks	No	H/W controlled entry/exit desktop idle mode support
Deep Sleep	30 µs	No	H/W controlled entry/exit powered-on suspend support

NOTE: See Table 29 for power dissipation in the low-power states.

2.2.9 Operating System Implications of Low-power States

There are a number of architectural features of the Intel Celeron Processor – LP/ULP that do not function in the Quick Start or Sleep state as they do in the Stop Grant state. The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start or Sleep states. The local APIC timer and performance monitor counter interrupts should be disabled before entering the Deep Sleep state or the resulting behavior will be unpredictable.

2.2.10 GTL+ Signals

The Intel Celeron Processor – LP/ULP system bus signals use a variation of the low-voltage swing GTL signaling technology. The Intel Celeron Processor – LP/ULP system bus specification is similar to the Pentium II processor system bus specification, which is a version of GTL with enhanced noise margins and less ringing.

The GTL+ system bus depends on incident wave switching and uses flight time for timing calculations of the GTL+ signals, as opposed to capacitive derating. Analog signal simulation of the system bus including trace lengths is highly recommended. Contact your field sales representative to receive the IBIS models for the Intel Celeron Processor – LP/ULP.

The GTL+ system bus of the Pentium II processor was designed to support high-speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in most embedded systems the system bus only has two loads (the processor and the chipset) and the bus traces are short. It is possible to change the layout and termination of the system bus to take advantage of the embedded environment using the same GTL+ I/O buffers. In embedded systems the GTL+ system bus is terminated at one end only. This termination is provided on the processor core (except for the RESET# signal). Refer to the *Mobile Pentium® III Processor GTL+ System Bus Layout Guideline* for details on laying out the GTL+ system bus.

2.2.11 Intel® Celeron® Processor – LP/ULP CPUID

When the CPUID version information is loaded with EAX=01H, the EAX and EBX registers contain the values shown in Table 2. After a power-on RESET, the EDX register contains the processor version information (type, family, model, stepping). See the *Intel® Processor Identification and the CPUID Instruction* application note AP-485 for further information.

Table 2. Intel® Celeron® Processor – LP/ULP CPUID

EAX[31:0]					EBX[7:0]
Reserved [31:14]	Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]	Brand ID
X	0	6	8	X	01

After the L2 cache is initialized, the CPUID cache/TLB descriptors will be the values shown in Table 3.

Table 3. Intel® Celeron® Processor – LP/ULP CPUID Cache and TLB Descriptors

Cache and TLB Descriptors	01H, 02H, 03H, 04H, 08H, 0CH, 41H

3.0 Electrical Specifications

3.1 Processor System Signals

Table 4 lists the processor system signals by type. All GTL+ signals are synchronous with the BCLK signal. All TAP signals are synchronous with the TCK signal except TRST#. All CMOS input signals can be applied asynchronously.

Table 4. System Signal Groups

Group Name	Signals
GTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
GTL+ Output	PRDY#
GTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BREQ0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
1.5 V CMOS Input[2]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SLP#, SMI#, STPCLK#
2.5 V CMOS Input[1, 3]	PWRGOOD
1.5 V Open Drain Output[2]	FERR#, IERR#
3.3 V CMOS Input[4]	BSEL[1:0]
Clock[3]	BCLK
APIC Clock[3]	PICCLK
APIC I/O[2]	PICD[1:0]
Thermal Diode	THERMDA, THERMDC
TAP Input[2]	TCK, TDI, TMS, TRST#
TAP Output[2]	TDO
Power/Other[5]	CLKREF, CMOSREF, EDGECTRLP, NC, PLL1, PLL2, RSVD, RTTIMPEDP, TESTHI, TESTLO[2:1], V_{CC}, V_{CCT}, VID[4:0], V_{REF}, V_{SS}

NOTES:
1. See Section 8.1.38 for information on the PWRGOOD signal.
2. These signals are tolerant to 1.5 V only. See Table 5 for the recommended pull-up resistor.
3. These signals are tolerant to 2.5 V only. See Table 5 for the recommended pull-up resistor.
4. These signals are tolerant to 3.3 V only. See Table 5 for the recommended pull-up resistor.
5. V_{CC} is the power supply for the core logic. PLL1 and PLL2 are the power supply for the PLL analog section. V_{CCT} is the power supply for the system bus buffers. V_{REF} is the voltage reference for the GTL+ input buffers. V_{SS} is system ground.

The CMOS, APIC, and TAP inputs can be driven from ground to 1.5 V. BCLK, PICCLK, and PWRGOOD can be driven from ground to 2.5 V. The APIC data and TAP outputs are Open-drain and should be pulled up to 1.5 V using resistors with the values shown in Table 5. If Open-drain drivers are used for input signals, then they should also be pulled up to the appropriate voltage using resistors with the values shown in Table 5.

Table 5. Recommended Resistors for Intel® Celeron® Processor – LP/ULP Signals

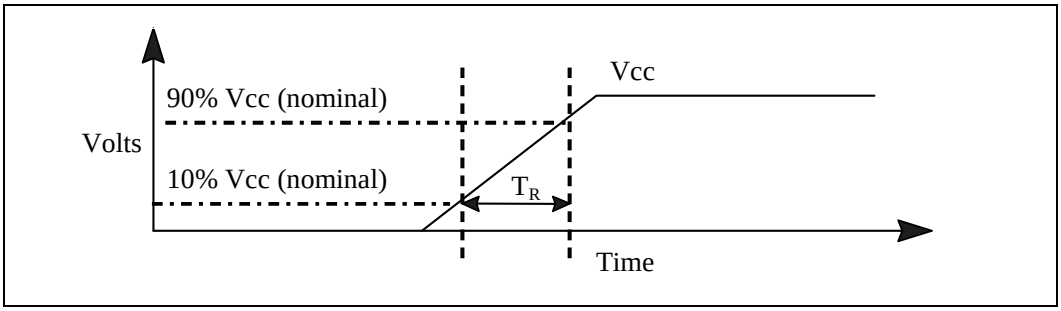
Recommended Resistor Value (Ω)	Celeron Processor – LP/ULP Signal[1, 2]
10 pull-down	BREQ0#[3]
56.2 pull-up	RESET#[4]
150 pull-up	PICD[1:0], TDI, TDO
270 pull-up	SMI#
680 pull-up	STPCLK#
1K pull-up	INIT#, TCK, TMS
1K pull-down	TRST#
1.5K pull-up	A20M#, FERR#, FLUSH#, IERR#, IGNNE#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD, SLP#

NOTES:
1. The recommendations above are only for signals that are being used. These recommendations are maximum values only; stronger pull-ups may be used. Pull-ups for the signals driven by the chipset should not violate the chipset specification. Refer to Section 3.1.4 for the required pull-up or pull-down resistors for signals that are not being used.
2. Open-drain signals must never violate the undershoot specification in Section 4.3. Use stronger pull-ups if there is too much undershoot.
3. A pull-down on BREQ0# is an alternative to having the central agent to drive BREQ0# low at reset.
4. A 56.2Ω 1% terminating resistor connected to V_{CCT} is required.

3.1.1 Power Sequencing Requirements

The Intel Celeron Processor – LP/ULP has no power sequencing requirements. Intel recommends that all of the processor power planes rise to their specified values within one second of each other. The V_{CC} power plane must not rise too fast. At least 200 µs (T_R) must pass from the time that V_{CC} is at 10% of its nominal value until the time that V_{CC} is at 90% of its nominal value (see Figure 3).

Figure 3. Vcc Ramp Rate Requirement



3.1.2 Test Access Port (TAP) Connection

The TAP interface is an implementation of the IEEE 1149.1 (“JTAG”) standard. Due to the voltage levels supported by the TAP interface, Intel recommends that the Intel Celeron Processor – LP/ULP and the other 1.5-V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3-V or 5.0-V JTAG interfaces within the system. A translation buffer should be

used to reduce the TDO output voltage of the last 3.3/5.0 V device down to the 1.5 V range that the Intel Celeron Processor – LP/ULP can tolerate. Multiple copies of TMS and TRST# must be provided, one for each voltage level.

A Debug Port and connector may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placing the Intel Celeron Processor – LP/ULP in the JTAG chain, except for those that are dictated by voltage requirements of the TAP signals.

3.1.3 Catastrophic Thermal Protection

The Intel Celeron Processor – LP/ULP does not support catastrophic thermal protection or the THERMTRIP# signal. An external thermal sensor must be used to protect the processor and the system against excessive temperatures.

3.1.4 Unused Signals

All signals named NC and RSVD must be unconnected. The TESTHI signal should be pulled up to V_{CCT}. The TESTLO1 and TESTLO2 signal should be pulled down to V_{SS}. Unused GTL+ inputs, outputs and bidirectional signals should be unconnected. Unused CMOS active low inputs should be connected to V_{CCT} and unused active high inputs should be connected to V_{SS}. Unused Open-drain outputs should be unconnected. If the processor is configured to enter the Quick Start state rather than the Stop Grant state, then the SLP# signal should be connected to V_{CCT}. When tying any signal to power or ground, a resistor will allow for system testability. For unused signals, Intel suggests that 1.5-kΩ resistors are used for pull-ups and 1-kΩ resistors are used for pull-downs.

If the local APIC is hardware disabled, then PICCLK and PICD[1:0] should be tied to V_{SS} with a 1-kΩ resistor, one resistor can be used for the three signals. Otherwise PICCLK must be driven with a clock that meets specification (see Table 16) and the PICD[1:0] signals must be pulled up to V_{CCT} with 150-Ω resistors, even if the local APIC is not used.

BSEL1 must be connected to V_{SS} and BSEL0 must be pulled up to V_{CCT}. VID[4:0] should be connected to V_{SS} if they are not used.

If the TAP signals are not used then the inputs should be pulled to ground with 1-kΩ resistors and TDO should be left unconnected.

3.1.5 Signal State in Low-power States

3.1.5.1 System Bus Signals

All of the system bus signals have GTL+ input, output, or input/output drivers. Except when servicing snoops, the system bus signals are three-stated and pulled up by the termination resistors. Snoops are not permitted in the Sleep and Deep Sleep states.

3.1.5.2 CMOS and Open-drain Signals

The CMOS input signals are allowed to be in either the logic high or low state when the processor is in a low-power state. In the Auto Halt and Stop Grant states these signals are allowed to toggle.

These input buffers have no internal pull-up or pull-down resistors and system logic can use CMOS or Open-drain drivers to drive them.

The Open-drain output signals have open drain drivers and external pull-up resistors are required. One of the two output signals (IERR#) is a catastrophic error indicator and is three-stated (and pulled-up) when the processor is functioning normally. The FERR# output can be either three-stated or driven to V_{SS} when the processor is in a low-power state depending on the condition of the floating point unit. Since this signal is a DC current path when it is driven to V_{SS}, Intel recommends that the software clears or masks any floating-point error condition before putting the processor into the Deep Sleep state.

3.1.5.3 Other Signals

The system bus clock (BCLK) must be driven in all of the low-power states except the Deep Sleep state. The APIC clock (PICCLK) must be driven whenever BCLK is driven unless the APIC is hardware disabled or the processor is in the Sleep state. Otherwise, it is permitted to turn off PICCLK by holding it at V_{SS}. The system bus clock should be held at V_{SS} when it is stopped in the Deep Sleep state.

In the Auto Halt and Stop Grant states the APIC bus data signals (PICD[1:0]) may toggle due to APIC bus messages. These signals are required to be three-stated and pulled-up when the processor is in the Quick Start, Sleep, or Deep Sleep states unless the APIC is hardware disabled.

3.2 Power Supply Requirements

3.2.1 Decoupling Recommendations

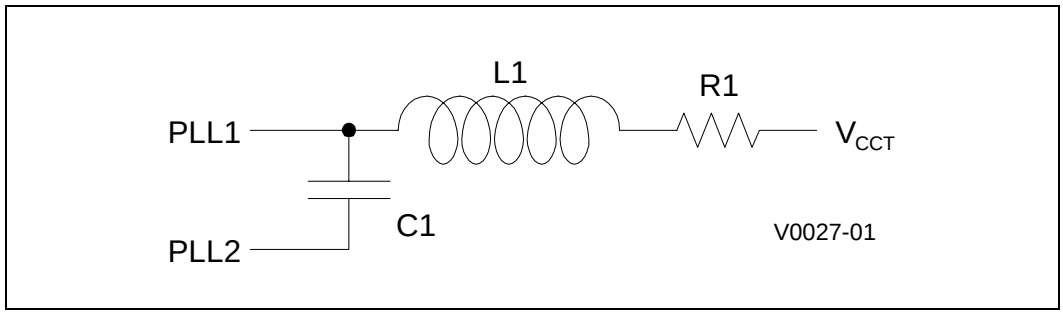
The amount of bulk decoupling required on the V_{CC} and V_{CCT} planes to meet the voltage tolerance requirements for the Intel Celeron Processor – LP/ULP are a strong function of the power supply design. Contact your Intel Field Sales Representative for tools to help determine how much bulk decoupling is required.

The processor core power plan (V_{CC}) should have eight 0.1-µF high frequency decoupling capacitors placed underneath the die and twenty 0.1-µF mid frequency decoupling capacitors placed around the die as close to the die as flex solution allows. The system bus buffer power plane (V_{CCT}) should have twenty 0.1-µF high frequency decoupling capacitors around the die.

3.2.2 Voltage Planes

All V_{CC} and V_{SS} pins/balls must be connected to the appropriate voltage plane. All V_{CCT} and V_{REF} pins/balls must be connected to the appropriate traces on the system electronics. In addition to the main V_{CC}, V_{CCT}, and V_{SS} power supply signals, PLL1 and PLL2 provide analog decoupling to the PLL section. PLL1 and PLL2 should be connected according to Figure 4. Do not connect PLL2 directly to V_{SS}. Section 9.0 contains the RLC filter specification.

Figure 4. PLL RLC Filter



3.3 System Bus Clock and Processor Clocking

The 2.5-V BCLK clock input directly controls the operating speed of the system bus interface. All system bus timing parameters are specified with respect to the rising edge of the BCLK input. The Intel Celeron Processor – LP/ULP core frequency is a multiple of the BCLK frequency. The processor core frequency is configured during manufacturing. The configured bus ratio is visible to software in the Power-on configuration register, see Section 7.2 for details.

Multiplying the bus clock frequency is necessary to increase performance while allowing for easier distribution of signals within the system. Clock multiplication within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK input. During Reset or on exit from the Deep Sleep state, the PLL requires some amount of time to acquire the phase of BCLK. This time is called the PLL lock latency, which is specified in Section 3.6, AC timing parameters T18 and T47.

3.4 Maximum Ratings

Table 6 contains the Intel Celeron Processor – LP/ULP stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are provided in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 6. Intel® Celeron® Processor – LP/ULP Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	–40	85	°C	Note 1
V_{CC}(Abs)	Supply Voltage with respect to V_{SS}	–0.5	2.1	V	
V_{CCT}	System Bus Buffer Voltage with respect to V_{SS}	–0.3	2.1	V	
$V_{IN\ GTL}$	System Bus Buffer DC Input Voltage with respect to V_{SS}	–0.3	2.1	V	Notes 2, 3
$V_{IN\ GTL}$	System Bus Buffer DC Input Voltage with respect to V_{CCT}	—	V_{CCT} + 0.7 V	V	Notes 2, 4
V_{IN15}	1.5 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	2.1	V	Note 5
V_{IN25}	2.5 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	3.3	V	Note 6
V_{IN33}	3.3 V Buffer DC Input Voltage with respect to V_{SS}	–0.3	3.5	V	Note 7
V_{INVID}	VID ball/pin DC Input Voltage with respect to V_{SS}	—	5.5	V	
I_{VID}	VID Current		5	mA	Note 8

NOTES:
1. The shipping container is only rated for 65° C.
2. Parameter applies to the GTL+ signal groups only. Compliance with both $V_{IN\ GTL}$ specifications is required.
3. The voltage on the GTL+ signals must never be below –0.3 or above 2.1 V with respect to ground.
4. The voltage on the GTL+ signals must never be above V_{CCT} + 0.7 V even if it is less than V_{SS} + 2.1 V, or a short to ground may occur.
5. Parameter applies to CMOS, Open-drain, APIC, and TAP bus signal groups only.
6. Parameter applies to BCLK, CLKREF, PICCLK and PWRGOOD signals.
7. Parameter applies to BSEL[1:0] signals.
8. Parameter applies to each VID pin/ball individually.

3.5 DC Specifications

Table 7 through Table 10 lists the DC specifications for the Intel Celeron Processor – LP/ULP. Specifications are valid only while meeting specifications for the junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 7. Power Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CC}	Transient V_{CC} for core logic at 300 MHz and 1.10 V at 400A MHz and 1.35 V	 1.02 1.25	 1.10 1.35	 1.18 1.45	 V V	Notes 7, 8 ±80 mV (1.10 V) ±100 mV (1.35 V)
$V_{CC,DC}$	Static V_{CC} for core logic at 300 MHz and 1.10 V at 400A MHz and 1.35 V	 1.02 1.25	 1.10 1.35	 1.18 1.45	 V V	Note 2, 8 ±80 mV (1.10 V) ±100 mV (1.35 V)
V_{CCT}	V_{CC} for System Bus Buffers, Transient tolerance	1.385	1.50	1.615	V	±115 mV, Note 7, 8
$V_{CCT,DC}$	V_{CC} for System Bus Buffers, Static tolerance	1.455	1.50	1.545	V	±3%, Notes 2, 8
I_{CC}	Current for V_{CC} at core frequency at 300 MHz and 1.10 V at 400A MHz and 1.35 V			 5.3 7.8	 A A	 Note 4 Note 4
I_{CCT}	Current for V_{CCT}			2.5	A	Notes 3, 4
$I_{CC,SG}$	Processor Stop Grant and Auto Halt current at 300 MHz and 1.10 V at 400A MHz and 1.35 V			 1.5 1.7	 A A	 Note 4 Note 4
$I_{CC,QS}$	Processor Quick Start and Sleep current at 300 MHz and 1.10 V at 400A MHz and 1.35 V			 1.3 1.5	 A A	 Note 4 Note 4
$I_{CC,DSLP}$	Processor Deep Sleep Leakage current at 300 MHz and 1.10 V at 400A MHz and 1.35 V			 1.1 1.2	 A A	 Note 4 Note 4
dI_{CC}/dt	V_{CC} power supply current slew rate			1400	A/µs	Notes 5, 6

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Static voltage regulation includes: DC output initial voltage set point adjust, output ripple and noise, output load ranges specified in this table, temperature, and warm up.
3. I_{CCT} is the current supply for the system bus buffers, including the on-die termination.
4. $I_{CCx,max}$ specifications are specified at $V_{CC, DC\ max}$, $V_{CCT,max}$, and 100° C and under maximum signal loading conditions.
5. Based on simulations and averaged over the duration of any change in current. Use to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
6. Maximum values specified by design/characterization at nominal V_{CC} and V_{CCT}.
7. V_{CCx} must be within this range under all operating conditions, including maximum current transients. V_{CCx} must return to within the static voltage specification, $V_{CCx,DC}$, within 100 µs after a transient event. The average of V_{CCx} over time must not exceed 1.65 V, as an arbitrarily large time span may be used for this average.
8. Voltages are measured at the package ball.

The signals on the Intel Celeron Processor – LP/ULP system bus are included in the GTL+ signal group. These signals are specified to be terminated to V_{CC}. The DC specifications for these signals are listed in Table 8 and the termination and reference voltage specifications for these signals are listed in Table 9. The Intel Celeron Processor – LP/ULP requires external termination and a V_{REF}. Refer to the *Mobile Pentium III Processor GTL+ System Bus Layout Guideline* for full details of system V_{CCT} and V_{REF} requirements. The CMOS, Open-drain, and TAP signals are designed to interface at 1.5 V levels to allow connection to other devices. BCLK and PICCLK are designed to receive a 2.5 V clock signal. The DC specifications for these signals are listed in Table 10.

Table 8. GTL+ Signal Group DC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{OH}	Output High Voltage	—	—	V	See $V_{CCT,max}$ in Table 9
R_{ON}	Output Low Drive Strength		16.67	Ω	
I_L	Leakage Current for Inputs, Outputs and I/Os		±100	µA	($0 \le V_{IN/OUT} \le V_{CCT}$)

Table 9. GTL+ Bus DC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCT}	Bus Termination Voltage	1.385	1.5	1.615	V	Note 1
V_{REF}	Input Reference Voltage	$^2/_3 V_{CCT}$ – 2%	$^2/_3 V_{CCT}$	$^2/_3 V_{CCT}$ + 2%	V	±2%, Note 2
R_{TT}	Bus Termination Strength	50	56	65	W	On-die R_{TT}, Note 3

NOTES:
1. For simulation use 1.5 V ±10%. For typical simulation conditions use V_{CCTmin} (1.5 V –10%).
2. V_{REF} should be created from V_{CCT} by a voltage divider.
3. The RESET# signal does not have an on-die R_{TT}. It requires an off-die 56.2 Ω ±1% terminating resistor connected to V_{CCT}.

Table 10. Clock, APIC, TAP, CMOS, and Open-drain Signal Group DC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL15}	Input Low Voltage, 1.5 V CMOS	–0.15	$V_{CMOSREFmin}$ – 200 mV	V	
V_{IL25}	Input Low Voltage, 2.5 V CMOS	–0.3	0.7	V	Notes 1, 2
V_{IL33}	Input Low Voltage, 3.3 V CMOS	–0.15	$V_{CMOSREFmin}$ – 200 mV	V	Note 7
$V_{IL,BCLK}$	Input Low Voltage, BCLK	–0.3	0.5	V	Note 2
V_{IH15}	Input High Voltage, 1.5 V CMOS	$V_{CMOSREFmax}$ + 200 mV	V_{CCT}	V	
V_{IH25}	Input High Voltage, 2.5 V CMOS	2.0	2.625	V	Notes 1, 2
V_{IH33}	Input High Voltage, 3.3 V CMOS	$V_{CMOSREFmax}$ + 200 mV	3.465	V	Note 7
$V_{IH,BCLK}$	Input High Voltage, BCLK	2.0	2.625	V	Note 2
V_{OL}	Output Low Voltage		0.4	V	Note 3
V_{OH15}	Output High Voltage, 1.5 V CMOS	N/A	1.615	V	All outputs are Open-drain
V_{OH25}	Output High Voltage, 2.5 V CMOS	N/A	2.625	V	All outputs are Open-drain
$V_{OH,VID}$	Output High Voltage, VID ball/pins	N/A	5.50	V	5V + 10%
$V_{CMOSREF}$	CMOSREF Voltage	0.90	1.10	V	Note 4
V_{CLKREF}	CLKREF Voltage	1.175	1.325	V	1.25V ±6%, Note 4
I_{OL}	Output Low Current	10		mA	Note 6
I_L	Leakage Current for Inputs, Outputs and I/Os		±100	µA	Notes 5, 8

NOTES:
1. Parameter applies to the PICCLK and PWRGOOD signals only.
2. $V_{ILx,min}$ and $V_{IHx,max}$ only apply when BCLK and PICCLK are stopped. BCLK and PICCLK should be stopped in the low state. See Table 20 for the BCLK voltage range specifications for when BCLK is running. See Table 21 for the PICCLK voltage range specifications for when PICCLK is running.
3. Parameter measured at 10 mA.
4. $V_{CMOSREF}$ and V_{CLKREF} should be created from a stable voltage supply using a voltage divider.
5. ($0 \leq V_{IN/OUT} \leq V_{IHx,max}$).
6. Specified as the minimum amount of current that the output buffer must be able to sink. However, $V_{OL,max}$ cannot be guaranteed if this specification is exceeded.
7. Parameter applies to BSEL[1:0] signals only.
8. For BSEL[1:0] signals, $I_{L, Max}$ can be up to 100 µA (with 1 KΩ pull-up to 1.5 V), and can be up to 500 µA (with 1 KΩ pull-up to 3.3 V)

3.6 AC Specifications

3.6.1 System Bus, Clock, APIC, TAP, CMOS, and Open-drain AC Specifications

Table 11 through Table 19 provide AC specifications associated with the Intel Celeron Processor – LP/ULP. The AC specifications are divided into the following categories: Table 11 contains the system bus clock specifications; Table 12 contains the processor core frequencies; Table 13 contains the GTL+ specifications; Table 14 contains the CMOS and Open-drain signal groups specifications; Table 15 contains timings for the reset conditions; Table 16 contains the APIC specifications; Table 17 contains the TAP specifications; and Table 18 and Table 19 contain the power management timing specifications.

All system bus AC specifications for the GTL+ signal group are relative to the rising edge of the BCLK input at 1.25 V. All GTL+ timings are referenced to V_{REF} for both "0" and "1" logic levels unless otherwise specified. All APIC, TAP, CMOS, and Open-drain signals except PWRGOOD are referenced to 0.75 V.

Table 11. System Bus Clock AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
	System Bus Frequency		100		MHz		
T1	BCLK Period		10		ns	Figure 6	Note 2
T2	BCLK Period Stability			±250	ps	Figure 6	Notes 3, 4
T3	BCLK High Time	2.70			ns	Figure 6	at >2.0 V
T4	BCLK Low Time	2.45			ns	Figure 6	at <0.5 V
T5	BCLK Rise Time	0.175		0.875	ns	Figure 6	(0.9 V – 1.6 V)
T6	BCLK Fall Time	0.175		0.875	ns	Figure 6	(1.6 V – 0.9 V)

NOTES:
1. All AC timings for GTL+ and CMOS signals are referenced to the BCLK rising edge at 1.25 V. All CMOS signals are referenced at 0.75 V.
2. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
3. Not 100% tested. Specified by design/characterization.
4. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.

Table 12. Supported Processor Frequencies

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

BCLK Frequency (MHz)	Frequency Multiplier	Core Frequency (MHz)	Power-on Configuration bits [27, 25:22]
100	3.0	300	0, 0001
100	4.0	400	0, 0010

NOTE: While other combinations of bus and core frequencies are defined, operation at frequencies other than those listed above will not be validated by Intel and are not guaranteed. The frequency multiplier is programmed into the processor when it is manufactured and it cannot be changed.

Table 13. GTL+ Signal Groups AC Specifications

R_{TT} = 56 Ω internally terminated to V_{CCT}; V_{REF} = $^2/_3$ V_{CCT}; load = 0 pF;
T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter[1]	Min	Max	Unit	Figure	Notes
T7	GTL+ Output Valid Delay at 300 MHz and 1.10 V at 400A MHz and 1.35 V	 0.2 0.2	 3.4 2.7	 ns ns	 Figure 7 Figure 7	 Note 7 Note 6
T8	GTL+ Input Setup Time	1.2		ns	Figure 8	Notes 2, 3
T9	GTL+ Input Hold Time at 300 MHz and 1.10 V at 400A MHz and 1.35 V	 1.2 0.80		 ns ns	 Figure 8 Figure 8	 Notes 4, 7 Notes 4, 6
T10	RESET# Pulse Width	1.0		ms	Figure 9 Figure 10	Note 5

NOTES:
1. All AC timings for GTL+ signals are referenced to the BCLK rising edge at 1.25 V. All GTL+ signals are referenced at V_{REF}.
2. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
3. Specification is for a minimum 0.40 V swing.
4. Specification is for a maximum 1.0 V swing.
5. After V_{CC}, V_{CCT}, and BCLK become stable and PWRGOOD is asserted.
6. Applies to all core VCC other than 1.10 V.
7. Applies only when core VCC is 1.10 V.

Table 14. CMOS and Open-drain Signal Groups AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter[1, 2]	Min	Max	Unit	Figure	Notes
T14	1.5 V Input Pulse Width, except PWRGOOD and LINT[1:0]	2		BCLKs	Figure 7	Active and Inactive states
T14B	LINT[1:0] Input Pulse Width	6		BCLKs	Figure 7	Note 3
T15	PWRGOOD Inactive Pulse Width	10		BCLKs	Figure 10	Notes 4, 5

NOTES:
1. All AC timings for CMOS and Open-drain signals are referenced to the BCLK rising edge at 1.25 V. All CMOS and Open-drain signals are referenced at 0.75 V.
2. Minimum output pulse width on CMOS outputs is 2 BCLKs.
3. This specification only applies when the APIC is enabled and the LINT1 or LINT0 signal is configured as an edge triggered interrupt with fixed delivery, otherwise specification T14 applies.
4. When driven inactive, or after V_{CC}, V_{CCT} and BCLK become stable. PWRGOOD must remain below $V_{IL25,max}$ from Table 10 until all the voltage planes meet the voltage tolerance specifications in Table 7 and BCLK has met the BCLK AC specifications in Table 11 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.
5. If the BCLK Settling Time specification (T60) can be guaranteed at power-on reset then the PWRGOOD Inactive Pulse Width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL25,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 15. Reset Configuration AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T16	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time	4		BCLKs	Figure 7 Figure 8	Before deassertion of RESET#
T17	Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time	2	20	BCLKs	Figure 7 Figure 8	After clock that deasserts RESET#
T18	RESET#/PWRGOOD Setup Time	1		ms	Figure 10	Before deassertion of RESET#, Note 1

NOTE:
1. At least 1 ms must pass after PWRGOOD rises above $V_{IH25,min}$ from Table 10 and BCLK meets its AC timing specification until RESET# may be deasserted.

Table 16. APIC Bus Signal AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter[1]	Min	Max	Unit	Figure	Notes
T21	PICCLK Frequency	2	33.3	MHz		Note 2
T22	PICCLK Period	30	500	ns	Figure 5	
T23	PICCLK High Time	10.5		ns	Figure 5	at >1. 7 V
T24	PICCLK Low Time	10.5		ns	Figure 5	at <0.7 V
T25	PICCLK Rise Time	0.25	3.0	ns	Figure 5	(0.7 V – 1.7 V)
T26	PICCLK Fall Time	0.25	3.0	ns	Figure 5	(1.7 V – 0.7 V)
T27	PICD[1:0] Setup Time	8.0		ns	Figure 8	Note 3
T28	PICD[1:0] Hold Time	2.5		ns	Figure 8	Note 3
T29	PICD[1:0] Valid Delay	1.5	10.0	ns	Figure 7	Notes 3, 4, 5

NOTES:
1. All AC timings for APIC signals are referenced to the PICCLK rising edge at 1.25 V. All CMOS signals are referenced at 0.75 V.
2. The minimum frequency is 2 MHz when PICD0 is at 1.5 V at reset. If PICD0 is strapped to V_{SS} at reset then the minimum frequency is 0 MHz.
3. Referenced to PICCLK Rising Edge.
4. For Open-drain signals, Valid Delay is synonymous with Float Delay.
5. Valid delay timings for these signals are specified into 150 Ω to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.

Table 17. TAP Signal AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter[1]	Min	Max	Unit	Figure	Notes
T30	TCK Frequency	—	16.67	MHz		
T31	TCK Period	60	—	ns	Figure 5	
T32	TCK High Time	25.0		ns	Figure 5	≥ 1.2 V, Note 2
T33	TCK Low Time	25.0		ns	Figure 5	≤ 0.6 V, Note 2
T34	TCK Rise Time		5.0	ns	Figure 5	(0.6 V – 1.2 V), Notes 2, 3
T35	TCK Fall Time		5.0	ns	Figure 5	(1.2 V – 1.6 V), Notes 2, 3
T36	TRST# Pulse Width	40.0		ns	Figure 12	Asynchronous, Note 2
T37	TDI, TMS Setup Time	5.0		ns	Figure 11	Note 4
T38	TDI, TMS Hold Time	14.0		ns	Figure 11	Note 4
T39	TDO Valid Delay	1.0	10.0	ns	Figure 11	Notes 5, 6
T40	TDO Float Delay		25.0	ns	Figure 11	Notes 2, 5, 6
T41	All Non-Test Outputs Valid Delay	2.0	25.0	ns	Figure 11	Notes 5, 7, 8
T42	All Non-Test Outputs Float Delay		25.0	ns	Figure 11	Notes 2, 5, 7, 8
T43	All Non-Test Inputs Setup Time	5.0		ns	Figure 11	Notes 4, 7, 8
T44	All Non-Test Inputs Hold Time	13.0		ns	Figure 11	Notes 4, 7, 8

NOTES:
1. All AC timings for TAP signals are referenced to the TCK rising edge at 0.75 V. All TAP and CMOS signals are referenced at 0.75 V.
2. Not 100% tested. Specified by design/characterization.
3. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified into 150 Ω terminated to 1.5 V and 0 pF of external load. For real system timings these specifications must be derated for external capacitance at 105 ps/pF.
7. Non-Test Outputs and Inputs are the normal output or input signals (except TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
8. During Debug Port operation use the normal specified timings rather than the TAP signal timings.

Table 18. Quick Start/Deep Sleep AC Specifications

T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter[1]	Min	Max	Unit	Figure	Notes
T45	Stop Grant Cycle Completion to Clock Stop	100		BCLKs	Figure 13	
T46	Stop Grant Cycle Completion to Input Signals Stable		0	µs	Figure 13	
T47	Deep Sleep PLL Lock Latency	0	30	µs	Figure 13 Figure 14	Note 2
T48	STPCLK# Hold Time from PLL Lock	0		ns	Figure 13	
T49	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	Figure 13	

NOTES:
1. Input signals other than RESET# and BPRI# must be held constant in the Quick Start state.
2. The BCLK Settling Time specification (T60) applies to Deep Sleep state exit under all conditions.

Table 19. Stop Grant/Sleep/Deep Sleep AC Specifications

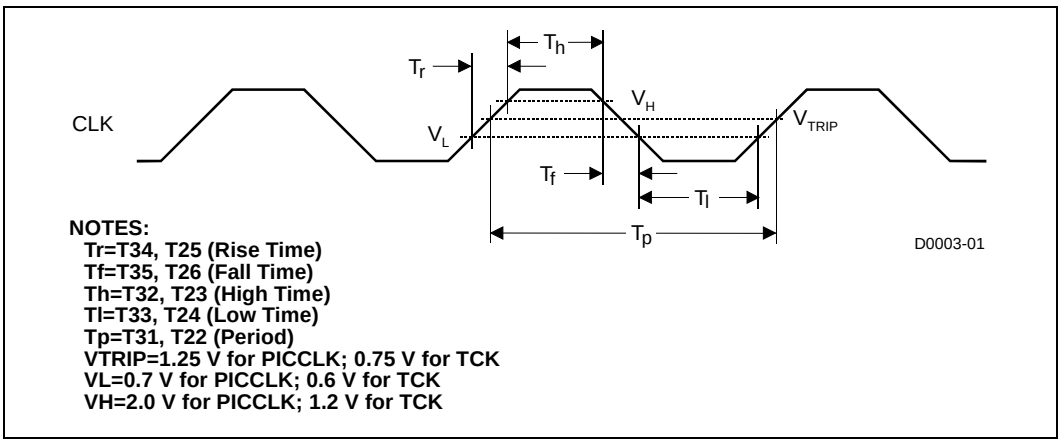
T_J = 0° C to 100° C; V_{CC} = 1.10 V ±80 mV or V_{CC} = 1.35 V ±100 mV; V_{CCT} = 1.50 V ±115 mV

Symbol	Parameter	Min	Max	Unit	Figure
T50	SLP# Signal Hold Time from Stop Grant Cycle Completion	100		BCLKs	Figure 14
T51	SLP# Assertion to Input Signals Stable		0	ns	Figure 14
T52	SLP# Assertion to Clock Stop	10		BCLKs	Figure 14
T54	SLP# Hold Time from PLL Lock	0		ns	Figure 14
T55	STPCLK# Hold Time from SLP# Deassertion	10		BCLKs	Figure 14
T56	Input Signal Hold Time from SLP# Deassertion	10		BCLKs	Figure 14

NOTE: Input signals other than RESET# must be held constant in the Sleep state. The BCLK Settling Time specification (T60) applies to Deep Sleep state exit under all conditions.

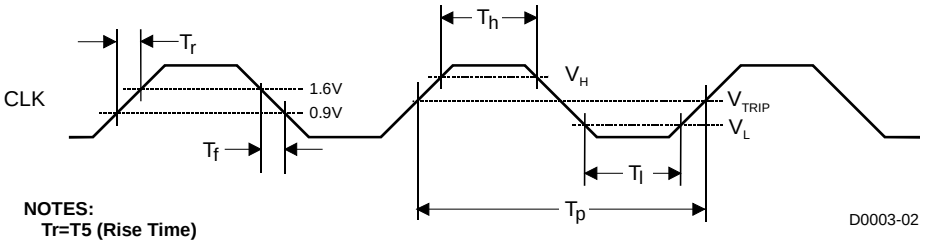
Figure 5 through Figure 15 are to be used in conjunction with Table 11 through Table 19.

Figure 5. PICCLK/TCK Clock Timing Waveform



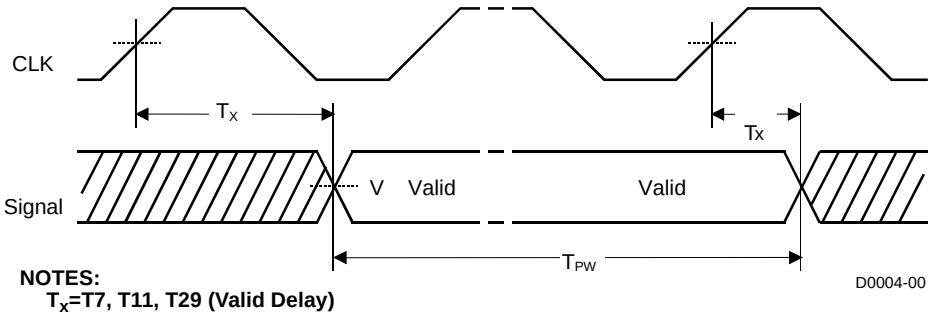
NOTES:
Tr=T34, T25 (Rise Time)
Tf=T35, T26 (Fall Time)
Th=T32, T23 (High Time)
Tl=T33, T24 (Low Time)
Tp=T31, T22 (Period)
VTRIP=1.25 V for PICCLK; 0.75 V for TCK
VL=0.7 V for PICCLK; 0.6 V for TCK
VH=2.0 V for PICCLK; 1.2 V for TCK

Figure 6. BCLK Timing Waveform



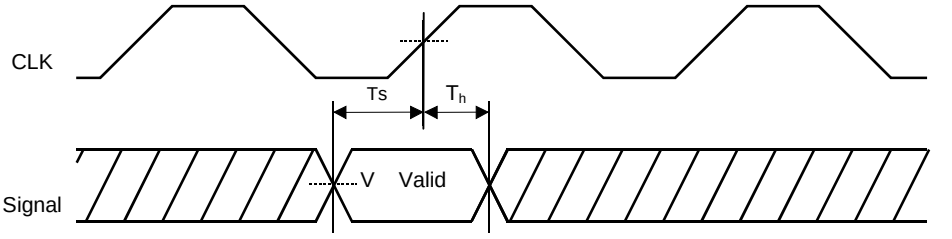
NOTES:
Tr=T5 (Rise Time)
Tf=T6 (Fall Time)
Th=T3 (High Time)
Tl=T4 (Low Time)
Tp=T1 (Period)
VTRIP=1.25 V for BCLK
VL=0.5 V for BCLK
VH=2.0 V for BCLK

Figure 7. Valid Delay Timings



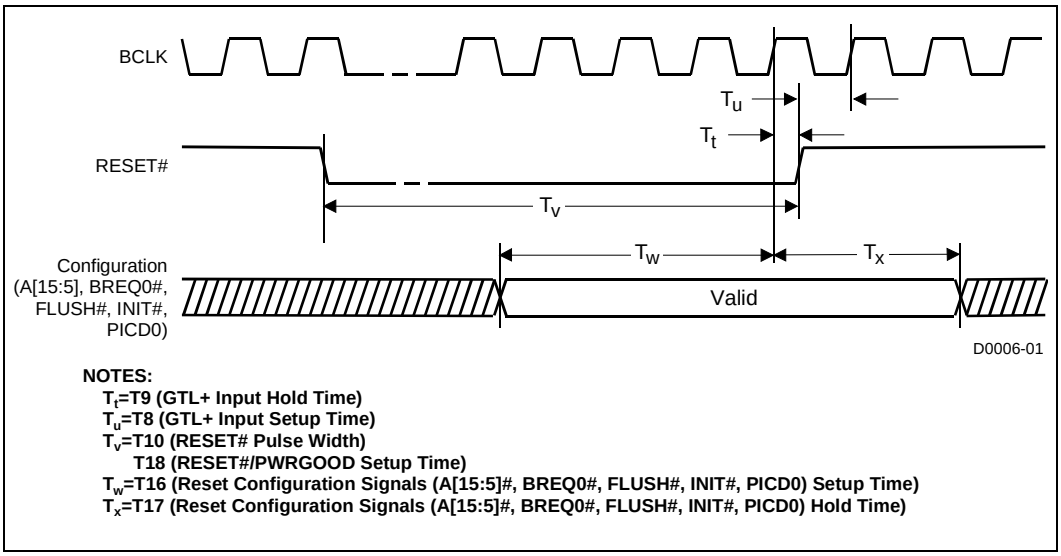
NOTES:
T_x=T7, T11, T29 (Valid Delay)
T_{pw}=T14, T14B (Pulse Width)
V=V_{REF} for GTL+ signal group; 0.75 V for CMOS, Open-drain, APIC, and TAP signal groups

Figure 8. Setup and Hold Timings



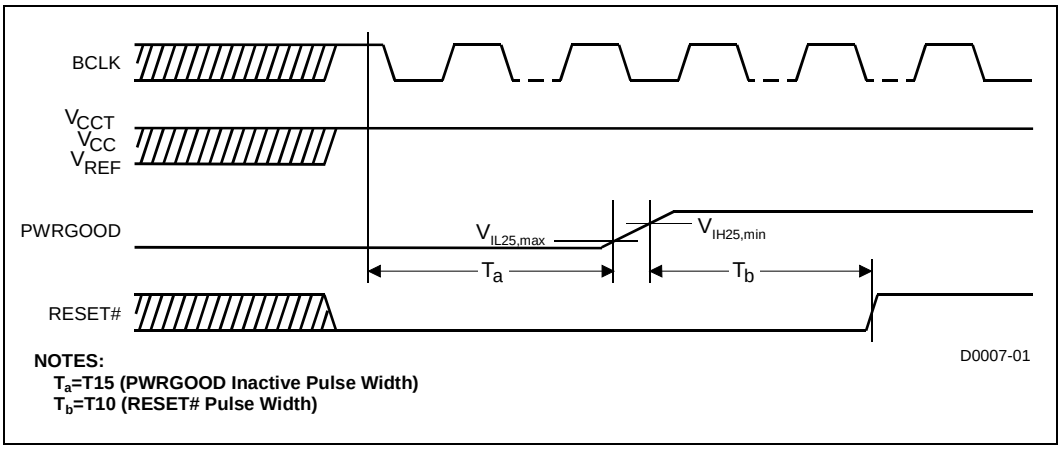
NOTES:
T_s=T8, T12, T27 (Setup Time)
T_h=T9, T13, T28 (Hold Time)
V=V_{REF} for GTL+ signals; 0.75 V for CMOS, APIC, and TAP signals

Figure 9. Cold/Warm Reset and Configuration Timings



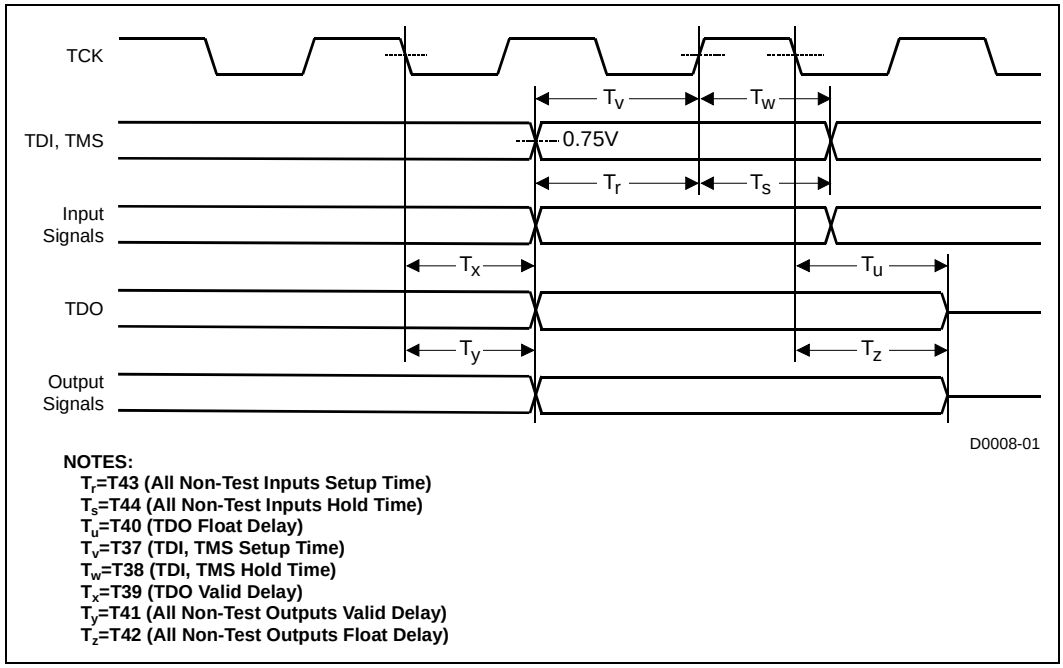
NOTES:
T_t=T9 (GTL+ Input Hold Time)
T_u=T8 (GTL+ Input Setup Time)
T_v=T10 (RESET# Pulse Width)
T18 (RESET#/PWRGOOD Setup Time)
T_w=T16 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Setup Time)
T_x=T17 (Reset Configuration Signals (A[15:5]#, BREQ0#, FLUSH#, INIT#, PICD0) Hold Time)

Figure 10. Power-on Reset Timings



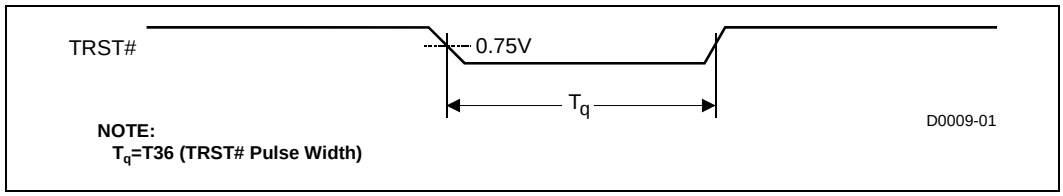
NOTES:
T_a=T15 (PWRGOOD Inactive Pulse Width)
T_b=T10 (RESET# Pulse Width)

Figure 11. Test Timings (Boundary Scan)



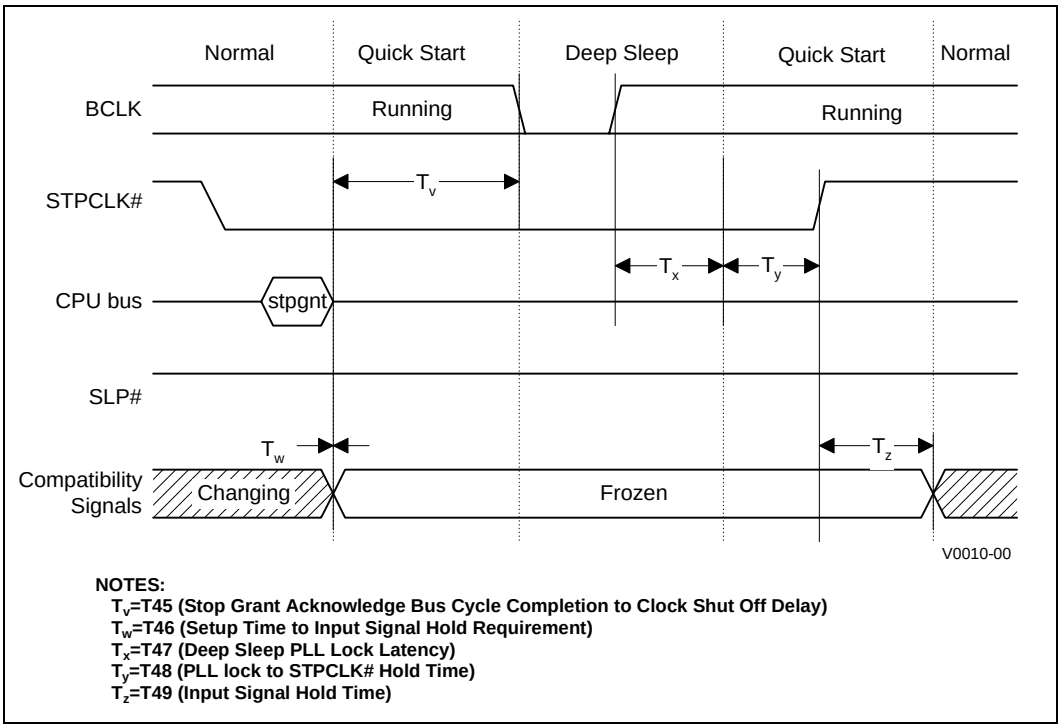
NOTES:
T_r=T43 (All Non-Test Inputs Setup Time)
T_s=T44 (All Non-Test Inputs Hold Time)
T_u=T40 (TDO Float Delay)
T_v=T37 (TDI, TMS Setup Time)
T_w=T38 (TDI, TMS Hold Time)
T_x=T39 (TDO Valid Delay)
T_y=T41 (All Non-Test Outputs Valid Delay)
T_z=T42 (All Non-Test Outputs Float Delay)

Figure 12. Test Reset Timings



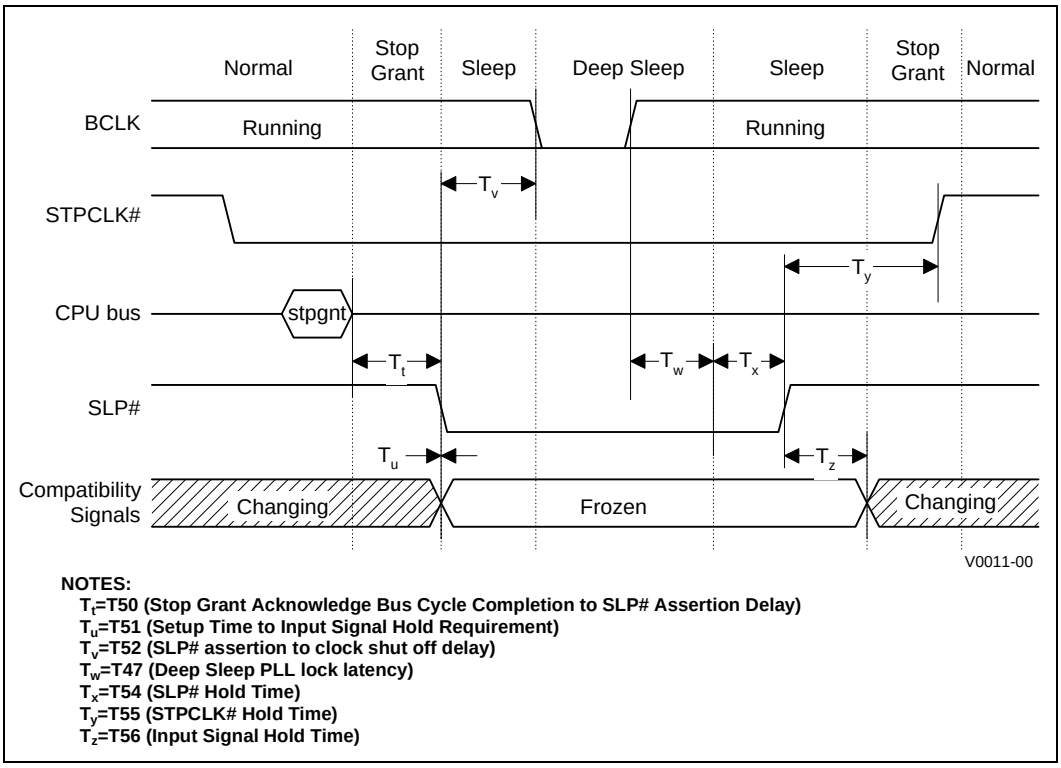
NOTE:
T_q=T36 (TRST# Pulse Width)

Figure 13. Quick Start/Deep Sleep Timing



NOTES:
T_v=T45 (Stop Grant Acknowledge Bus Cycle Completion to Clock Shut Off Delay)
T_w=T46 (Setup Time to Input Signal Hold Requirement)
T_x=T47 (Deep Sleep PLL Lock Latency)
T_y=T48 (PLL lock to STPCLK# Hold Time)
T_z=T49 (Input Signal Hold Time)

Figure 14. Stop Grant/Sleep/Deep Sleep Timing



NOTES:
T_t=T50 (Stop Grant Acknowledge Bus Cycle Completion to SLP# Assertion Delay)
T_u=T51 (Setup Time to Input Signal Hold Requirement)
T_v=T52 (SLP# assertion to clock shut off delay)
T_w=T47 (Deep Sleep PLL lock latency)
T_x=T54 (SLP# Hold Time)
T_y=T55 (STPCLK# Hold Time)
T_z=T56 (Input Signal Hold Time)

4.0 System Signal Simulations

Many scenarios have been simulated to generate a set of GTL+ processor system bus layout guidelines, which are available in the *Mobile Pentium® III Processor GTL+ System Bus Layout Guideline.* Systems must be simulated using the IBIS model to determine if they are compliant with this specification.

4.1 System Bus Clock (BCLK) and PICCLK AC Signal Quality Specifications

Table 20 and Figure 16 show the signal quality for the system bus clock (BCLK) signal, and Table 21 and Figure 16 show the signal quality for the APIC bus clock (PICCLK) signal at the processor. BCLK and PICCLK are 2.5 V clocks.

Table 20. BCLK Signal Quality Specification

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$		0.5	V	Figure 16	Note 1
V2	$V_{IH,BCLK}$	2.0		V	Figure 16	Note 1
V3	V_{IN} Absolute Voltage Range	-0.7	3.5	V	Figure 16	Undershoot/Overshoot, Note 2
V4	BCLK Rising Edge Ringback	2.0		V	Figure 16	Absolute Value, Note 3
V5	BCLK Falling Edge Ringback		0.5	V	Figure 16	Absolute Value, Note 3

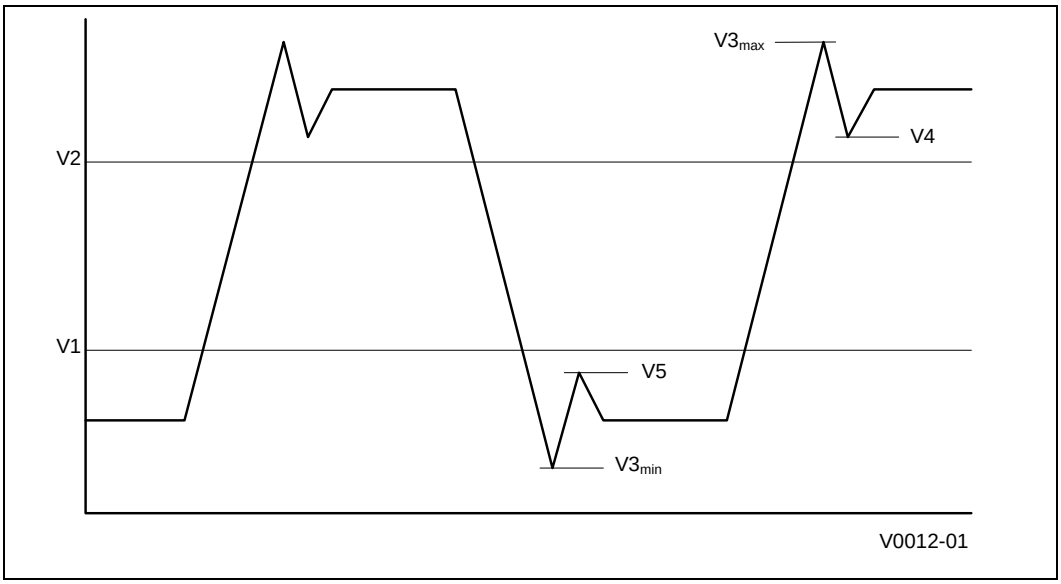
NOTES:
1. The clock must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$.
2. These specifications apply only when BCLK is running, see Table 10 for the DC specifications for when BCLK is stopped. BCLK may not be above $V_{IH,BCLK,max}$ or below $V_{IL,BCLK,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can go to after passing the $V_{IH,BCLK}$ (rising) or $V_{IL,BCLK}$ (falling) voltage limits.

Table 21. PICCLK Signal Quality Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	V_{IL25}		0.7	V	Figure 16	Note 1
V2	V_{IH25}	2.0		V	Figure 16	Note 1
V3	V_{IN} Absolute Voltage Range	–0.7	3.5	V	Figure 16	Undershoot, Overshoot, Note 2
V4	PICCLK Rising Edge Ringback	2.0		V	Figure 16	Absolute Value, Note 3
V5	PICCLK Falling Edge Ringback		0.7	V	Figure 16	Absolute Value, Note 3

NOTES:
1. The clock must rise/fall monotonically between V_{IL25} and V_{IH25}.
2. These specifications apply only when PICCLK is running, see Table 10 for the DC specifications for when PICCLK is stopped. PICCLK may not be above $V_{IH25,max}$ or below $V_{IL25,min}$ for more than 50% of the clock cycle.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the PICCLK signal can go to after passing the V_{IH25} (rising) or V_{IL25} (falling) voltage limits.

Figure 15. BCLK/PICCLK Generic Clock Waveform



4.2 GTL+ AC Signal Quality Specifications

Table 22, Figure 17, and Figure 18 illustrate the GTL+ signal quality specifications for the Intel Celeron Processor – LP/ULP. Refer to the *Pentium® II Processor Developer's Manual* for the GTL+ buffer specification. The Intel Celeron Processor – LP/ULP maximum overshoot and undershoot specifications for a given duration of time are specified in Table 23. Contact your Intel Field Sales representative for a copy of the OVERSHOOT_CHECKER tool. The OVERSHOOT_CHECKER determines if a specific waveform meets the overshoot/undershoot specification. Figure 19 shows the overshoot/undershoot waveform. The tolerances listed in Table 23 are conservative. Signals that exceed these tolerances may still meet the processor overshoot/undershoot tolerance if the OVERSHOOT_CHECKER tool says that they pass.

Table 22. GTL+ Signal Group Ringback Specification

Symbol	Parameter	Min	Unit	Figure	Notes
α	Overshoot	100	mV	Figure 17 Figure 18	Notes 1, 2
τ	Minimum Time at High	0.5	ns	Figure 17 Figure 18	Notes 1, 2
ρ	Amplitude of Ringback	-200	mV	Figure 17 Figure 18	Notes 1, 2, 3
ϕ	Final Settling Voltage	200	mV	Figure 17 Figure 18	Notes 1, 2
δ	Duration of Sequential Ringback	N/A	ns	Figure 17 Figure 18	Notes 1, 2

NOTES:
1. Specified for the edge rate of 0.3 – 0.8 V/ns. See Figure 17 for the generic waveform.
2. All values determined by design/characterization.
3. Ringback below $V_{REF,max}$ + 200 mV is not authorized during low to high transitions. Ringback above $V_{REF,min}$ – 200 mV is not authorized during high to low transitions.

Figure 16. Low to High, GTL+ Receiver Ringback Tolerance

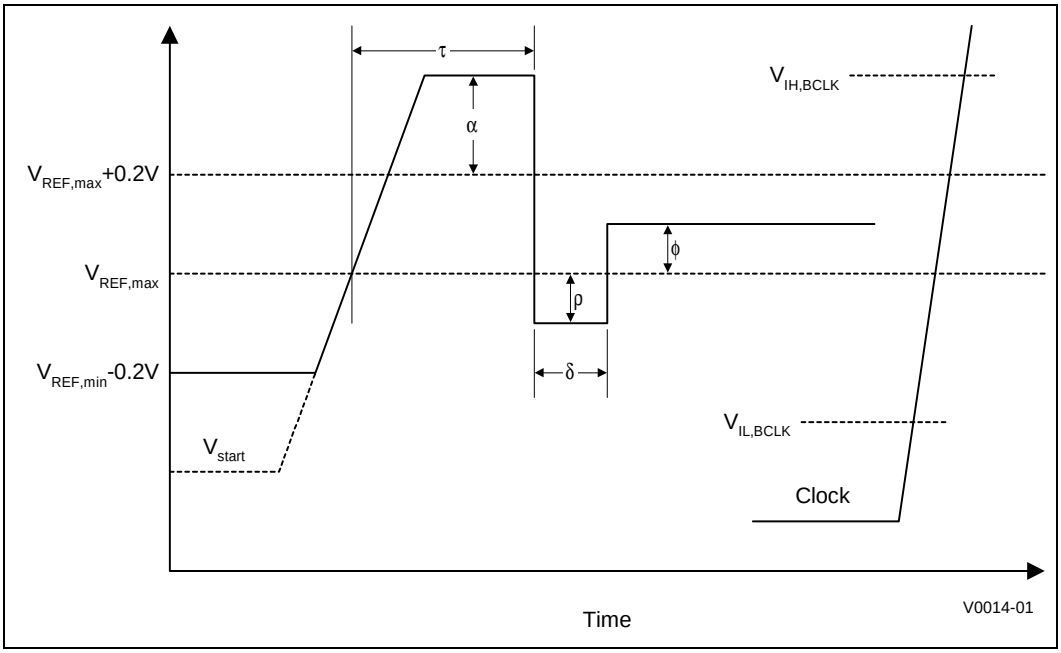


Figure 17. High to Low, GTL+ Receiver Ringback Tolerance

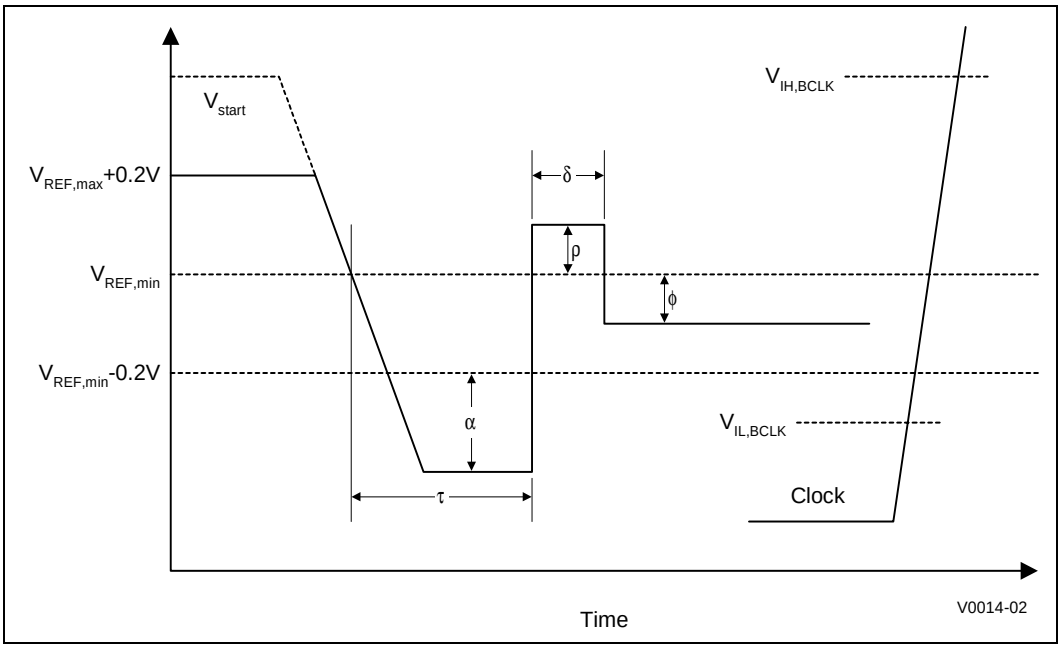
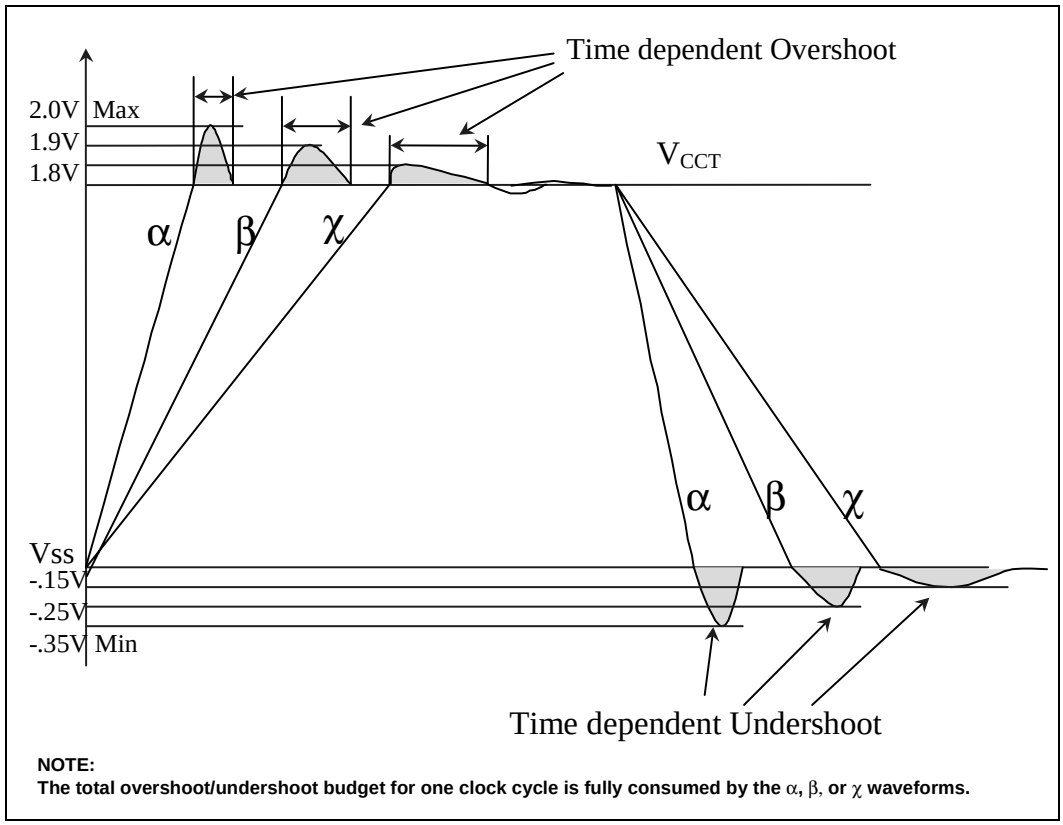


Table 23. GTL+ Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Overshoot Amplitude	Undershoot Amplitude	Allowed Pulse Duration
2.0 V	-0.35 V	0.35 ns
1.9 V	-0.25 V	1.2 ns
1.8 V	-0.15 V	4.3 ns

NOTES:
1. Under no circumstances should the GTL+ signal voltage ever exceed 2.0 V maximum with respect to ground or -2.0 V minimum with respect to V_{CCT} (i.e., V_{CCT} - 2.0 V) under operating conditions.
2. Ringbacks below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
3. Ringbacks above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
4. System designers are encouraged to follow Intel provided GTL+ layout guidelines.
5. All values are specified by design characterization and are not tested.

Figure 18. Maximum Acceptable Overshoot/Undershoot Waveform



NOTE:
The total overshoot/undershoot budget for one clock cycle is fully consumed by the α, β, or χ waveforms.

4.3 Non-GTL+ Signal Quality Specifications

Signals driven to the Intel Celeron Processor – LP/ULP should meet signal quality specifications to ensure that the processor reads data properly and that incoming signals do not affect the long-term reliability of the processor. The Intel Celeron Processor – LP/ULP uses GTL+ buffers for non-GTL+ signals. The input and output paths of the buffers have been slowed down to match the requirements for the non-GTL+ signals. The signal quality specifications for the non-GTL+ signals are identical to the GTL+ signal quality specifications except that they are relative to VCMOSREF rather than VREF transitions OVERSHOOT_CHECKER can be used to verify non-GTL+ signal compliance with the signal overshoot and undershoot tolerance. The tolerances listed in Table 24 are conservative. Signals that exceed these tolerances may still meet the processor overshoot and undershoot tolerance if the OVERSHOOT_CHECKER tool says that they pass.

Table 24. Non-GTL+ Signal Group Overshoot/Undershoot Tolerance at the Processor Core

Overshoot Amplitude	Undershoot Amplitude	Allowed Pulse Duration
2.1 V	-0.45 V	0.45 ns
2.0 V	-0.35 V	1.5 ns
1.9 V	-0.25 V	5.0 ns
1.8 V	-0.15 V	17 ns

NOTES:
1. Under no circumstances should the non-GTL+ signal voltage ever exceed 2.1 V maximum with respect to ground or -2.1 V minimum with respect to V_{CCT} (i.e., V_{CCT} - 2.1 V) under operating conditions.
2. Ring-backs below V_{CCT} cannot be subtracted from overshoots. Lesser undershoot does not allocate longer or larger overshoot.
3. Ring-backs above ground cannot be subtracted from undershoots. Lesser overshoot does not allocate longer or larger undershoot.
4. System designers are encouraged to follow Intel provided non-GTL+ layout guidelines.
5. All values are specified by design characterization, and are not tested.

4.3.1 PWRGOOD Signal Quality Specifications

The processor requires PWRGOOD to be a clean indication that clocks and the power supplies (V_{CC}, V_{CCT}, etc.) are stable and within their specifications. Clean implies that the signal will remain below V_{IL25} and without errors from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5 V) state. PWRGOOD may not ringback below 2.0 V after rising above V_{IH25}.

5.0 Mechanical Specifications

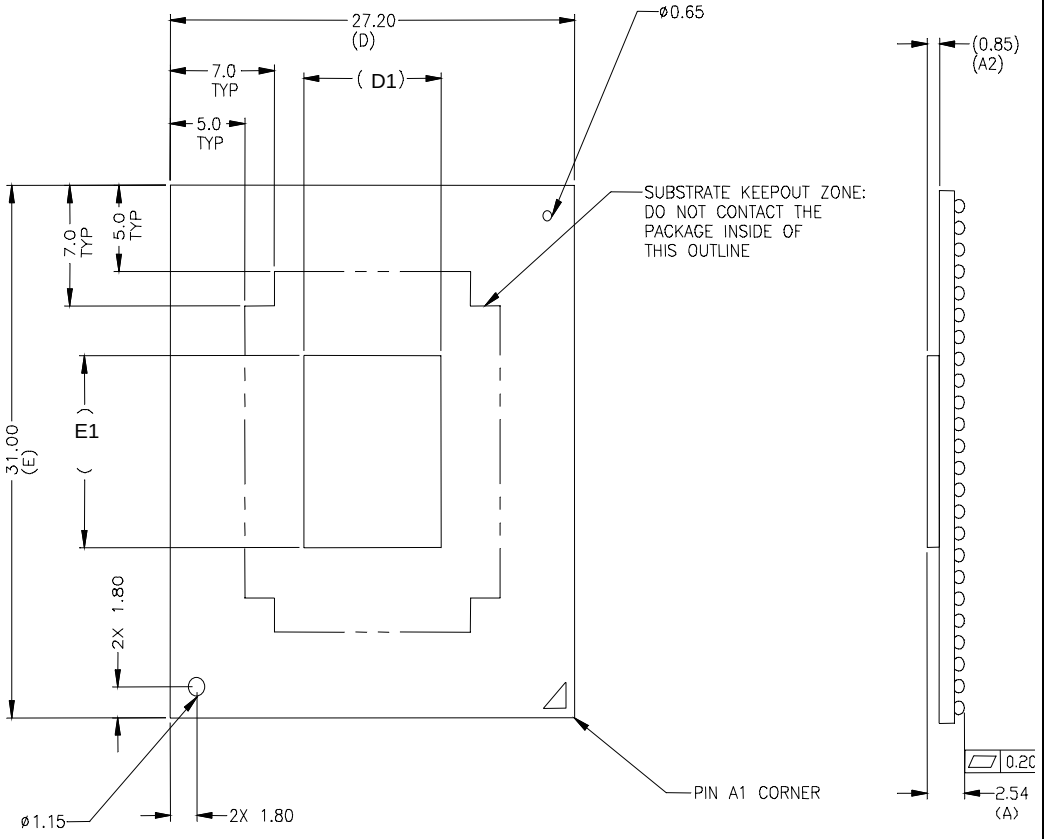
5.1 Surface-mount BGA2 Package Dimensions

The Intel Celeron Processor – LP/ULP is packaged in a PBGA-B495 package (also known as BGA2) with the back of the processor die exposed on top. Unlike previous processors with exposed die, the back of the Intel Celeron Processor – LP/ULP die may be polished and very smooth. The mechanical specifications for the surface-mount package are provided in Table 25. Figure 20 shows the top and side views of the surface-mount package, and Figure 21 shows the bottom view of the surface-mount package. The substrate may only be contacted within the shaded region between the keep-out outline and the edge of the substrate. The Intel Celeron Processor – LP/ULP will have one or two label marks. These label marks will be located along the long edge of the substrate outside of the keep-out region and they will not encroach upon the 7-mm by 7-mm squares at the substrate corners. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated.

Table 25. Surface-mount BGA2 Package Specifications

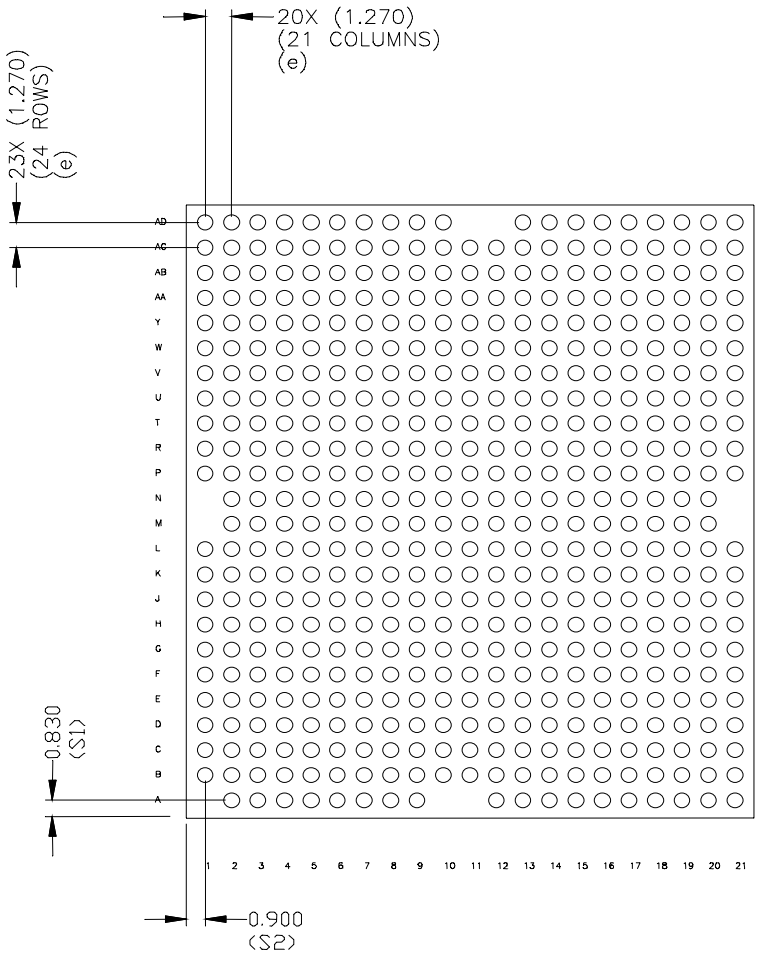
Symbol	Parameter	Min	Max	Unit
A	Overall Height, as delivered	2.29	2.79	mm
A_1	Substrate Height, as delivered	1.50 REF		mm
A_2	Die Height	0.854 REF		mm
b	Ball Diameter	0.78 REF		mm
D	Package Width	27.05	27.35	mm
D_1	Die Width	8.82 REF (CPUID = 0686h) 8.82 REF (CPUID = 068Ah)		mm
E	Package Length	30.85	31.15	mm
e	Ball Pitch	1.27		mm
E_1	Die Length	10.80 REF (CPUID = 0686h) 11.00 REF (CPUID = 068Ah)		mm
N	Ball Count	495		each
S_1	Outer Ball Center to Short Edge of Substrate	0.895 REF		mm
S_2	Outer Ball Center to Long Edge of Substrate	0.900 REF		mm
P_{DIE}	Allowable Pressure on the Die for Thermal Solution	—	689	kPa
W	Package Weight	4.5 REF		grams

Figure 19. Surface-mount BGA2 Package - Top and Side View



NOTE: All dimensions are in millimeters. Dimensions in figure are for reference only, see Table 25 for specifications.

Figure 20. Surface-mount BGA2 Package - Bottom View

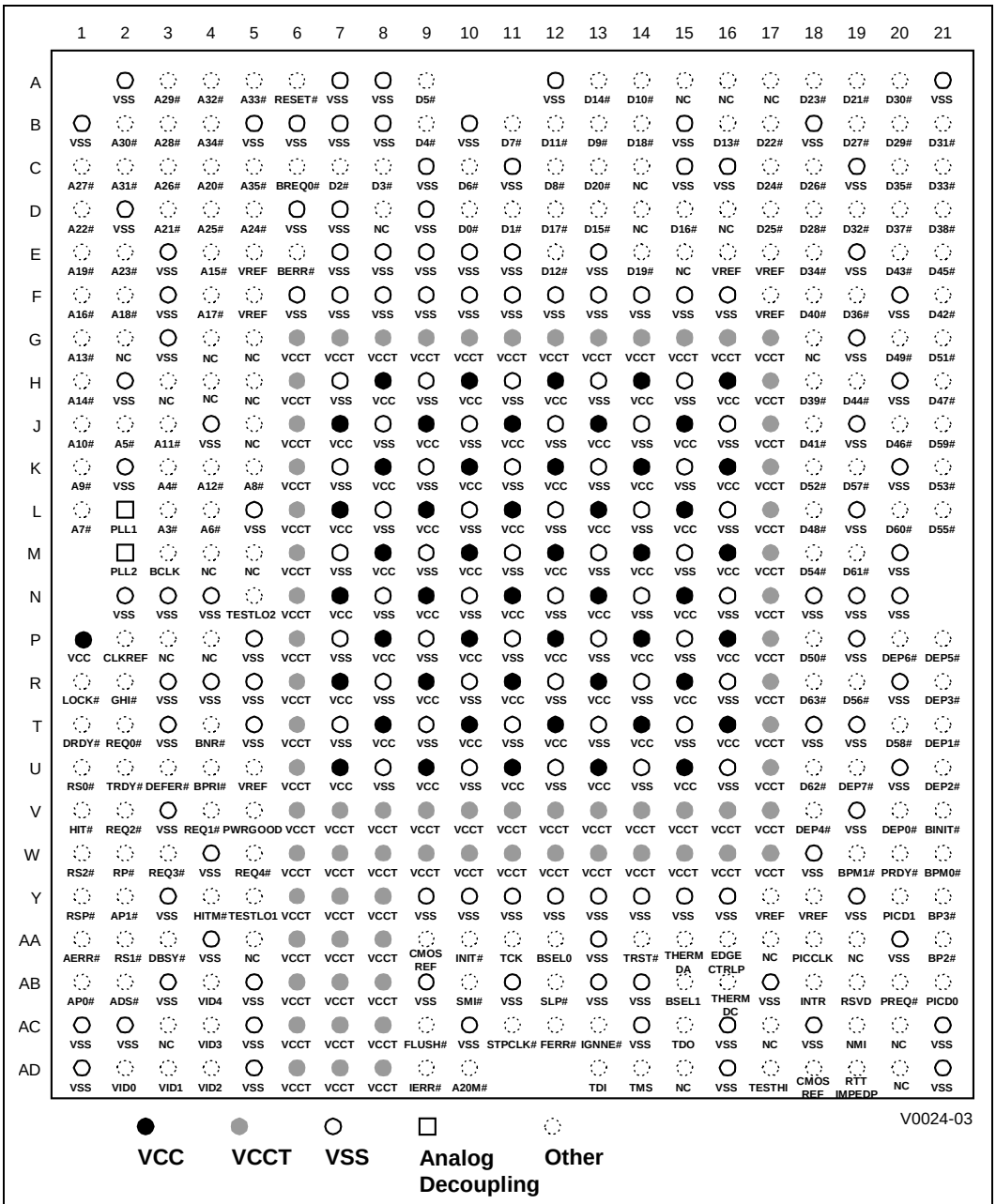


NOTE: All dimensions are in millimeters. Dimensions in figure are for reference only, see Table 25 for specifications

5.2 Signal Listings

Figure 21 is a top-side view of the ball or pin map of the Intel Celeron Processor – LP/ULP with the voltage balls/pins called out. Table 26 lists the signals in ball/pin number order. Table 27 lists the signals in signal name order.

Figure 21. Pin/Ball Map - Top View



NOTES:
1. In order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated.
2. Ball P1 must be connected to Vcc

Table 26. Signal Listing in Order by Pin/Ball Number (Sheet 1 of 3)

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
A2	VSS	C3	A26#	E2	A23#	G1	A13#
A3	A29#	C4	A20#	E3	VSS	G2	NC
A4	A32#	C5	A35#	E4	A15#	G3	VSS
A5	A33#	C6	BREQ0#	E5	VREF	G4	NC
A6	RESET#	C7	D2#	E6	BERR#	G5	NC
A7	VSS	C8	D3#	E7	VSS	G6	VCCT
A8	VSS	C9	VSS	E8	VSS	G7	VCCT
A9	D5#	C10	D6#	E9	VSS	G8	VCCT
A12	VSS	C11	VSS	E10	VSS	G9	VCCT
A13	D14#	C12	D8#	E11	VSS	G10	VCCT
A14	D10#	C13	D20#	E12	D12#	G11	VCCT
A15	NC	C14	NC	E13	VSS	G12	VCCT
A16	NC	C15	VSS	E14	D19#	G13	VCCT
A17	NC	C16	VSS	E15	NC	G14	VCCT
A18	D23#	C17	D24#	E16	VREF	G15	VCCT
A19	D21#	C18	D26#	E17	VREF	G16	VCCT
A20	D30#	C19	VSS	E18	D34#	G17	VCCT
A21	VSS	C20	D35#	E19	VSS	G18	NC
B1	VSS	C21	D33#	E20	D43#	G19	VSS
B2	A30#	D1	A22#	E21	D45#	G20	D49#
B3	A28#	D2	VSS	F1	A16#	G21	D51#
B4	A34#	D3	A21#	F2	A18#	H1	A14#
B5	VSS	D4	A25#	F3	VSS	H2	VSS
B6	VSS	D5	A24#	F4	A17#	H3	NC
B7	VSS	D6	VSS	F5	VREF	H4	NC
B8	VSS	D7	VSS	F6	VSS	H5	NC
B9	D4#	D8	NC	F7	VSS	H6	VCCT
B10	VSS	D9	VSS	F8	VSS	H7	VSS
B11	D7#	D10	D0#	F9	VSS	H8	VCC
B12	D11#	D11	D1#	F10	VSS	H9	VSS
B13	D9#	D12	D17#	F11	VSS	H10	VCC
B14	D18#	D13	D15#	F12	VSS	H11	VSS
B15	VSS	D14	NC	F13	VSS	H12	VCC
B16	D13#	D15	D16#	F14	VSS	H13	VSS
B17	D22#	D16	NC	F15	VSS	H14	VCC
B18	VSS	D17	D25#	F16	VSS	H15	VSS
B19	D27#	D18	D28#	F17	VREF	H16	VCC
B20	D29#	D19	D32#	F18	D40#	H17	VCCT
B21	D31#	D20	D37#	F19	D36#	H18	D39#
C1	A27#	D21	D38#	F20	VSS	H19	D44#
C2	A31#	E1	A19#	F21	D42#	H20	VSS

Table 26. Signal Listing in Order by Pin/Ball Number (Sheet 2 of 3)

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
H21	D47#	K20	VSS	M20	VSS	R1	LOCK#
J1	A10#	K21	D53#	N2	VSS	R2	NC
J2	A5#	L1	A7#	N3	VSS	R3	VSS
J3	A11#	L2	PLL1	N4	VSS	R4	VSS
J4	VSS	L3	A3#	N5	TESTLO2	R5	VSS
J5	NC	L4	A6#	N6	VCCT	R6	VCCT
J6	VCCT	L5	VSS	N7	VCC	R7	VCC
J7	VCC	L6	VCCT	N8	VSS	R8	VSS
J8	VSS	L7	VCC	N9	VCC	R9	VCC
J9	VCC	L8	VSS	N10	VSS	R10	VSS
J10	VSS	L9	VCC	N11	VCC	R11	VCC
J11	VCC	L10	VSS	N12	VSS	R12	VSS
J12	VSS	L11	VCC	N13	VCC	R13	VCC
J13	VCC	L12	VSS	N14	VSS	R14	VSS
J14	VSS	L13	VCC	N15	VCC	R15	VCC
J15	VCC	L14	VSS	N16	VSS	R16	VSS
J16	VSS	L15	VCC	N17	VCCT	R17	VCCT
J17	VCCT	L16	VSS	N18	VSS	R18	D63#
J18	D41#	L17	VCCT	N19	VSS	R19	D56#
J19	VSS	L18	D48#	N20	VSS	R20	VSS
J20	D46#	L19	VSS	P1	VCC	R21	DEP3#
J21	D59#	L20	D60#	P2	CLKREF	T1	DRDY#
K1	A9#	L21	D55#	P3	NC	T2	REQ0#
K2	VSS	M2	PLL2	P4	NC	T3	VSS
K3	A4#	M3	BCLK	P5	VSS	T4	BNR#
K4	A12#	M4	NC	P6	VCCT	T5	VSS
K5	A8#	M5	NC	P7	VSS	T6	VCCT
K6	VCCT	M6	VCCT	P8	VCC	T7	VSS
K7	VSS	M7	VSS	P9	VSS	T8	VCC
K8	VCC	M8	VCC	P10	VCC	T9	VSS
K9	VSS	M9	VSS	P11	VSS	T10	VCC
K10	VCC	M10	VCC	P12	VCC	T11	VSS
K11	VSS	M11	VSS	P13	VSS	T12	VCC
K12	VCC	M12	VCC	P14	VCC	T13	VSS
K13	VSS	M13	VSS	P15	VSS	T14	VCC
K14	VCC	M14	VCC	P16	VCC	T15	VSS
K15	VSS	M15	VSS	P17	VCCT	T16	VCC
K16	VCC	M16	VCC	P18	D50#	T17	VCCT
K17	VCCT	M17	VCCT	P19	VSS	T18	VSS
K18	D52#	M18	D54#	P20	DEP6#	T19	VSS
K19	D57#	M19	D61#	P21	DEP5#	T20	D58#

Table 26. Signal Listing in Order by Pin/Ball Number (Sheet 3 of 3)

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
T21	DEP1#	V21	BINIT#	Y21	BP3#	AB21	PICD0
U1	RS0#	W1	RS2#	AA1	AERR#	AC1	VSS
U2	TRDY#	W2	RP#	AA2	RS1#	AC2	VSS
U3	DEFER#	W3	REQ3#	AA3	DBSY#	AC3	NC
U4	BPRI#	W4	VSS	AA4	VSS	AC4	VID3
U5	VREF	W5	REQ4#	AA5	NC	AC5	VSS
U6	VCCT	W6	VCCT	AA6	VCCT	AC6	VCCT
U7	VCC	W7	VCCT	AA7	VCCT	AC7	VCCT
U8	VSS	W8	VCCT	AA8	VCCT	AC8	VCCT
U9	VCC	W9	VCCT	AA9	CMOSREF	AC9	FLUSH#
U10	VSS	W10	VCCT	AA10	INIT#	AC10	VSS
U11	VCC	W11	VCCT	AA11	TCK	AC11	STPCLK#
U12	VSS	W12	VCCT	AA12	BSEL0	AC12	FERR#
U13	VCC	W13	VCCT	AA13	VSS	AC13	IGNNE#
U14	VSS	W14	VCCT	AA14	TRST#	AC14	VSS
U15	VCC	W15	VCCT	AA15	THERMDA	AC15	TDO
U16	VSS	W16	VCCT	AA16	EDGECTRLP	AC16	VSS
U17	VCCT	W17	VCCT	AA17	NC	AC17	NC
U18	D62#	W18	VSS	AA18	PICCLK	AC18	VSS
U19	DEP7#	W19	BPM1#	AA19	NC	AC19	NMI/LINT1
U20	VSS	W20	PRDY#	AA20	VSS	AC20	NC
U21	DEP2#	W21	BPM0#	AA21	BP2#	AC21	VSS
V1	HIT#	Y1	RSP#	AB1	AP0#	AD1	VSS
V2	REQ2#	Y2	AP1#	AB2	ADS#	AD2	VID0
V3	VSS	Y3	VSS	AB3	VSS	AD3	VID1
V4	REQ1#	Y4	HITM#	AB4	VID4	AD4	VID2
V5	PWRGOOD	Y5	TESTLO1	AB5	VSS	AD5	VSS
V6	VCCT	Y6	VCCT	AB6	VCCT	AD6	VCCT
V7	VCCT	Y7	VCCT	AB7	VCCT	AD7	VCCT
V8	VCCT	Y8	VCCT	AB8	VCCT	AD8	VCCT
V9	VCCT	Y9	VSS	AB9	VSS	AD9	IERR#
V10	VCCT	Y10	VSS	AB10	SMI#	AD10	A20M#
V11	VCCT	Y11	VSS	AB11	VSS	AD13	TDI
V12	VCCT	Y12	VSS	AB12	SLP#	AD14	TMS
V13	VCCT	Y13	VSS	AB13	VSS	AD15	NC
V14	VCCT	Y14	VSS	AB14	VSS	AD16	VSS
V15	VCCT	Y15	VSS	AB15	BSEL1	AD17	TESTHI
V16	VCCT	Y16	VSS	AB16	THERMDC	AD18	CMOSREF
V17	VCCT	Y17	VREF	AB17	VSS	AD19	RTTIMPEDP
V18	DEP4#	Y18	VREF	AB18	INTR/LINT0	AD20	NC
V19	VSS	Y19	VSS	AB19	RSVD	AD21	VSS
V20	DEP0#	Y20	PICD1	AB20	PREQ#		

NOTE: Ball P1 must be connected to Vcc.

Table 27. Signal Listing in Order by Signal Name (Sheet 1 of 3)

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
L3	A3#	GTL+ I/O	T4	BNR#	GTL+ I/O
K3	A4#	GTL+ I/O	AA21	BP2#	GTL+ I/O
J2	A5#	GTL+ I/O	Y21	BP3#	GTL+ I/O
L4	A6#	GTL+ I/O	W21	BPM0#	GTL+ I/O
L1	A7#	GTL+ I/O	W19	BPM1#	GTL+ I/O
K5	A8#	GTL+ I/O	U4	BPRI#	GTL+ Input
K1	A9#	GTL+ I/O	C6	BREQ0#	GTL+ I/O
J1	A10#	GTL+ I/O	AA12	BSEL0	3.3V CMOS Input
J3	A11#	GTL+ I/O	AB15	BSEL1	3.3V CMOS Input
K4	A12#	GTL+ I/O	P2	CLKREF	BCLK Reference Voltage
G1	A13#	GTL+ I/O	AA9	CMOSREF	CMOS Reference Voltage
H1	A14#	GTL+ I/O	AD18	CMOSREF	CMOS Reference Voltage
E4	A15#	GTL+ I/O	D10	D0#	GTL+ I/O
F1	A16#	GTL+ I/O	D11	D1#	GTL+ I/O
F4	A17#	GTL+ I/O	C7	D2#	GTL+ I/O
F2	A18#	GTL+ I/O	C8	D3#	GTL+ I/O
E1	A19#	GTL+ I/O	B9	D4#	GTL+ I/O
C4	A20#	GTL+ I/O	A9	D5#	GTL+ I/O
D3	A21#	GTL+ I/O	C10	D6#	GTL+ I/O
D1	A22#	GTL+ I/O	B11	D7#	GTL+ I/O
E2	A23#	GTL+ I/O	C12	D8#	GTL+ I/O
D5	A24#	GTL+ I/O	B13	D9#	GTL+ I/O
D4	A25#	GTL+ I/O	A14	D10#	GTL+ I/O
C3	A26#	GTL+ I/O	B12	D11#	GTL+ I/O
C1	A27#	GTL+ I/O	E12	D12#	GTL+ I/O
B3	A28#	GTL+ I/O	B16	D13#	GTL+ I/O
A3	A29#	GTL+ I/O	A13	D14#	GTL+ I/O
B2	A30#	GTL+ I/O	D13	D15#	GTL+ I/O
C2	A31#	GTL+ I/O	D15	D16#	GTL+ I/O
A4	A32#	GTL+ I/O	D12	D17#	GTL+ I/O
A5	A33#	GTL+ I/O	B14	D18#	GTL+ I/O
B4	A34#	GTL+ I/O	E14	D19#	GTL+ I/O
C5	A35#	GTL+ I/O	C13	D20#	GTL+ I/O
AD10	A20M#	1.5V CMOS Input	A19	D21#	GTL+ I/O
AB2	ADS#	GTL+ I/O	B17	D22#	GTL+ I/O
AA1	AERR#	GTL+ I/O	A18	D23#	GTL+ I/O
AB1	AP0#	GTL+ I/O	C17	D24#	GTL+ I/O
Y2	AP1#	GTL+ I/O	D17	D25#	GTL+ I/O
M3	BCLK	2.5V Clock Input	C18	D26#	GTL+ I/O
E6	BERR#	GTL+ I/O	B19	D27#	GTL+ I/O
V21	BINIT#	GTL+ I/O	D18	D28#	GTL+ I/O

Table 27. Signal Listing in Order by Signal Name (Sheet 2 of 3)

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
B20	D29#	GTL+ I/O	V18	DEP4#	GTL+ I/O
A20	D30#	GTL+ I/O	P21	DEP5#	GTL+ I/O
B21	D31#	GTL+ I/O	P20	DEP6#	GTL+ I/O
D19	D32#	GTL+ I/O	U19	DEP7#	GTL+ I/O
C21	D33#	GTL+ I/O	T1	DRDY#	GTL+ I/O
E18	D34#	GTL+ I/O	AA16	EDGECTRLP	GTL+ Control
C20	D35#	GTL+ I/O	AC12	FERR#	1.5V Open Drain Output
F19	D36#	GTL+ I/O	AC9	FLUSH#	1.5V CMOS Input
D20	D37#	GTL+ I/O	V1	HIT#	GTL+ I/O
D21	D38#	GTL+ I/O	Y4	HITM#	GTL+ I/O
H18	D39#	GTL+ I/O	AD9	IERR#	1.5V Open Drain Output
F18	D40#	GTL+ I/O	AC13	IGNNE#	1.5V CMOS Input
J18	D41#	GTL+ I/O	AA10	INIT#	1.5V CMOS Input
F21	D42#	GTL+ I/O	AB18	INTR/LINT0	1.5V CMOS Input
E20	D43#	GTL+ I/O	R1	LOCK#	GTL+ I/O
H19	D44#	GTL+ I/O	AC19	NMI/LINT1	1.5V CMOS Input
E21	D45#	GTL+ I/O	AA18	PICCLK	2.5V APIC Clock Input
J20	D46#	GTL+ I/O	AB21	PICD0	1.5V Open Drain I/O
H21	D47#	GTL+ I/O	Y20	PICD1	1.5V Open Drain I/O
L18	D48#	GTL+ I/O	L2	PLL1	PLL Analog Voltage
G20	D49#	GTL+ I/O	M2	PLL2	PLL Analog Voltage
P18	D50#	GTL+ I/O	W20	PRDY#	GTL+ Output
G21	D51#	GTL+ I/O	AB20	PREQ#	1.5V CMOS Input
K18	D52#	GTL+ I/O	V5	PWRGOOD	2.5V CMOS Input
K21	D53#	GTL+ I/O	T2	REQ0#	GTL+ I/O
M18	D54#	GTL+ I/O	V4	REQ1#	GTL+ I/O
L21	D55#	GTL+ I/O	V2	REQ2#	GTL+ I/O
R19	D56#	GTL+ I/O	W3	REQ3#	GTL+ I/O
K19	D57#	GTL+ I/O	W5	REQ4#	GTL+ I/O
T20	D58#	GTL+ I/O	U1	RS0#	GTL+ Input
J21	D59#	GTL+ I/O	A6	RESET#	GTL+ Input
L20	D60#	GTL+ I/O	W2	RP#	GTL+ I/O
M19	D61#	GTL+ I/O	AA2	RS1#	GTL+ Input
U18	D62#	GTL+ I/O	W1	RS2#	GTL+ Input
R18	D63#	GTL+ I/O	Y1	RSP#	GTL+ Input
AA3	DBSY#	GTL+ I/O	AB19	RSVD	Reserved
U3	DEFER#	GTL+ Input	AD19	RTTIMPEDP	GTL+ Pull-up Control
V20	DEP0#	GTL+ I/O	AB12	SLP#	1.5V CMOS Input
T21	DEP1#	GTL+ I/O	AB10	SMI#	1.5V CMOS Input
U21	DEP2#	GTL+ I/O	AC11	STPCLK#	1.5V CMOS Input
R21	DEP3#	GTL+ I/O			

Table 27. Signal Listing in Order by Signal Name (Sheet 3 of 3)

No.	Signal Name	Signal Buffer Type	No.	Signal Name	Signal Buffer Type
AA11	TCK	1.5V JTAG Clock Input	AA14	TRST#	JTAG Input
AD13	TDI	JTAG Input	AD2	VID0	Voltage Identification
AC15	TDO	JTAG Output	AD3	VID1	Voltage Identification
AD17	TESTHI	Test Input	AD4	VID2	Voltage Identification
Y5	TESTLO1	Test Input	AC4	VID3	Voltage Identification
N5	TESTLO2	Test Input	AB4	VID4	Voltage Identification
AD20	NC	Core Voltage Test Point	E5	VREF	GTL+ Reference Voltage
H4	NC	Core Voltage Test Point	E16	VREF	GTL+ Reference Voltage
AA17	NC	Core Voltage Test Point	E17	VREF	GTL+ Reference Voltage
G4	NC	Core Voltage Test Point	F5	VREF	GTL+ Reference Voltage
AA15	THERMDA	Thermal Diode Anode	F17	VREF	GTL+ Reference Voltage
AB16	THERMDC	Thermal Diode Cathode	U5	VREF	GTL+ Reference Voltage
AD14	TMS	JTAG Input	Y17	VREF	GTL+ Reference Voltage
U2	TRDY#	GTL+ Input	Y18	VREF	GTL+ Reference Voltage

Table 28. Voltage and No-Connect Pin/Ball Locations

Signal Name	Pin/Ball Numbers
NC	A15, A16, A17, C14, D8, D14, D16, E15, G2, G4, G5, G18, H3, H4, H5, J5, M4, M5, P3, P4, R2, AA5, AA17, AA19, AC3, AC17, AC20, AD15, AD20
VCC	H8, H10, H12, H14, H16, J7, J9, J11, J13, J15, K8, K10, K12, K14, K16, L7, L9, L11, L13, L15, M8, M10, M12, M14, M16, N7, N9, N11, N13, N15, P1, P8, P10, P12, P14, P16, R7, R9, R11, R13, R15, T8, T10, T12, T14, T16, U7, U9, U11, U13, U15
VCCT	G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, H6, H17, J6, J17, K6, K17, L6, L17, M6, M17, N6, N17, P6, P17, R6, R17, T6, T17, U6, U17, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, Y6, Y7, Y8, AA6, AA7, AA8, AB6, AB7, AB8, AC6, AC7, AC8, AD6, AD7, AD8
VSS	A2, A7, A8, A12, A21, B1, B5, B6, B7, B8, B10, B15, B18, C9, C11, C15, C16, C19, D2, D6, D7, D9, E3, E7, E8, E9, E10, E11, E13, E19, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F20, G3, G19, H2, H7, H9, H11, H13, H15, H20, J4, J8, J10, J12, J14, J16, J19, K2, K7, K9, K11, K13, K15, K20, L5, L8, L10, L12, L14, L16, L19, M7, M9, M11, M13, M15, M20, N2, N3, N4, N8, N10, N12, N14, N16, N18, N19, N20, P5, P7, P9, P11, P13, P15, P19, R3, R4, R5, R8, R10, R12, R14, R16, R20, T3, T5, T7, T9, T11, T13, T15, T18, T19, U8, U10, U12, U14, U16, U20, V3, V19, W4, W18, Y3, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y19, AA4, AA13, AA20, AB3, AB5, AB9, AB11, AB13, AB14, AB17, AC1, AC2, AC5, AC10, AC14, AC16, AC18, AC21, AD1, AD5, AD16, AD21

NOTE: Pin/ball P1 must be connected to Vcc.

6.0 Thermal Specifications

This section provides needed data for designing a thermal solution. The Intel Celeron Processor – LP/ULP is a surface mount PBGA-B495 package with the back of the processor die exposed and has a specified operational junction temperature (T_J) limit.

In order to achieve proper cooling of the processor, a thermal solution (e.g., heat spreader, heat pipe, or other heat transfer system) must make firm contact to the exposed processor die. The processor die must be clean before the thermal solution is attached or the processor may be damaged.

Table 29 provides the maximum Thermal Design Power (TDP_{MAX}) dissipation and the minimum and maximum T_J temperatures for the Intel Celeron Processor – LP/ULP. A thermal solution should be designed to ensure the junction temperature never exceeds these specifications. If no closed loop thermal fail-safe mechanism (processor throttling) is present to maintain TJ within specification then the thermal solution should be designed to cool the TDP_{MAX} condition. If a thermal fail-safe mechanism is present then thermal solution could possibly be designed to a typical Thermal Design Power (TDP_{TYP}). TDP_{TYP} is a thermal design power recommendation based on the power dissipation of the processor while executing publicly available software under normal operating conditions at nominal voltages. TDP_{TYP} power is lower than TDP_{MAX}. Contact your Intel field sales representative for further information.

Table 29. Power Specifications for the Intel® Celeron® Processor – LP/ULP

Symbol	Parameter	Min	TDP_{TYP}[1]	Max	Unit	Notes
TDP	Thermal Design Power at 1.10 V (300 MHz) at 1.35 V (400A MHz)		 4.2 6.5	 5.7 10.1	W	at 100° C Notes 2, 3
P_{SGNT}	Stop Grant and Auto Halt power at 1.10 V (300 MHz) at 1.35 V (400A MHz)			 0.8 1.1	W	at 50° C Note 3
P_{QS}	Quick Start and Sleep power at 1.10 V (300 MHz) at 1.35 V (400A MHz)			 0.6 0.8	W	at 50° C Note 3
P_{DSLP}	Deep Sleep power at 1.10 V (300 MHz) at 1.35 V (400A MHz)			 0.2 0.3	W	at 35° C Note 3
T_J	Junction Temperature	0		100	°C	Note 4

NOTES:
1. TDP_{TYP} is a recommendation based on the power dissipation of the processor while executing publicly available software under normal operating conditions at nominal voltages. Contact your Intel Field Sales Representative for further information. Not 100% tested.
2. TDP_{MAX} is a specification of the total power dissipation of the processor while executing a worst-case instruction mix under normal operating conditions at nominal voltages. It includes the power dissipated by all of the components within the processor. Not 100% tested. Specified by design/characterization.
3. Not 100% tested or guaranteed. The power specifications are composed of the current of the processor on the various voltage planes. These currents are measured and specified at high temperature in Table 7. These power specifications are determined by characterization of the processor currents at higher temperatures.
4. T_J is measured with the on-die thermal diode.

6.1 Thermal Diode

The Intel Celeron Processor – LP/ULP has an on-die thermal diode that can be used to monitor the die temperature (T_J). A thermal sensor located on the motherboard, or a stand-alone measurement kit, may monitor the die temperature of the processor for thermal management or instrumentation purposes. Table 30 and Table 31 provide the diode interface and specifications.

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Table 30. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	AA15	Thermal diode anode
THERMDC	AB16	Thermal diode cathode

Table 31. Thermal Diode Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		500	µA	Note 1
n	Diode Ideality Factor	1.0057	1.0080	1.0125		Notes 2, 3, 4

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized at 100° C.
3. Not 100% tested. Specified by design/characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S \cdot \left(e^{qV_D / nkT} - 1\right)$$

Where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

7.0 Processor Initialization and Configuration

7.1 Description

The Intel Celeron Processor – LP/ULP has some configuration options that are determined by hardware and some that are determined by software. The processor samples its hardware configuration at reset on the active-to-inactive transition of RESET#. Most of the configuration options for the Intel Celeron Processor – LP/ULP are identical to those of the Pentium II processor. The *Pentium® II Processor Developer's Manual* describes these configuration options. New configuration options for the Intel Celeron Processor – LP/ULP are described in the remainder of this section.

7.1.1 Quick Start Enable

The processor normally enters the Stop Grant state when the STPCLK# signal is asserted but it will enter the Quick Start state instead if A15# is sampled active on the RESET# signal's active-to-inactive transition. The Quick Start state supports snoops from the bus priority device like the Stop Grant state but it does not support symmetric master snoops nor is the latching of interrupts supported. A "1" in bit position 5 of the Power-on Configuration register indicates that the Quick Start state has been enabled.

7.1.2 System Bus Frequency

The current generation Intel Celeron Processor – LP/ULP will only function with a system bus frequency of 100 MHz. Bit positions 18 to 19 of the Power-on Configuration register indicates at which speed a processor will run. A "00" in bits [19:18] indicates a 66-MHz bus frequency, a "10" indicates a 100-MHz bus frequency, and a "01" indicates a 133-MHz bus frequency.

7.1.3 APIC Enable

If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal then the PICCLK signal can be tied to V_{SS}. Otherwise the PICD[1:0] signals must be pulled up to V_{CCT} and PICCLK must be supplied. Driving PICD0 low at reset also has the effect of clearing the APIC Global Enable bit in the APIC Base MSR. This bit is normally set when the processor is reset, but when it is cleared the APIC is completely disabled until the next reset.

7.2 Clock Frequencies and Ratios

The Intel Celeron Processor – LP/ULP uses a clock design in which the bus clock is multiplied by a ratio to produce the processor's internal (or "core") clock. Unlike some of the Intel Celeron Processor – LP/ULP, the ratio used is programmed into the processor during manufacturing. The bus ratio programmed into the processor is visible in bit positions 22 to 25 and bit 27 of the Power-on Configuration register. Table 12 shows the 5-bit codes in the Power-on Configuration register and their corresponding bus ratios.

8.0 Processor Interface

8.1 Alphabetical Signal Reference

8.1.1 A[35:3]# (I/O - GTL+)

The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal.

On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4.0 of this document and the *Pentium® II Processor Developer's Manual* for details.

8.1.2 A20M# (I - 1.5 V Tolerant)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.

8.1.3 ADS# (I/O - GTL+)

The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.4 AERR# (I/O - GTL+)

The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.

8.1.5 AP[1:0]# (I/O - GTL+)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered

signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.

8.1.6 BCLK (I - 2.5 V Tolerant)

The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

8.1.7 BERR# (I/O - GTL+)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the Intel Celeron Processor – LP/ULP do not observe assertions of the BERR# signal.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Asserted optionally by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

8.1.8 BINIT# (I/O - GTL+)

The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

8.1.9 BNR# (I/O - GTL+)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

8.1.10 BP[3:2]# (I/O - GTL+)

The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.

8.1.11 BPM[1:0]# (I/O - GTL+)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

8.1.12 BPRI# (I - GTL+)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.

8.1.13 BREQ0# (I/O - GTL+)

The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal.

During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#. Optionally, this signal may be grounded with a 10ohm resistor.

8.1.14 BSEL[1:0] (I – 3.3 V Tolerant)

The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 32 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the Intel Celeron Processor – LP/ULP is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with “01” then the processor is not guaranteed to function properly.

Table 32. BSEL[1:0] Encoding

BSEL[1:0]	System Bus Frequency
00	66 MHz
01	100 MHz
10	Reserved
11	133 MHz

8.1.15 CLKREF (Analog)

The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25 V from the 2.5-V supply.

8.1.16 CMOSREF (Analog)

The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5 V or 3.3 V). This signal must be provided with a DC voltage that meets the $V_{CMOSREF}$ specification from Table 10.

8.1.17 D[63:0]# (I/O - GTL+)

The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

8.1.18 DBSY# (I/O - GTL+)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.19 DEFER# (I - GTL+)

The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.20 DEP[7:0]# (I/O - GTL+)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.

8.1.21 DRDY# (I/O - GTL+)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.22 EDGCTRLP (Analog)

The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to V_{SS} with a 110-Ω, 1% resistor.

8.1.23 FERR# (O - 1.5 V Tolerant Open-drain)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.

8.1.24 FLUSH# (I - 1.5 V Tolerant)

When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted.

On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

8.1.25 HIT# (I/O - GTL+), HITM# (I/O - GTL+)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

8.1.26 IERR# (O - 1.5 V Tolerant Open-drain)

The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.

8.1.27 IGNNE# (I - 1.5 V Tolerant)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.

8.1.28 INIT# (I - 1.5 V Tolerant)

The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input.

If INIT# is sampled active on RESET#’s active-to-inactive transition, then the processor executes its built-in self test (BIST).

8.1.29 INTR (I - 1.5 V Tolerant)

The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

8.1.30 LINT[1:0] (I - 1.5 V Tolerant)

The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs.

Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.

8.1.31 LOCK# (I/O - GTL+)

The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.

8.1.32 NMI (I - 1.5 V Tolerant)

The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

8.1.33 PICCLK (I - 2.5 V Tolerant)

The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.

8.1.34 PICD[1:0] (I/O - 1.5 V Tolerant Open-drain)

The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.

8.1.35 PLL1, PLL2 (Analog)

The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.

8.1.36 PRDY# (O - GTL+)

The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.

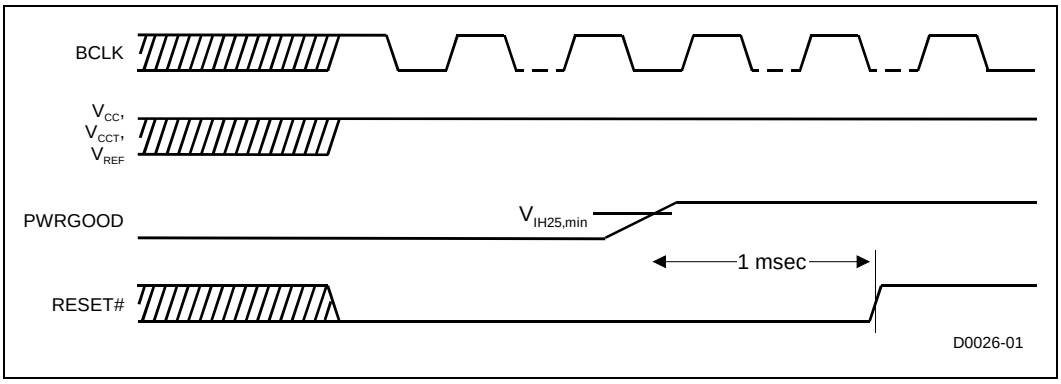
8.1.37 PREQ# (I - 1.5 V Tolerant)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.

8.1.38 PWRGOOD (I - 2.5 V Tolerant)

PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (V_{CC}, V_{CCT}, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5 V) state. Figure 22 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 14 on page 27 and be followed by a 1 ms RESET# pulse.

Figure 22. PWRGOOD Relationship at Power On



The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

8.1.39 REQ[4:0]# (I/O - GTL+)

The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.

8.1.40 RESET# (I - GTL+)

Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 ms after V_{CC} and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω 1% terminating resistor connected to V_{CCT} is required.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4.0 and in the *Pentium® II Processor Developer's Manual*.

Unless its outputs are three-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.41 RP# (I/O - GTL+)

The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

8.1.42 RS[2:0]# (I - GTL+)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.43 RSP# (I - GTL+)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus.

A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

8.1.44 RSVD (TBD)

The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.

8.1.45 RTTIMPEDP (Analog)

The RTTIMPEDP (R_{TT} Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to V_{SS} with a 56.2-Ω, 1% resistor.

8.1.46 SLP# (I - 1.5 V Tolerant)

The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.

8.1.47 SMI# (I - 1.5 V Tolerant)

The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

8.1.48 STPCLK# (I - 1.5 V Tolerant)

The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.

8.1.49 TCK (I - 1.5 V Tolerant)

The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

8.1.50 TDI (I - 1.5 V Tolerant)

The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.

8.1.51 TDO (O - 1.5 V Tolerant Open-drain)

The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.

8.1.52 TESTHI (I - 1.5 V Tolerant)

The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.

8.1.53 TESTLO[2:1] (I - 1.5 V Tolerant)

The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.

8.1.54 THERMDA, THERMDC (Analog)

The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.

8.1.55 TMS (I - 1.5 V Tolerant)

The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.

8.1.56 TRDY# (I - GTL+)

The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.

8.1.57 TRST# (I - 1.5 V Tolerant)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The Intel Celeron Processor – LP/ULP do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

8.1.58 VID[4:0] (O – Open-drain)

The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to V_{SS} on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on Intel Celeron Processor – LP/ULP. The voltage encoded by VID[4:0] is defined in Table 33. A “1” in this table refers to an open pin/ball and a “0” refers to a short to VSS. The power supply must provide the requested voltage or disable itself.

Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a “1” in Table 33 implies that the corresponding VID ball is depopulated, while a “0” implies that the corresponding VID ball is not depopulated.

Table 33. Voltage Identification Encoding

VID[4:0]	V_{CC}	VID[4:0]	V_{CC}	VID[4:0]	V_{CC}	VID[4:0]	V_{CC}
00000	2.00	01000	1.60	10000	1.275	11000	1.075
00001	1.95	01001	1.55	10001	1.250	11001	1.050
00010	1.90	01010	1.50	10010	1.225	11010	1.025
00011	1.85	01011	1.45	10011	1.200	11011	1.000
00100	1.80	01100	1.40	10100	1.175	11100	0.975
00101	1.75	01101	1.35	10101	1.150	11101	0.950
00110	1.70	01110	1.30	10110	1.125	11110	0.925
00111	1.65	01111	No CPU	10111	1.100	11111	No CPU

8.1.59 VREF (Analog)

The VREF (GTL+ Reference Voltage) signal provides a DC level reference voltage for the GTL+ input buffers. A voltage divider should be used to divide V_{CCT} by $^{2}/_{3}$. Resistor values of 1.00 KΩ and 2.00 KΩ are recommended. Decouple the VREF signal with three 0.1-µF high frequency capacitors close to the processor.

8.2 Signal Summaries

Table 34 through Table 37 list the attributes of the processor input, output, and I/O signals.

Table 34. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS	Always
BCLK	High	—	System Bus	Always
BPRI#	Low	BCLK	System Bus	Always
BSEL[1:0]	High	Asynch	Implementation	Always
DEFER#	Low	BCLK	System Bus	Always
FLUSH#	Low	Asynch	CMOS	Always
IGNNE#	Low	Asynch	CMOS	Always
INIT#	Low	Asynch	System Bus	Always
INTR	High	Asynch	CMOS	APIC disabled mode
LINT[1:0]	High	Asynch	APIC	APIC enabled mode
NMI	High	Asynch	CMOS	APIC disabled mode
PICCLK	High	—	APIC	Always
PREQ#	Low	Asynch	Implementation	Always
PWRGOOD	High	Asynch	Implementation	Always
RESET#	Low	BCLK	System Bus	Always
RS[2:0]#	Low	BCLK	System Bus	Always
RSP#	Low	BCLK	System Bus	Always
SLP#	Low	Asynch	Implementation	Stop Grant state
SMI#	Low	Asynch	CMOS	Always
STPCLK#	Low	Asynch	Implementation	Always
TCK	High	—	JTAG	
TDI		TCK	JTAG	
TMS		TCK	JTAG	
TRDY#	Low	BCLK	System Bus	Response phase
TRST#	Low	Asynch	JTAG	

Table 35. Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	Open-drain
IERR#	Low	Asynch	Open-drain
PRDY#	Low	BCLK	Implementation
TDO	High	TCK	JTAG
VID[4:0]	High	Asynch	Implementation

Table 36. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	System Bus	ADS#, ADS#+1
ADS#	Low	BCLK	System Bus	Always
AP[1:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
BREQ0#	Low	BCLK	System Bus	Always
BP[3:2]#	Low	BCLK	System Bus	Always
BPM[1:0]#	Low	BCLK	System Bus	Always
D[63:0]#	Low	BCLK	System Bus	DRDY#
DBSY#	Low	BCLK	System Bus	Always
DEP[7:0]#	Low	BCLK	System Bus	DRDY#
DRDY#	Low	BCLK	System Bus	Always
LOCK#	Low	BCLK	System Bus	Always
REQ[4:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
RP#	Low	BCLK	System Bus	ADS#, ADS#+1

Table 37. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	System Bus	ADS#+3
BERR#	Low	BCLK	System Bus	Always
BINIT#	Low	BCLK	System Bus	Always
BNR#	Low	BCLK	System Bus	Always
HIT#	Low	BCLK	System Bus	Always
HITM#	Low	BCLK	System Bus	Always
PICD[1:0]	High	PICCLK	APIC	Always

9.0 PLL RLC Filter Specification

9.1 Introduction

The Intel Celeron Processor – LP/ULP processor has an internal PLL clock generator, which are analog in nature and require quiet power supplies for minimum jitter. Jitter is detrimental to a system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). For the Pentium II Processor – Low Power (mobile Pentium II processor), the power supply filter was specified as an external LC network. This remains largely the same for the Intel Celeron Processor – LP/ULP. However, due to increased current flow, the value of the inductor has to be reduced, thereby requiring new components. The general desired topology is shown in Figure 4. Excluded from the external circuitry are parasitics associated with each component.

9.2 Filter Specification

The function of the filter is two fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter.

The AC low-pass specification, with input at V_{CCT} and output measured across the capacitor, is as follows:

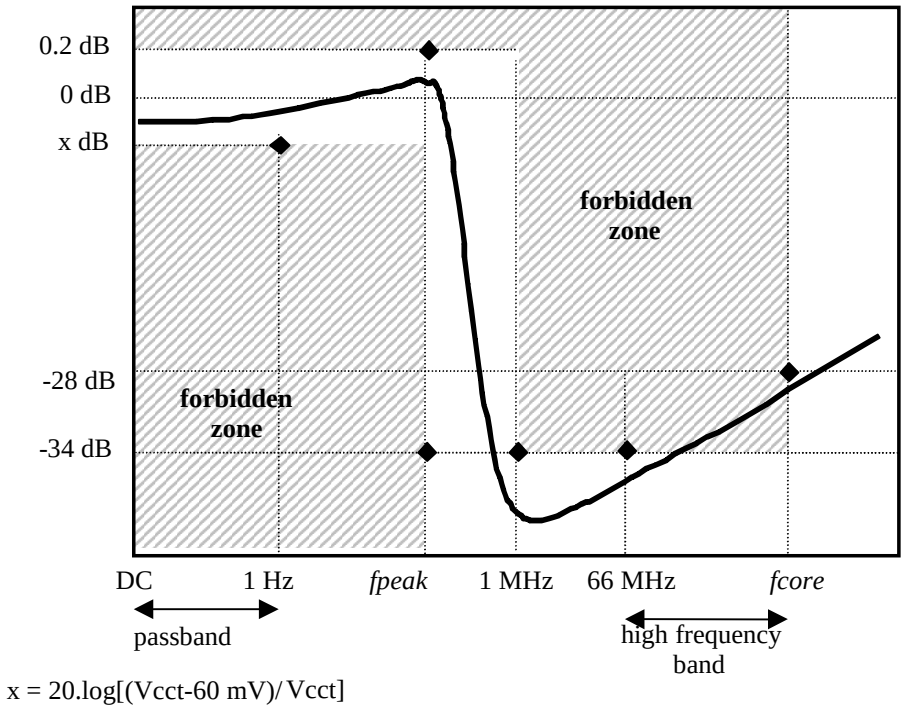
- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency

The filter specification (AC) is graphically shown in Figure 23.

Other requirements:

- Use a shielded type inductor to minimize magnetic pickup
- The filter should support a DC current of at least 30 mA
- The DC voltage drop from V_{CCT} to PLL1 should be less than 60 mV, which in practice implies series resistance of less than 2Ω. This also means that the pass band (from DC to 1Hz) attenuation below 0.5 dB is for V_{CCT} = 1.1 V and below 0.35 dB for V_{CCT} = 1.5 V.

Figure 23. PLL Filter Specifications



$x = 20.\log[(Vcct-60\ mV)/Vcct]$

NOTES:
Diagram is not to scale
No specification for frequencies beyond f_{core}
F_{peak}, if existent, should be less than 0.05 MHz

9.3 Recommendation for Low Power Systems

The following LC components are recommended. The tables will be updated as other suitable components and specifications are identified.

Table 38. PLL Filter Inductor Recommendations

Inductor	Part Number	Value	Tol	SRF	Rated I	DCR	Min Damping R needed
L1	TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56Ω (1Ω max)	0Ω
L2	Murata LQG21N4R7K10	4.7 µH	10%	47 MHz	30 mA	0.7Ω (+/-50%)	0Ω
L3	Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3Ω max	0.2Ω (assumed)

NOTE: Minimum damping resistance is calculated from 0.35Ω – DCR_{min}. From vendor provided data, L1 and L2 DCR_{min} is 0.4 Ω and 0.5 Ω respectively, qualifying them for zero required trace resistance. DCR_{min} for L3 is not known and is assumed to be 0.15 Ω. There may be other vendors who might provide parts of equivalent characteristics and the OEMs should consider doing their own testing for selecting their own vendors.

Table 39. PLL Filter Capacitor Recommendations

Capacitor	Part Number	Value	Tolerance	ESL	ESR
C1	Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
C2	AVX TPSD336M020S0200	33 µF	20%	unknown	0.2 Ω

NOTE: There may be other vendors who might provide parts of equivalent characteristics and the OEMs should consider doing their own testing for selecting their own vendors.

Table 40. PLL Filter Resistor Recommendations

Resistor	Part Number	Value	Tolerance	Power
R1	various	1 Ω	10%	1/16 W

To satisfy damping requirements, total series resistance in the filter (from V_{CCT} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 Ω, which precludes using L2 and possibly L1.

Other routing requirements:

- The capacitor should be close to the PLL1 and PLL2 pins, with less than 0.1 Ω per route (These routes do not count towards the minimum damping resistance requirement).
- The PLL2 route should be parallel and next to the PLL1 route (minimize loop area).
- The inductor should be close to the capacitor; any routing resistance should be inserted between VCCT and the inductor.
- Any discrete resistor should be inserted between VCCT and the inductor.

9.4 Comments

- A magnetically shielded inductor protects the circuit from picking up external flux noise. This should provide better timing margins than with an unshielded inductor.
- A discrete or routed resistor is required because the LC filter by nature has an under-damped response, which can cause resonance at the LC pole. Noise amplification at this band, although not in the PLL-sensitive spectrum, could cause a fatal headroom reduction for analog circuitry. The resistor serves to dampen the response. Systems with tight space constraints should consider a discrete resistor to provide the required damping resistance. Too large of a damping resistance can cause a large IR drop, which means less analog headroom and lower frequency.
- Ceramic capacitors have very high self-resonance frequencies, but they are not available in large capacitance values. A high self-resonant frequency coupled with low ESL/ESR is crucial for sufficient rejection in the PLL and high frequency band. The recommended tantalum capacitors have acceptably low ESR and ESL.
- The capacitor must be close to the PLL1 and PLL2 pins, otherwise the value of the low ESR tantalum capacitor is wasted. Note the distance constraint should be translated from the 0.1 Ω requirement.

The mobile Pentium II processor LC filter cannot be used with the Intel Celeron Processor – LP/ULP. The larger inductor of the old LC filter imposes a lower current rating. Due to increased current requirements for the Intel Celeron Processor – LP/ULP, a lower value inductor is required.