# *4M X 72 Bits SDRAM Unbuffered DIMM with ECC (PC100)*

## FEATURES

- PC100 compliant ($t_{CYC}$=10ns@CL2) and Intel Qualified
- Burst Mode Operation
- Auto and self refresh capability (4096 cycles/64ms refresh)
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  - Latency (access from column address)
  - Burst Length (1, 2, 4, 8, and full page)
  - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- ECC Optimized
- Serial Presence Detect with EEPROM

## GENERAL DESCRIPTION

The SimpleTech INT72U6D4M4H-A10DV is a 4M x 72 bits Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM). This module consists of five CMOS 1M x 16 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP-II packages mounted on a 168-pin glass epoxy substrate. A serial EEPROM using the two pin $I^2C$ protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.33µF and 0.1µF are mounted for the SDRAMs and the EEPROM.

The module has gold edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for unbuffered signals and 3.3V power supply.

The module is PC100 compliant and Intel Qualified. The module uses NEC µPD4564163G5-A80 SDRAM components.

## PIN CONFIGURATION

### Pin Symbols

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 25 | NC | 49 | $V_{DD}$ | 73 | $V_{DD}$ | 97 | $DQ_{41}$ | 121 | $A_9$ | 145 | NC |
| 2 | $DQ_0$ | 26 | $V_{DD}$ | 50 | NC | 74 | $DQ_{28}$ | 98 | $DQ_{42}$ | 122 | $BA_0$ | 146 | NC |
| 3 | $DQ_1$ | 27 | $\overline{WE}$ | 51 | NC | 75 | $DQ_{29}$ | 99 | $DQ_{43}$ | 123 | $A_{11}$ | 147 | NC |
| 4 | $DQ_2$ | 28 | $DQMB_0$ | 52 | $CB_2$ | 76 | $DQ_{30}$ | 100 | $DQ_{44}$ | 124 | $V_{DD}$ | 148 | $V_{SS}$ |
| 5 | $DQ_3$ | 29 | $DQMB_1$ | 53 | $CB_3$ | 77 | $DQ_{31}$ | 101 | $DQ_{45}$ | 125 | $CLK_1$* | 149 | $DQ_{53}$ |
| 6 | $V_{DD}$ | 30 | $\overline{S_0}$ | 54 | $V_{SS}$ | 78 | $V_{SS}$ | 102 | $V_{DD}$ | 126 | $A_{12}$* | 150 | $DQ_{54}$ |
| 7 | $DQ_4$ | 31 | DU | 55 | $DQ_{16}$ | 79 | $CLK_2$ | 103 | $DQ_{46}$ | 127 | $V_{SS}$ | 151 | $DQ_{55}$ |
| 8 | $DQ_5$ | 32 | $V_{SS}$ | 56 | $DQ_{17}$ | 80 | NC | 104 | $DQ_{47}$ | 128 | $CKE_0$ | 152 | $V_{SS}$ |
| 9 | $DQ_6$ | 33 | $A_0$ | 57 | $DQ_{18}$ | 81 | NC | 105 | $CB_4$ | 129 | $\overline{S_3}$* | 153 | $DQ_{56}$ |
| 10 | $DQ_7$ | 34 | $A_2$ | 58 | $DQ_{19}$ | 82 | SDA | 106 | $CB_5$ | 130 | $DQMB_6$ | 154 | $DQ_{57}$ |
| 11 | $DQ_8$ | 35 | $A_4$ | 59 | $V_{DD}$ | 83 | SCL | 107 | $V_{SS}$ | 131 | $DQMB_7$ | 155 | $DQ_{58}$ |
| 12 | $V_{SS}$ | 36 | $A_6$ | 60 | $DQ_{20}$ | 84 | $V_{DD}$ | 108 | NC | 132 | $A_{13}$* | 156 | $DQ_{59}$ |
| 13 | $DQ_9$ | 37 | $A_8$ | 61 | NC | 85 | $V_{SS}$ | 109 | NC | 133 | $V_{DD}$ | 157 | $V_{DD}$ |
| 14 | $DQ_{10}$ | 38 | $A_{10}$/AP | 62 | NC | 86 | $DQ_{32}$ | 110 | $V_{DD}$ | 134 | NC | 158 | $DQ_{60}$ |
| 15 | $DQ_{11}$ | 39 | $BA_1$ | 63 | $CKE_1$* | 87 | $DQ_{33}$ | 111 | $\overline{CAS}$ | 135 | NC | 159 | $DQ_{61}$ |
| 16 | $DQ_{12}$ | 40 | $V_{DD}$ | 64 | $V_{SS}$ | 88 | $DQ_{34}$ | 112 | $DQMB_4$ | 136 | $CB_6$ | 160 | $DQ_{62}$ |
| 17 | $DQ_{13}$ | 41 | $V_{DD}$ | 65 | $DQ_{21}$ | 89 | $DQ_{35}$ | 113 | $DQMB_5$ | 137 | $CB_7$ | 161 | $DQ_{63}$ |
| 18 | $V_{DD}$ | 42 | $CLK_0$ | 66 | $DQ_{22}$ | 90 | $V_{DD}$ | 114 | $\overline{S_1}$* | 138 | $V_{SS}$ | 162 | $V_{SS}$ |
| 19 | $DQ_{14}$ | 43 | $V_{SS}$ | 67 | $DQ_{23}$ | 91 | $DQ_{36}$ | 115 | $\overline{RAS}$ | 139 | $DQ_{48}$ | 163 | $CLK_3$* |
| 20 | $DQ_{15}$ | 44 | DU | 68 | $V_{SS}$ | 92 | $DQ_{37}$ | 116 | $V_{SS}$ | 140 | $DQ_{49}$ | 164 | NC |
| 21 | $CB_0$ | 45 | $\overline{S_2}$ | 69 | $DQ_{24}$ | 93 | $DQ_{38}$ | 117 | $A_1$ | 141 | $DQ_{50}$ | 165 | $SA_0$ |
| 22 | $CB_1$ | 46 | $DQMB_2$ | 70 | $DQ_{25}$ | 94 | $DQ_{39}$ | 118 | $A_3$ | 142 | $DQ_{51}$ | 166 | $SA_1$ |
| 23 | $V_{SS}$ | 47 | $DQMB_3$ | 71 | $DQ_{26}$ | 95 | $DQ_{40}$ | 119 | $A_5$ | 143 | $V_{DD}$ | 167 | $SA_2$ |
| 24 | NC | 48 | DU | 72 | $DQ_{27}$ | 96 | $V_{SS}$ | 120 | $A_7$ | 144 | $DQ_{52}$ | 168 | $V_{DD}$ |

* Not used in this module.

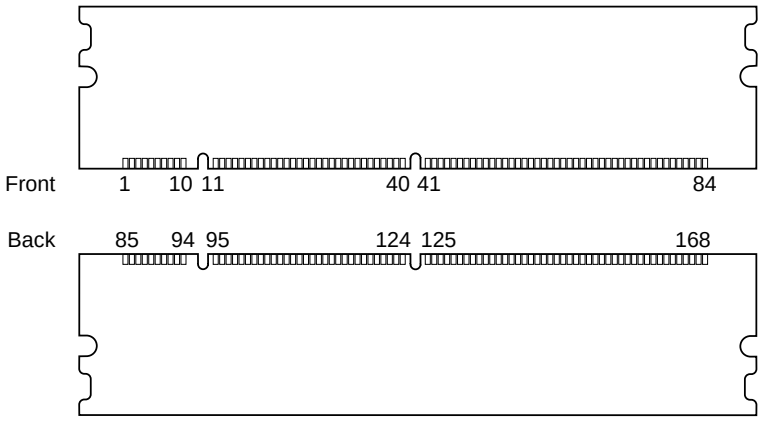
continued on the next page

## PIN CONFIGURATION *(continued)*

### Pin Functions

| Pin Symbol | Pin Function |
|---|---|
| $A_0$-$A_{10}$/AP, $A_{11}$ | Address Inputs |
| $BA_0$, $BA_1$ | Select Bank |
| $DQ_0$-$DQ_{63}$ | Data In/Out |
| $CB_0$-CB7 | Check Bit |
| $\overline{WE}$ | Write Enable |
| $CLK_0$, $CLK_2$ | Clock Input |
| $CKE_0$, $CKE_1$ | Clock Enable Input |
| $\overline{RAS}$ | Row Adress Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $DQMB_0$-$DQMB_7$ | Data Input/Output Mask |
| $\overline{S}_0$, $\overline{S}_2$ | Chip Select Input |
| SDA | Serial Address/Data I/O |
| SCL | Serial Clock |
| $SA_0$-$SA_2$ | Address in EEPROM |
| $V_{DD}$ | Power (+3.3V) |
| $V_{SS}$ | Ground |
| NC | No Connection |
| DU | Don't Use |

### Pin Arrangement

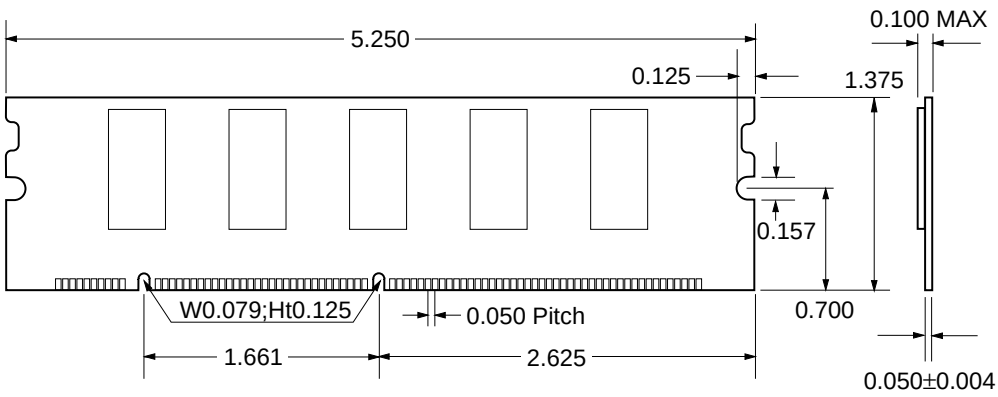



## ORDERING INFORMATION

| Part Number | PC100 100MHz Parameters | | | | |
|---|---|---|---|---|---|
| | CL | $t_{RCD}$ | $t_{RP}$ | $t_{RC}$ | Units |
| INT72U6D4M4H-A10DV | 2 | 2 | 2 | 7 | clks |

## PACKAGE DIMENSIONS

Units: Inches

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TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

## SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: $I^2C$; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

| Byte # | Function Described | Function Supported | Hex Value |
|---|---|---|---|
| 0 | # of bytes written into serial memory at module manufacturer | 128 bytes | 80h |
| 1 | Total # of bytes of SPD memory device | 256Bytes (2K-bit) | 08h |
| 2 | Fundamental memory type | SDRAM | 04h |
| 3 | # of row addresses on this assembly | 12 | 0Ch |
| 4 | # of column addresses on this assembly | 8 | 08h |
| 5 | # of module banks on this assembly | 1 bank | 01h |
| 6 | Data width of this assembly | 72 bits | 48h |
| 7 | …Data width of this assembly (continued) | — | 00h |
| 8 | Voltage interface standard of this assembly | LVTTL | 01h |
| 9 | SDRAM cycle time at CL=3 ($t_{CYC}$) | 10ns | A0h |
| 10 | SDRAM access time from clock at CL=3 ($t_{AC}$) | 6ns | 60h |
| 11 | DIMM configuration type | ECC | 02h |
| 12 | Refresh rate/type | 15.625µs, Self-refresh | 80h |
| 13 | SDRAM width | 16 bits | 10h |
| 14 | Error Checking DRAM data width | x8 | 08h |
| 15 | Min. CLK delay for back-to-back rand. col. addr. | $t_{CCD}$=1 CLK | 01h |
| 16 | SDRAM device attributes: burst lengths supported | 1,2,4,8, and full page | 8Fh |
| 17 | SDRAM device attributes: # of banks on SDRAM device | 4 banks | 04h |
| 18 | SDRAM device attributes: CAS latency | CAS latency = 2,3 | 06h |
| 19 | SDRAM device attributes: CS latency | CS latency = 0 | 01h |
| 20 | SDRAM device attributes: Write latency | Write Latency = 0 | 01h |
| 21 | SDRAM module attributes | non-PLL, non-buff., non-reg. | 00h |
| 22 | SDRAM device attributes: general | $V_{CC}$10%, B/R, S/W, P/A, A/P | 0Eh |
| 23 | Minimum clock cycle time at CL=2 ($t_{CYC}$) | 10ns | A0h |
| 24 | Max. data access time form clock at CL=2 ($t_{AC}$) | 6ns | 60h |
| 25 | Minimum clock cycle time at CL=1 ($t_{CYC}$) | — | 00h |
| 26 | Max. data access time from clock at CL=1 ($t_{AC}$) | — | 00h |
| 27 | Minimum row precharge time ($t_{RP}$) | 20ns | 14h |
| 28 | Minimum row active to row active delay ($t_{RRD}$) | 20ns | 14h |
| 29 | Minumum RAS to CAS ($t_{RCD}$) | 20ns | 14h |
| 30 | Minumum RAS pulse width ($t_{RAS}$) | 50ns | 32h |
| 31 | Module bank density | 32MB | 08h |
| 32 | Min. command and address signal setup time ($t_{AS}$) | 2ns | 20h |
| 33 | Min. command and address signal hold time ($t_{AH}$) | 1ns | 10h |
| 34 | Min. data signal input setup time ($t_{DS}$) | 2ns | 20h |

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| Byte # | Function Described | Function Supported | Hex Value |
|---|---|---|---|
| 35 | Min. data signal input hold time ($t_{DH}$) | 1ns | 10h |
| 36-61 | Superset information (may be used in future) | — | 00h |
| 62 | SPD revision | 1.2 | 12h |
| 63 | Checksum for bytes 0-62 | JEDEC calculation | xxh |
| 64 | Manufacturer's JEDEC ID code per JEP-106E | Continuation code | 7Fh |
| 65 | Man. JEDEC ID code (continued) | SimpleTech's ID | A8h |
| 66-71 | | | 00h |
| 72 | Manufacturing location | SimpleTech USA | 01h |
| 73-90 | Manufacturer's part number | | xxh |
| 91 | Revision code of PCB | Eng(00),RevA(01),RevB(02) | 01h |
| 92 | | | 00h |
| 93 | Manufacturing date | Year (BCD) | yy |
| 94 | | Calender Week (BCD) | ww |
| 95 | Assembly serial number | Tester number | ss |
| 96 | | Serial number (bits 7-0) | ss |
| 97 | | Serial number (bits 15-8) | ss |
| 98 | | Serial number (bits 23-16) | ss |
| 99-125 | Manufacturer's specific data | | xxh |
| 126 | Intel specification frequency | 100MHz | 64h |
| 127 | Intel specification details | Detailed 100MHz Info | AFh |

## FUNCTIONAL BLOCK DIAGRAM