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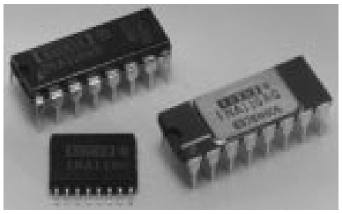


INA110

Fast-Settling FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4µs to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2µV/°C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

APPLICATIONS

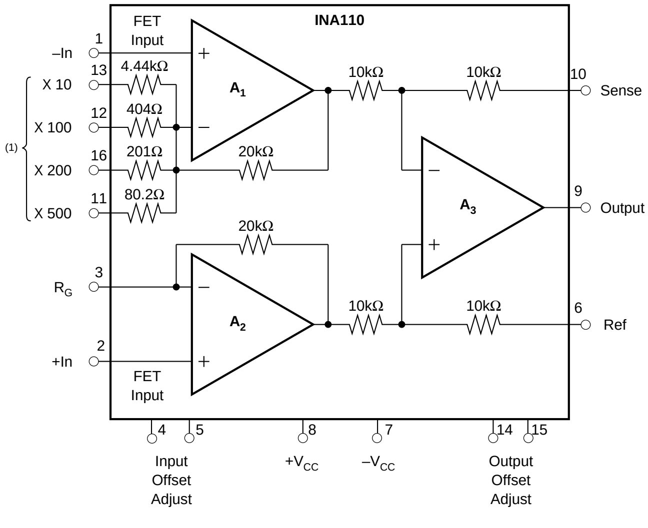
- MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
- FAST DIFFERENTIAL PULSE AMPLIFIER
- HIGH SPEED GAIN BLOCK
- AMPLIFICATION OF HIGH IMPEDANCE SOURCES

DESCRIPTION

The INA110 is a versatile monolithic FET-input instrumentation amplifier. Its current-feedback circuit topology and laser trimmed input stage provide excellent dynamic performance and accuracy. The INA110 settles in 4µs to 0.01%, making it ideal for high speed or multiplexed-input data acquisition systems.

Internal gain-set resistors are provided for gains of 1, 10, 100, 200, and 500V/V. Inputs are protected for differential and common-mode voltages up to $\pm V_{CC}$. Its very high input impedance and low input bias current make the INA110 ideal for applications requiring input filters or input protection circuitry.

The INA110 is available in 16-pin plastic and ceramic DIPs, and in the SOL-16 surface-mount package. Military, industrial and commercial temperature range grades are available.



NOTE: (1) Connect to R_G for desired gain.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-645E

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SBOS147

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, and R_L = 2kΩ, unless otherwise specified.

		INA110AG			INA110BG, SG			INA110KP, KU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN											
Range of Gain		1		800	*		*	*		*	V/V
Gain Equation$^{(1)}$			*		G = 1 + [40k/(R_G + 50Ω)]				*		V/V
Gain Error, DC: G = 1			0.002	0.04		*	0.02		*	*	%
G = 10			0.01	0.1		0.005	0.05		*	*	%
G = 100			0.02	0.2		0.01	0.1		*	*	%
G = 200			0.04	0.4		0.02	0.2		*	*	%
G = 500			0.1	1		0.05	0.5		*	*	%
Gain Temp. Coefficient: G = 1			±3	±20		*	±10		*		ppm/°C
G = 10			±4	±20		±2	±10		*		ppm/°C
G = 100			±6	±40		±3	±20		*		ppm/°C
G = 200			±10	±60		±5	±30		*		ppm/°C
G = 500			±25	±100		±10	±50		*		ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005		*	*	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005		*	*	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01		*	*	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01		*	*	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02		*	*	% of FS
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10	±12.7		*	*		*	*		V
Current	Over Temperature	±5	±25		*	*		*	*		mA
Short-Circuit Current			±25			*			*		mA
Capacitive Load	Stability		5000			*			*		pF
INPUT OFFSET VOLTAGE$^{(2)}$											
Initial Offset: G, P			±(100 + 1000/G)	±(500 + 5000/G)		±(50 + 600/G)	±(250 + 3000/G)		*	*	µV
U									±(200 + 2000/G)	±(1000 + 5000/G)	µV
vs Temperature			±(2 + 20/G)	±(5 + 100/G)		±(1 + 10/G)	±(2 + 50/G)		*		µV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4 + 60/G)	±(30 + 300/G)		±(2 + 30/G)	±(10 + 180/G)		*	*	µV/V
BIAS CURRENT											
Initial Bias Current	Each Input		20	100		10	50		*	*	pA
Initial Offset Current			2	50		1	25		*	*	pA
Impedance: Differential			$5\text{x}10^{12} \parallel 6$			*			*		Ω ∥ pF
Common-Mode			$2\text{x}10^{12} \parallel 1$			*			*		Ω ∥ pF
VOLTAGE RANGE	V_{IN} Diff. = 0V$^{(3)}$										
Range, Linear Response		±10	±12					*	*		V
CMR with 1kΩ Source Imbalance:											
G = 1	DC	70	90		80	100		*	*		dB
G = 10	DC	87	104		96	112		*	*		dB
G = 100	DC	100	110		106	116		*	*		dB
G = 200	DC	100	110		106	116		*	*		dB
G = 500	DC	100	110		106	116		*	*		dB
INPUT NOISE$^{(4)}$											
Voltage, f_O = 10kHz			10			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*			*		µVp-p
Current, f_O = 10kHz			1.8			*			*		fA/√Hz
OUTPUT NOISE$^{(4)}$											
Voltage, f_O = 10kHz			65			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz			8			*			*		µVp-p
DYNAMIC RESPONSE											
Small Signal: G = 1	–3dB		2.5			*			*		MHz
G = 10			2.5			*			*		MHz
G = 100			470			*			*		kHz
G = 200			240			*			*		kHz
G = 500			100			*			*		kHz
Full Power	V_{OUT} = ±10V, G = 2 to 100	190	270		*	*			*	*	kHz
Slew Rate	G = 2 to 100	12	17		*	*			*	*	V/µs
Settling Time:											
0.1%, G = 1	V_O = 20V Step		4			*			*		µs
G = 10			2			*			*		µs
G = 100			3			*			*		µs
G = 200			5			*			*		µs
G = 500			11			*			*		µs

SPECIFICATIONS (CONT)

ELECTRICAL

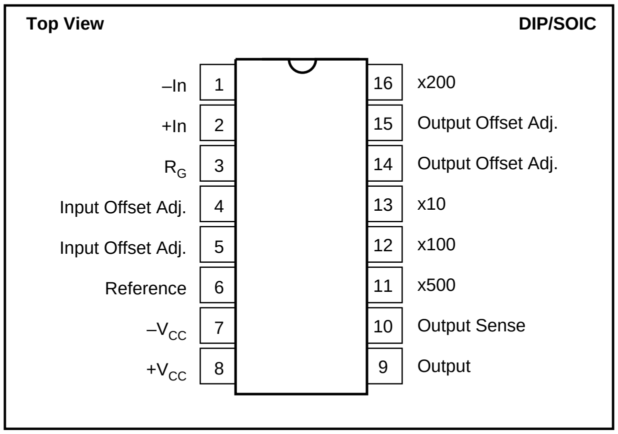
At +25°C, $\pm V_{CC}$ 15VDC, and $R_L = 2K\Omega$, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time:											
0.01%,G = 1	V_O = 20V Step		5	12.5		*	*		*		µs
G = 10			3	7.5		*	*		*		µs
G = 100			4	7.5		*	*		*		µs
G = 200			7	12.5		*	*		*		µs
G = 500			16	25		*	*		*		µs
Recovery(5)	50% Overdrive		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±3	±4.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: A, B, K		–25		+85	*		*	0		+70	°C
S					–55		+125				°C
Operation		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–40		+85	°C
θ_{JA}			100			*			*		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12 and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_{CC}$
Operating Temperature Range: G	–55°C to +125°C
P, U	–25°C to +85°C
Storage Temperature Range: G	–65°C to +150°C
P, U	–40°C to +85°C
Lead Temperature (soldering, 10s): G, P	+300°C
(soldering, 3s): U	+260°C
Output Short Circuit Duration	Continuous to Common

PACKAGE INFORMATION

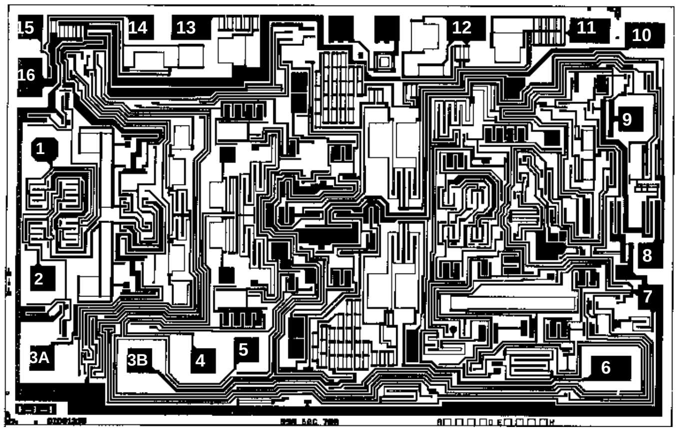
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA110AG	16-Pin Ceramic DIP	109
INA110BG	16-Pin Ceramic DIP	109
INA110SG	16-Pin Ceramic DIP	109
INA110KP	16-Pin Plastic DIP	180
INA110KU	SOL-16 SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA110AG	16-Pin Ceramic DIP	–25°C to +85°C
INA110BG	16-Pin Ceramic DIP	–25°C to +85°C
INA110SG	16-Pin Ceramic DIP	–55°C to +125°C
INA110KP	16-Pin Plastic DIP	0°C to +70°C
INA110KU	SOL-16 SOIC	0°C to +70°C

DICE INFORMATION



INA110 DIE TOPOGRAPHY

PAD	FUNCTION
1	–In
2	+In
3A,3B	R_G (connect both)
4	Input Offset Adjust
5	Input Offset Adjust
6	Reference
7	$-V_{CC}$
8	$+V_{CC}$
9	Output
10	Output Sense
11	x500
12	x100
13	x10
14	Output Offset Adjust
15	Output Offset Adjust
16	x200

Pads 3A and 3B must be connected.

Substrate Bias: Internally connected to $-V_{CC}$ power supply.

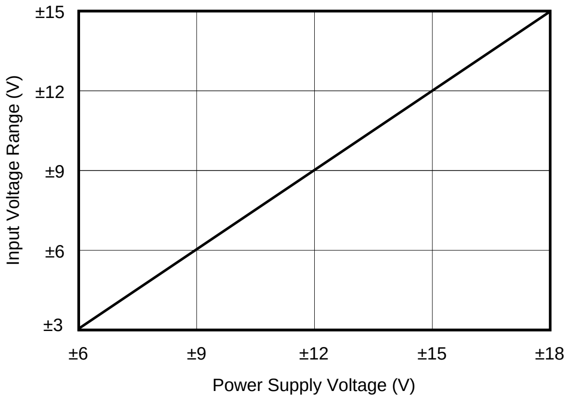
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	139 x 89 ±5	3.53 x 2.26 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

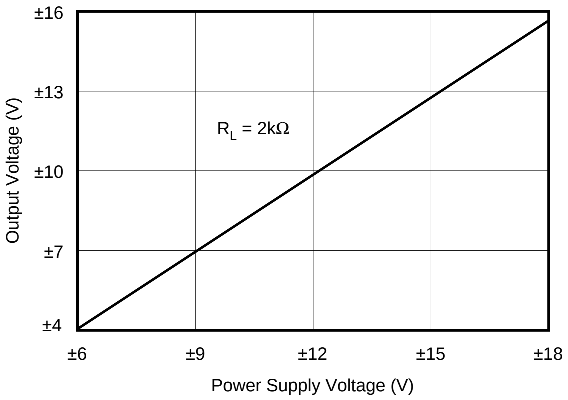
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and $\pm V_{CC}$ = 15VDC, unless otherwise noted.

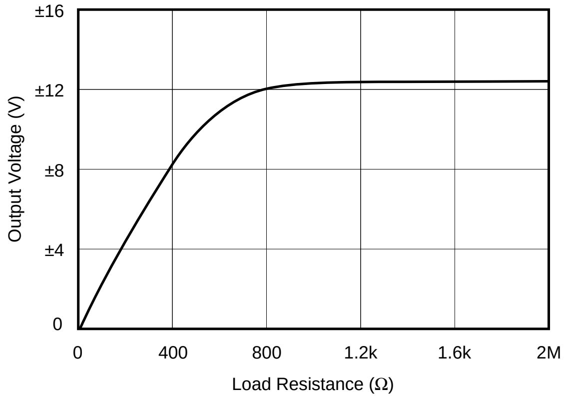
INPUT VOLTAGE RANGE vs SUPPLY



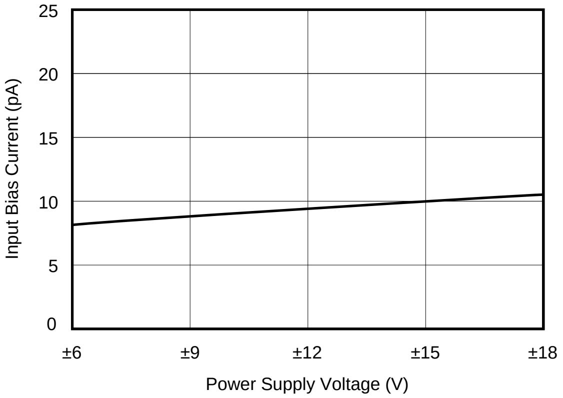
OUTPUT SWING vs SUPPLY



OUTPUT SWING vs LOAD RESISTANCE

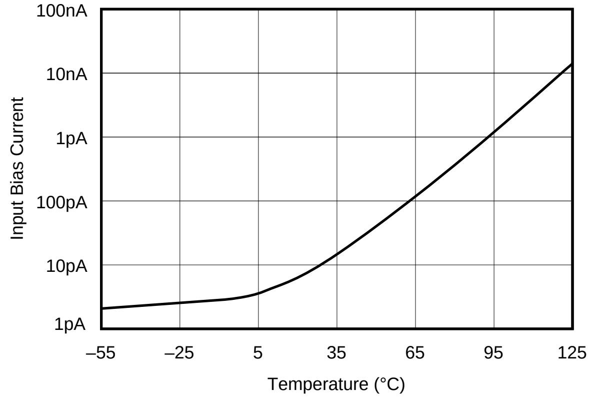


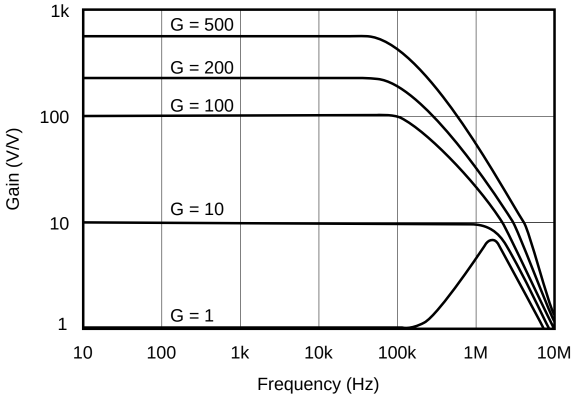
BIAS CURRENT vs SUPPLY

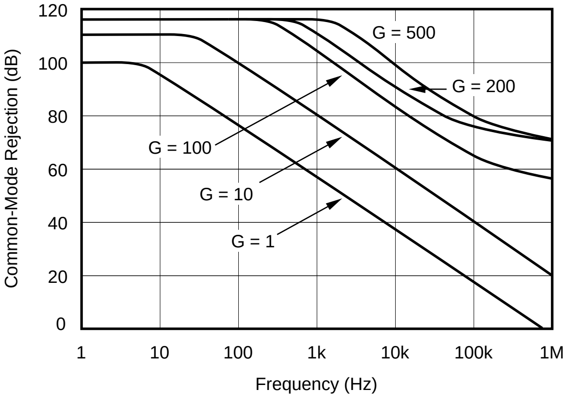


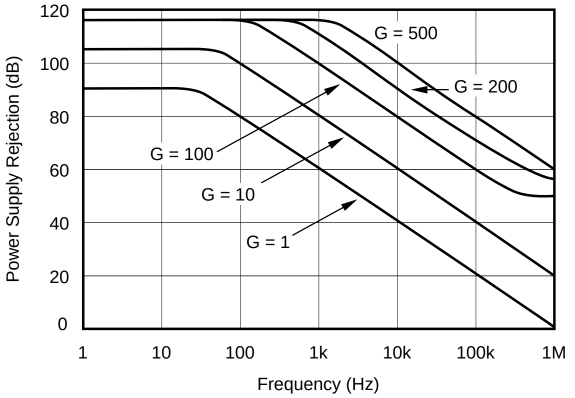
TYPICAL PERFORMANCE CURVES (CONT)

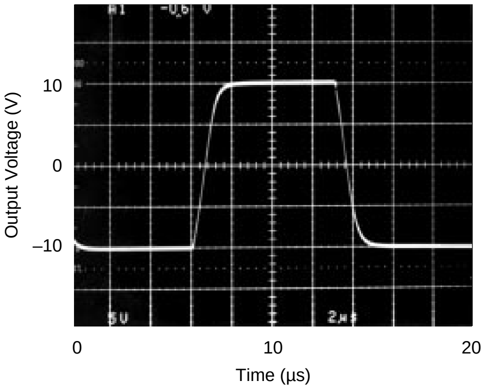
T_A = +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

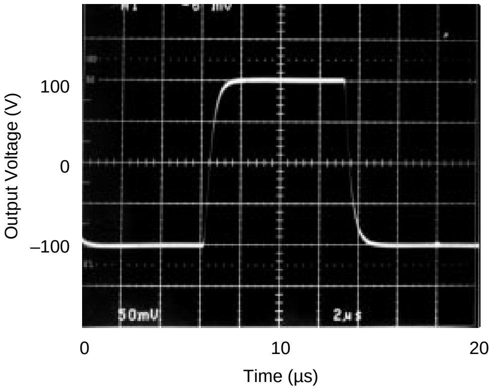

BIAS CURRENT vs TEMPERATURE


GAIN vs FREQUENCY


CMR vs FREQUENCY

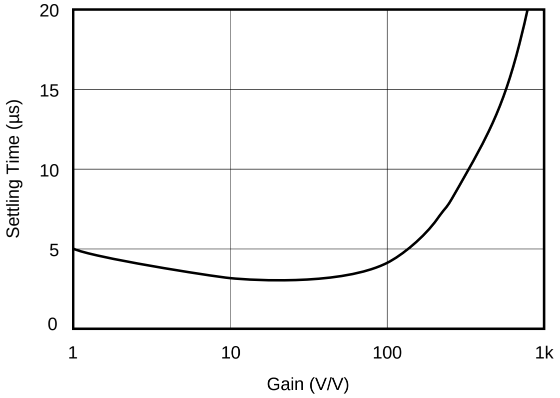

POWER SUPPLY REJECTION vs FREQUENCY

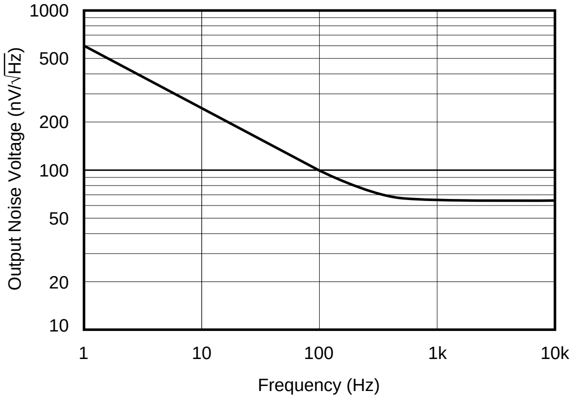

LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)

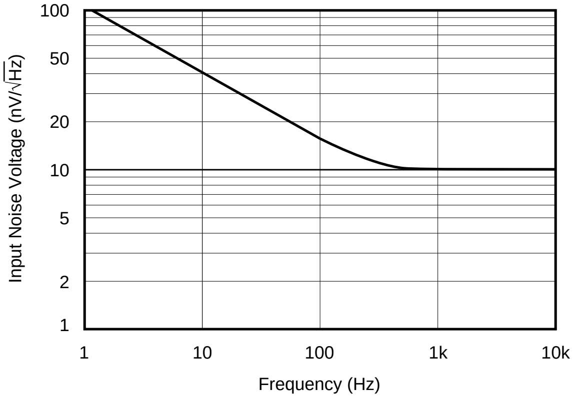

SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)

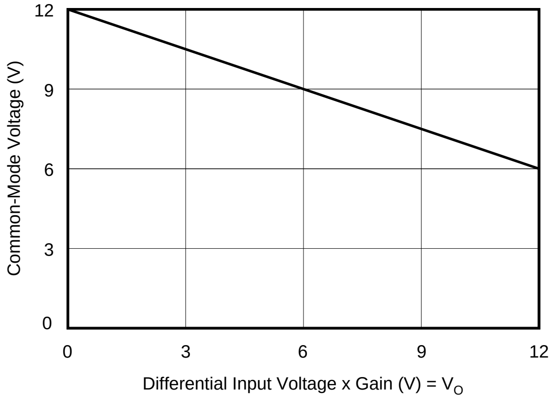
TYPICAL PERFORMANCE CURVES (CONT)

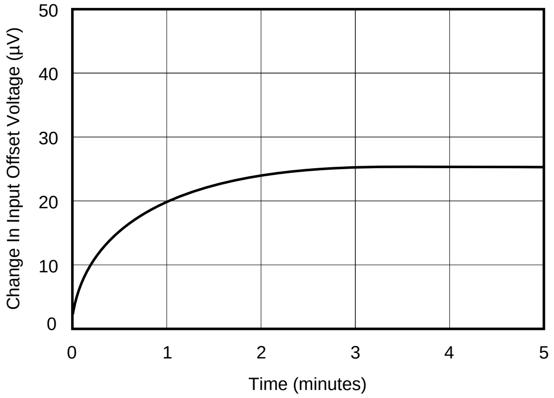
$T_A = +25°C$, $\pm V_{CC} = 15VDC$, unless otherwise noted.


SETTLING TIME vs GAIN
(0.01%, 20V Step)


OUTPUT NOISE VOLTAGE vs FREQUENCY


INPUT NOISE VOLTAGE vs FREQUENCY


COMMON-MODE VOLTAGE vs
DIFFERENTIAL INPUT VOLTAGE


WARM-UP DRIFT vs TIME

DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration using current-feedback type op amps with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10kΩ resistors, especially over temperature and time, assures high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. To maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

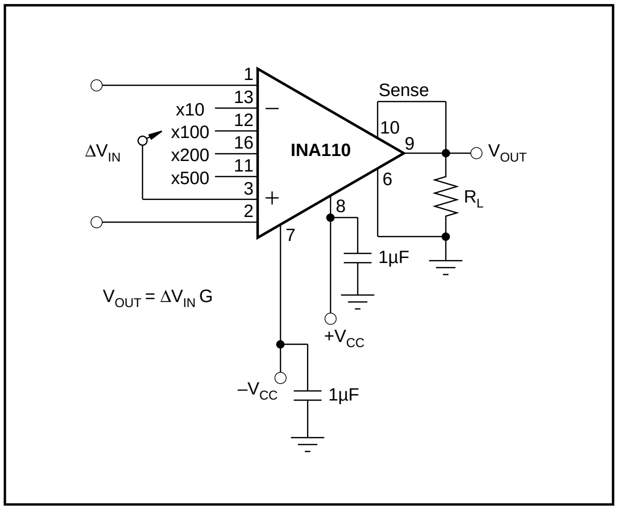


FIGURE 1. Basic Circuit Connection.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by the gain of the input stage. This allows specification of offset independent of gain.

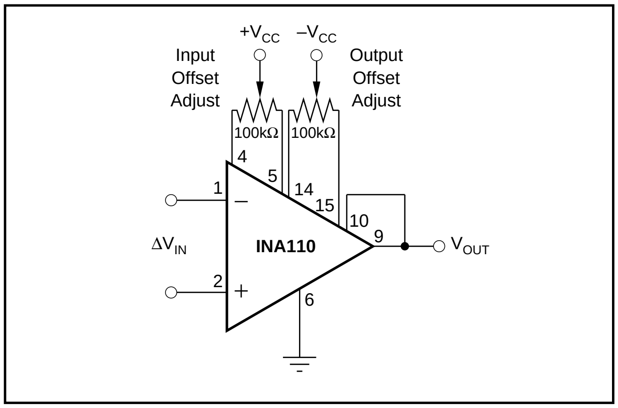
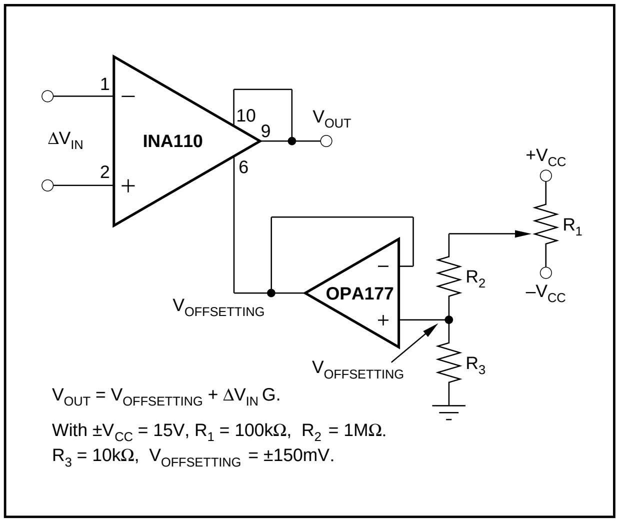


FIGURE 2. Offset Adjustment Circuit.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications, the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33µV/°C per 100µV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 3 by applying a voltage to the reference (pin 6) through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.



$V_{OUT} = V_{OFFSETTING} + \Delta V_{IN}\, G.$

With $\pm V_{CC} = 15V$, $R_1 = 100k\Omega$, $R_2 = 1M\Omega$.
$R_3 = 10k\Omega$, $V_{OFFSETTING} = \pm 150mV$.

FIGURE 3. Output Offsetting.

GAIN SELECTION

Gain selection is accomplished by connecting the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

GAIN	CONNECT PIN 3 TO PIN	GAIN ACCURACY (%)	GAIN DRIFT (ppm/°C)
The following gains have guaranteed accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12, 16	0.25	10
600	11, 12	0.25	40
700	11, 16	2	40
800	11, 12, 16	2	80

TABLE I. Internal Gain Connections.

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G-1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 4. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

OUTPUT STAGE GAIN	R_1 AND R_3	R_2
2	1.2kΩ	2.74kΩ
5	1kΩ	511Ω
10	1.5kΩ	340Ω

TABLE II. Output Stage Gain Control.

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 4).

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents that are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 5. Buffer errors are minimized by the loop gain of the output amplifier.

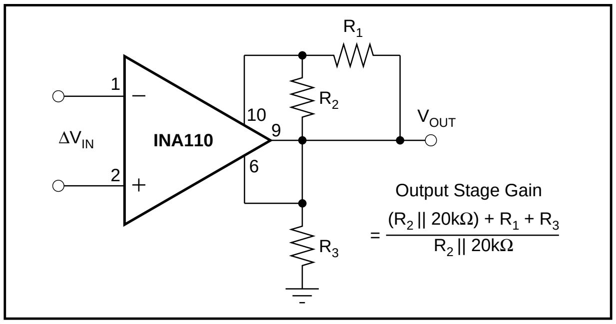


FIGURE 4. Gain Adjustment of Output Stage Using H Pad Attenuator.

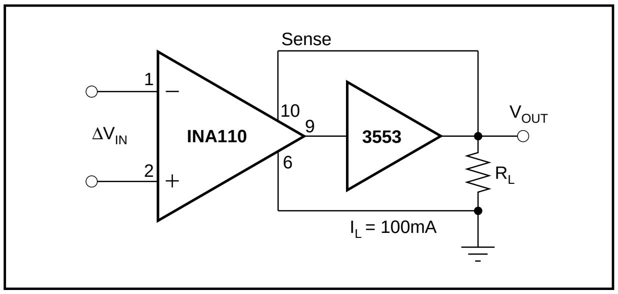


FIGURE 5. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise, the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

Applications with balanced-source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the circuit stability. If the impedance in the positive input is greater, the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback depends upon source impedance imbalance, operating gain, and board layout. The addition of a small bypass capacitor of 5pF to 50pF directly between the inputs of the IA will generally eliminate any positive feedback. CMR errors due to the input impedance mismatch will also be reduced by the capacitor.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit significant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response. CMR is not affected by the addition of the 400kHz RC in a gain of 1.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 6 through 19 show application circuits.

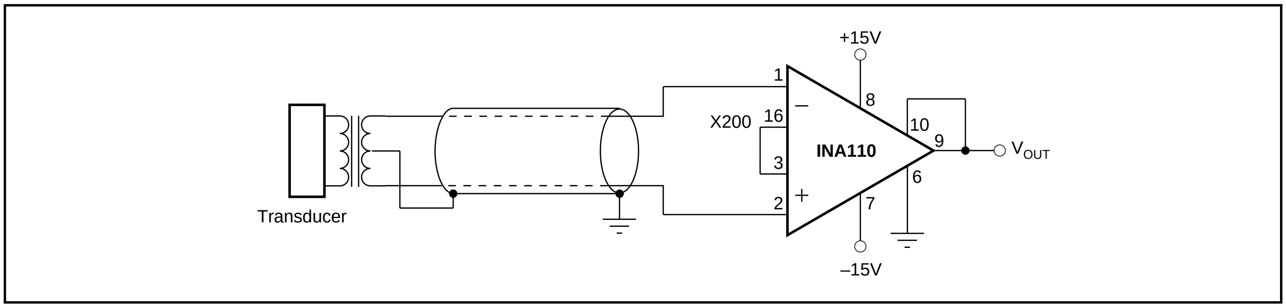


FIGURE 6. Transformer-Coupled Amplifier.

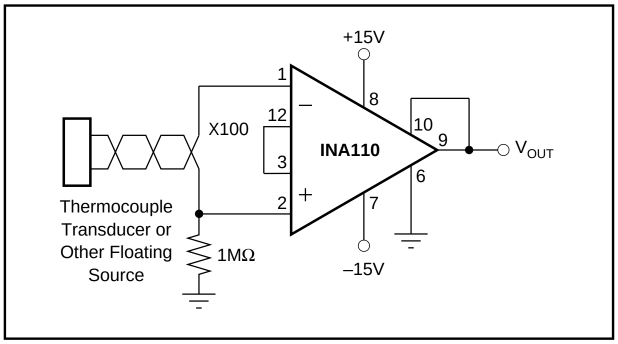
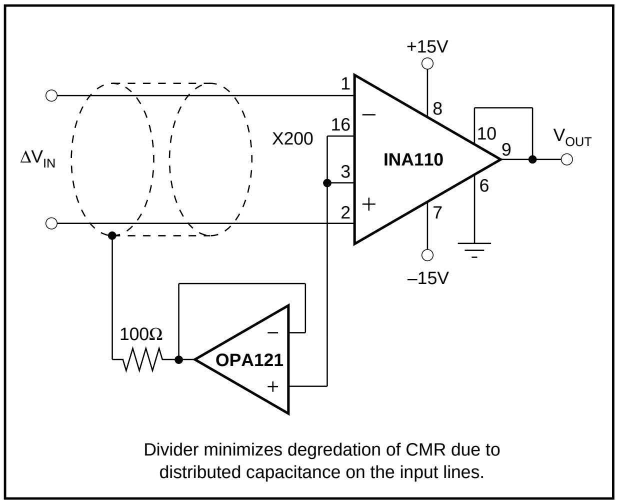
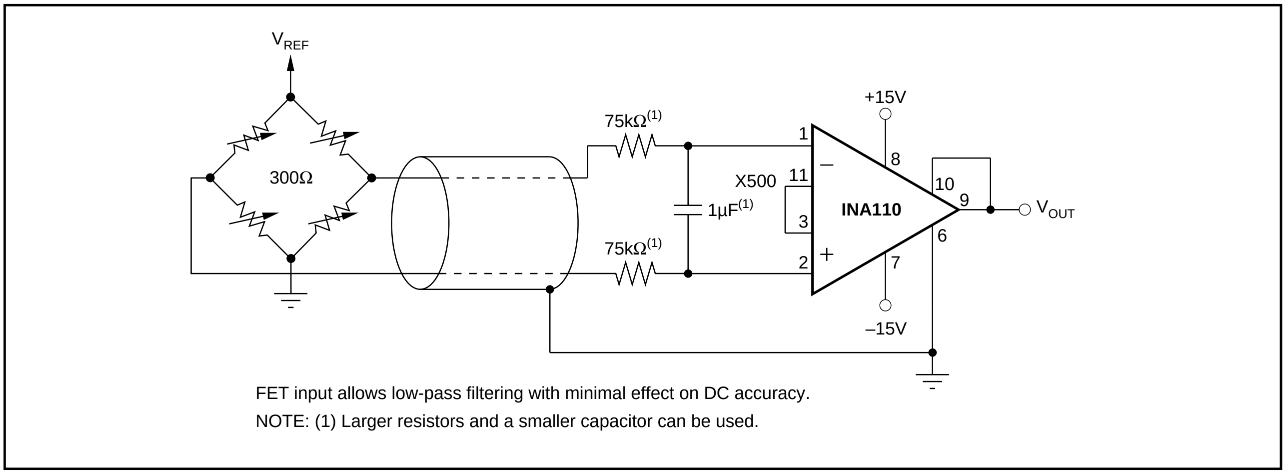


FIGURE 7. Floating Source Instrumentation Amplifier.



Divider minimizes degredation of CMR due to distributed capacitance on the input lines.

FIGURE 8. Instrumentation Amplifier with Shield Driver.



FET input allows low-pass filtering with minimal effect on DC accuracy.

NOTE: (1) Larger resistors and a smaller capacitor can be used.

FIGURE 9. Bridge Amplifier with 1Hz Low-Pass Input Filter.

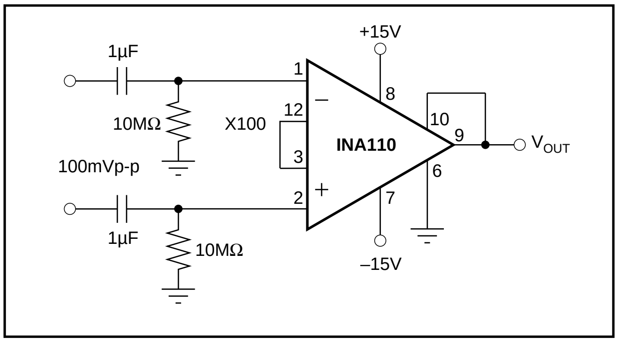
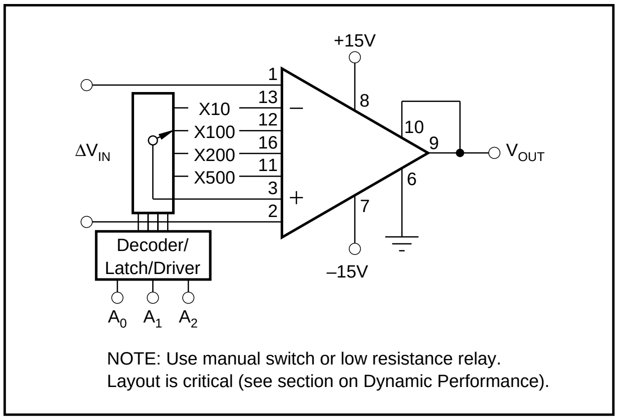


FIGURE 10. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.



NOTE: Use manual switch or low resistance relay.
Layout is critical (see section on Dynamic Performance).

FIGURE 11. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).

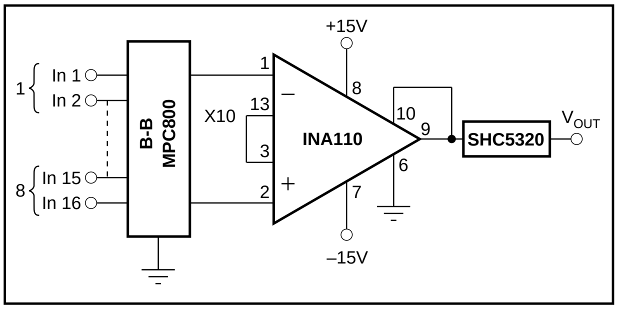
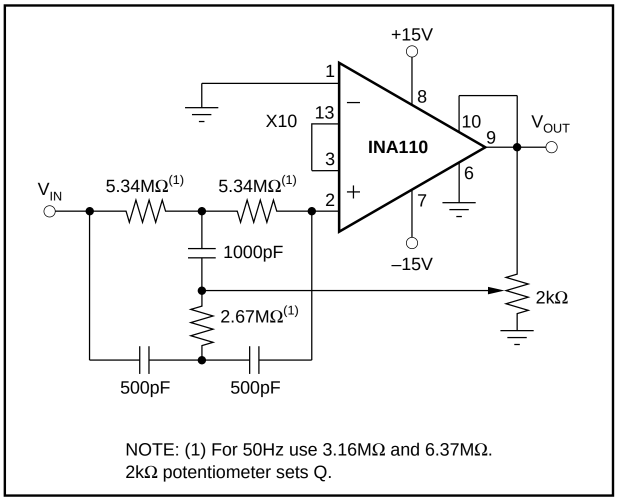
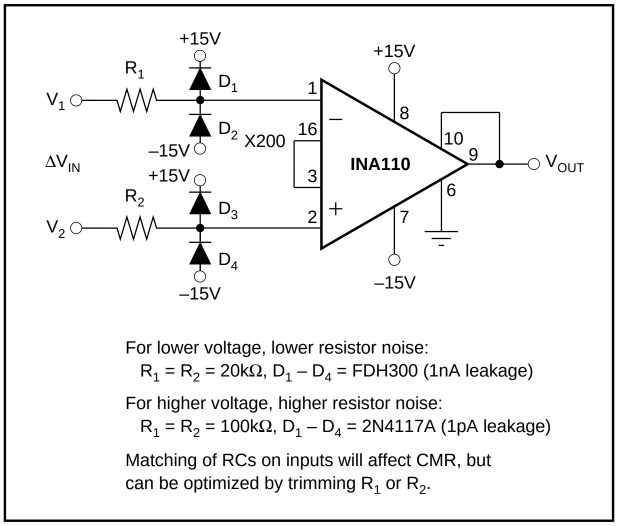


FIGURE 12. Rapid-Scanning-Rate Data Acquisition Channel with 5µs Settling to 0.01%.



NOTE: (1) For 50Hz use 3.16MΩ and 6.37MΩ.
2kΩ potentiometer sets Q.

FIGURE 13. 60Hz Input Notch Filter.

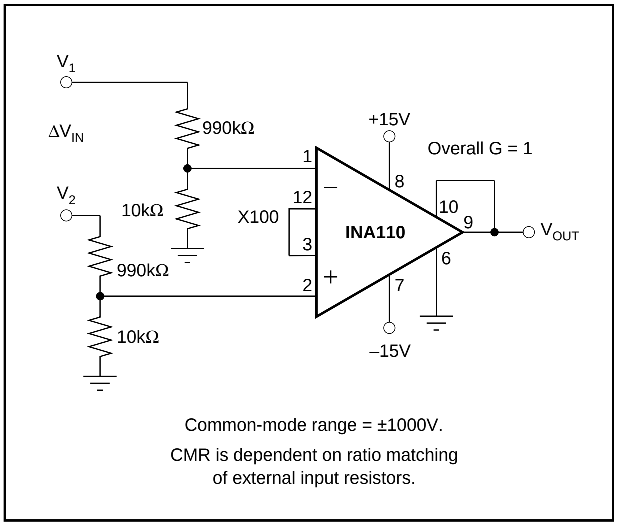


For lower voltage, lower resistor noise:
$R_1 = R_2 = 20k\Omega$, $D_1 – D_4$ = FDH300 (1nA leakage)

For higher voltage, higher resistor noise:
$R_1 = R_2 = 100k\Omega$, $D_1 – D_4$ = 2N4117A (1pA leakage)

Matching of RCs on inputs will affect CMR, but can be optimized by trimming R_1 or R_2.

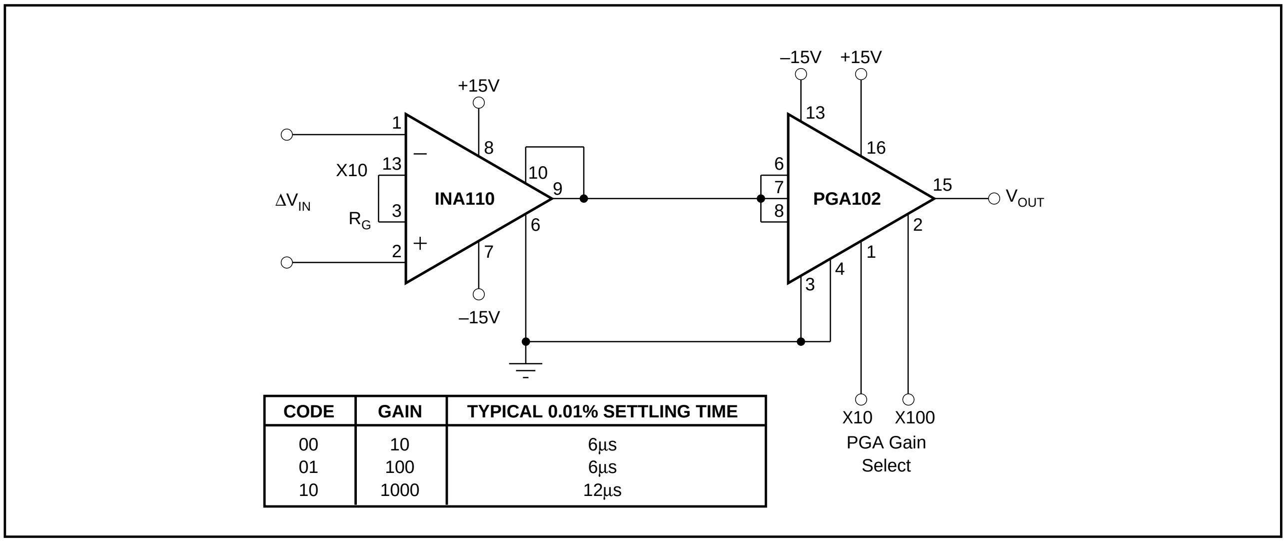
FIGURE 14. Input-Protected Instrumentation Amplifier.



Common-mode range = ±1000V.

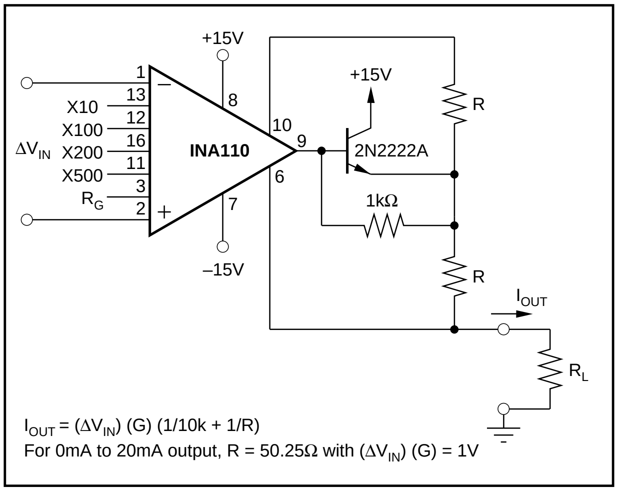
CMR is dependent on ratio matching of external input resistors.

FIGURE 15. High Common-Mode Voltage Differential Amplifier.



CODE	GAIN	TYPICAL 0.01% SETTLING TIME
00	10	6µs
01	100	6µs
10	1000	12µs

FIGURE 16. Digitally-Controlled Fast-Settling Programmable Gain Instrumentation Amplifier.



$I_{OUT} = (\Delta V_{IN})\ (G)\ (1/10k + 1/R)$

For 0mA to 20mA output, R = 50.25Ω with (ΔV_{IN}) (G) = 1V

FIGURE 17. Differential Input FET Buffered Current Source.

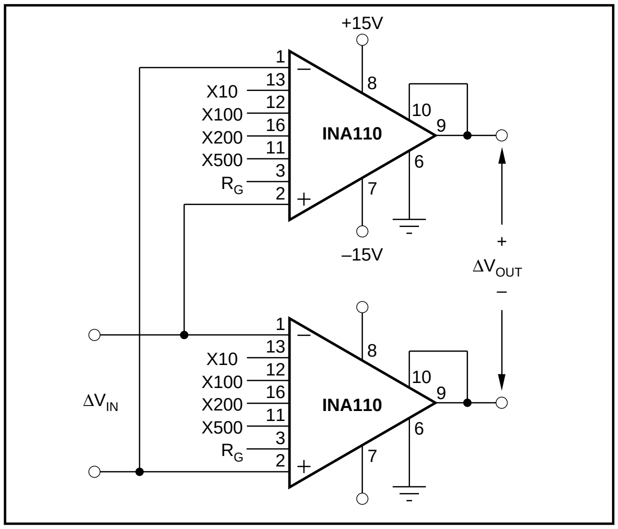


FIGURE 18. Differential Input/Differential Output Amplifier.

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