REVISIONS		
REV.	DESCRIPTION	APPROVED
1	V1.0	1998/04/06

DATA-SHEET

IFK200

Encoder interface board for PC-AT

Index

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1. GENERAL FUNCTIONAL DESCRIPTION

The interface board "IFK200" contains two channels for data logging. The board is applicable as 24-Bit counter interface with integrated decoder for digital Z-track signals, as connection to 2 incremental encoders or as synchronous serial interface (SSI) for 2 absolute encoder.

The board is suitable for applications with length and angle measuring systems and controlling systems. At incremental mode the encoder with sin/cos-outputs (current output: 6 µA < Ipp < 16 µA, voltage output: 0.56 V < Upp < 1.5 V) or square pulse outputs (RS422) can be connected. At SSI mode a connection with to an absolute encoder RS422-interface is needed.

The following functions are available at incremental mode: edge detection, 24-Bit forward and backward counter, register, adder, comparator and bus-interface. To get better resistance against disturbances programmable digital filters are available for the input signals of the measuring system. A transfer clock of up to 32 pulses is provided at SSI mode. A serial-to-parallel converter receives encoder data. All functions are programmable. There is a timer for both modes (incremental and SSI), which is either for generation of a hardware strobe or for representation of the iteration rate (defined hold time). The clock frequency of the system equals 25 MHz of cycle time.

There are D-SUB9-connectors for the power supply of plugged encoders. VPLUS is +5V at incremental mode and +12V at SSI mode. The maximal load per channel is 400 mAmps.

Figure 1 shows the block diagram of the board „IFK200“.

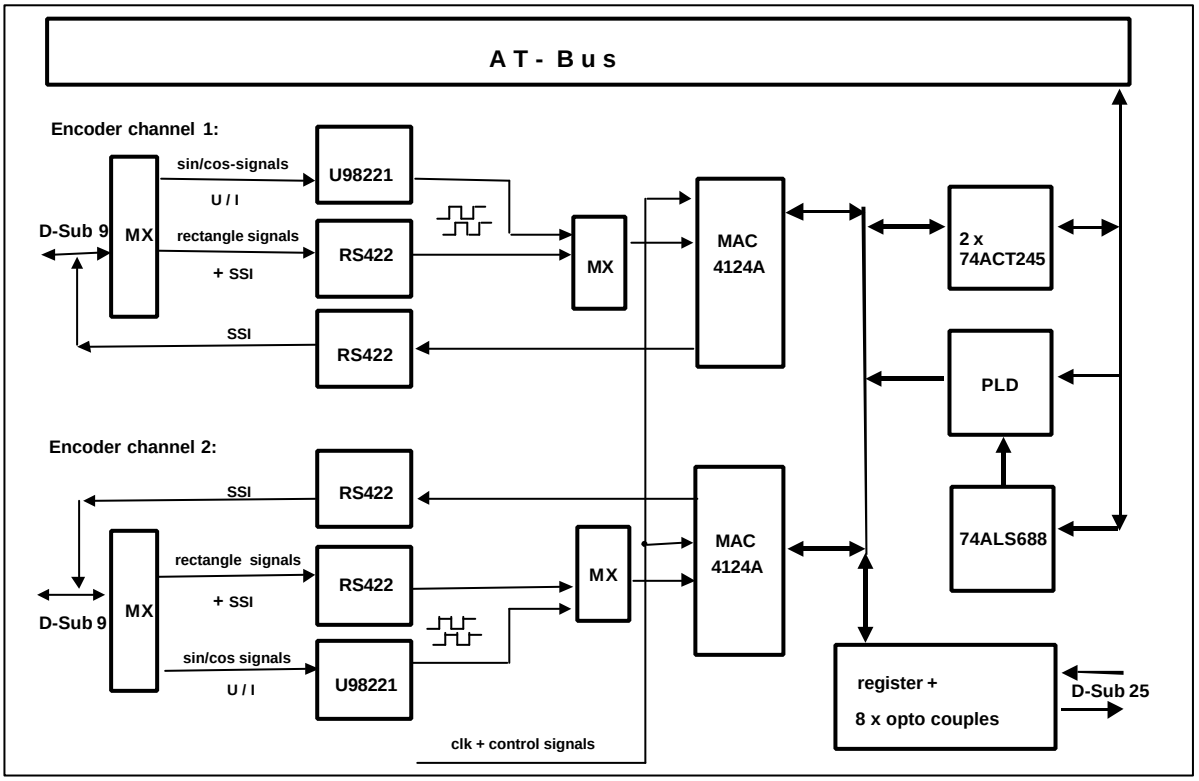

Figure 1: block diagram „IFK200“

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REV.	DESCRIPTION	APPROVED
1	V1.0	1998/04/06

Generation of square pulses by using of sin/cos-inputs

Figures 2-7 shows the creation of square pulse-signals within the interpolator.

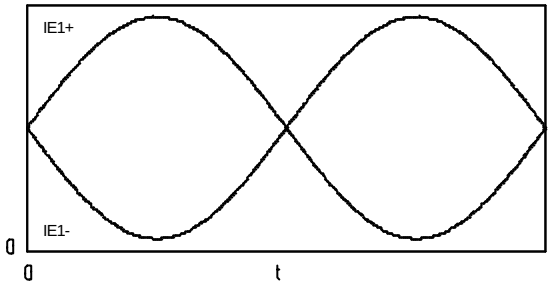


Figure 2: IE1 = M11, MI21

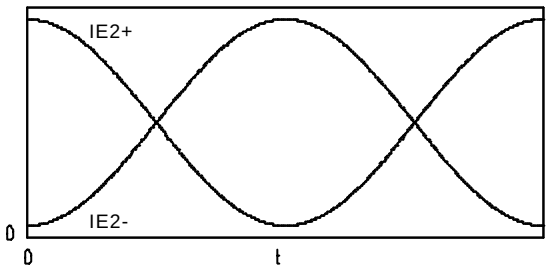


Figure 3: IE2 = M12, MI22

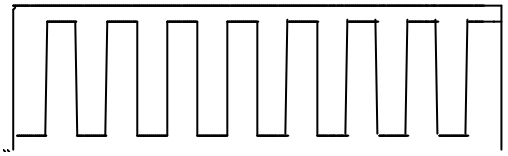


Figure 4: Z1 = CHA

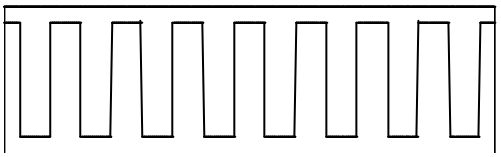


Figure 5: Z2 = CHB

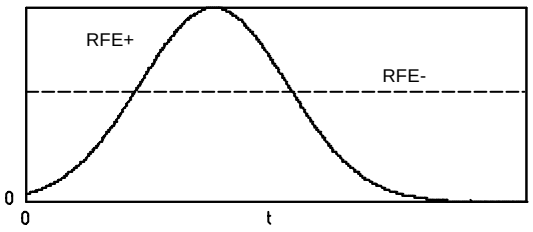


Figure 6: RFE = MI10, MI20

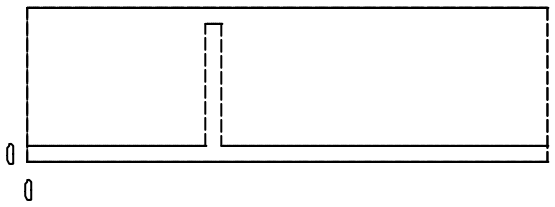


Figure 7: RI = CHC

2. I/O-ADDRESSES AND BUS INTERFACE

The card module supports exclusive 16-Bit accesses (to even-numbered addresses). The addresses decode logic is realisable with SA4 ... SA9 and adjustable by using the DIL-switch S1 (standard value 330/h). The unit needs an address range of 8/h.

The levels of the resources and the board-internal addresses are fixed with writing to offset address 0 to an internal register. After that the access can be made to the corresponding resource with offset address 2.

offset addresses	**function**
0 (write-only)	determination of the level and the board-internal address
2 (read/write)	data access
4	software reset
8	reserved

Table 1a: offset addresses

Table 1b shows the occupancy of the resources and the internal addresses.

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
reserved	Resource-level	Resource-level	address A4	address A3	address A2	address A1	address A0

Table 1b: occupancy of the resources and the internal addresses

D6, D5 = 0 level 0: control register, interrupt-select-RG, opto-coupler
1 level 1: measuring system channel 1
2 level 2: measuring system channel 2
3 level 3: NAS-status register

Tables 2-5 show the addressing of the several resources. The board uses automatic increment.

Level 0:

A(4:0)	**resource**	**write**	**read**
16	control register	set common control register	
		1	
24	interrupt select register	set interrupt select channel 1, 2	
		1	
28	register opto-coupler	set bit 0 - 3	read bit 4 - 7
		1	1

Table 2: address assignment level 0

Level 1, 2: Mode: incremental (SSI = 0)

A(4:0)	**resource**	**write**	**read**
0, 2	strobe register	SW-strobe or write-function	read strobe register ***
		1	2
4, 6	preset register (+)	set preset register	read preset register
		2	2
8, 10	counter	set counter	read counter ***
		1	2
12, 14	reference/offset register	set reference/offset register **	read reference register
		2	2

A(4:0)	resource	write	read
16, 18	control register	set control register 2	read control register 2
20	status register	set register for selection of the resource 1	read status register with reset (++) 1
24	interrupt mask	set interrupt mask 1	read interrupt mask 1
28	timer incl. register	set timer register 1	read status register without reset 1

Table 3: address assignment level 1

Level 1, 2: Mode: synchronous serial interface (SSI = 1)

A(4:0)	resource	write	read
0, 2	serial-to-parallel converter		read serial-to-parallel converter 2
4	preset register (+)	set preset register 1	read preset register 1
8	frequency divider		read frequency divider **** 1
12, 14	reference/offset register	set reference/offset register ** 2	read reference register 2
16, 18	control register	set control register 2	read control register 2
20	status register		read status register with reset (++) 1
24	interrupt mask	set interrupt mask 1	set interrupt mask 1
28	timer incl. register	set timer register 1	read status register without reset 1

Table 4: address assignment level 2

** For activated "Add-Offset" bit of the control register the reference/offset registers are loaded with data of the input registers at a time. For not activated "Add-Offset" bit the reference/offset registers are loaded with the actual counter value.

*** For activated "Add-Offset" bit the value of the offset register is added on read resource.

**** Function is only for test purposes.

(+) SSI=0: preset register (24-Bit) for counter, SSI=1: preset register (16-Bit) -> D(15:10) impulse count, D(9:0) clock frequency

(++) reset status register (except bit 3 - "zero") and reset automatic increment

| | needed accesses

Two accesses are needed for resources >16-Bit. Thereby the access should be started with the low word. The high word is assessable with the twice incremented address.

Level 3:

A(4:0)	resource	write	read
28	NAS status register	reset NAS 1, 2 1	read NAS 1, 2 1

Table 5: address assignment level 3

3. CONFIGURATIONS OF THE MEASURING SYSTEM

3.1 Common control register

The configurations of the measuring system are stored in several control registers. A common 11-Bit control register (offset address: 0/8/dec) contains information for both channels about selection of the encoder interface, selection of the interpolation factor and about zero-adjustment and strobe for being in "master-slave-mode" (channels are cascadable).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF22	IF21	MX21	MX20	IF12	IF11	MX11	MX10
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Analog switch	Analog switch	Analog switch	Analog switch	SSI-mode	casc. Strobe	casc. Strobe	casc. Zero position

The capable encoder interface is selectable by bits 0, 1, 4 and 5:

MX11 MX21	**MX10 MX20**	**channel 1 / channel 2 / for encoder with:**
0	0	analog current output (Iss = 11µA nominal)
0	1	analog voltage output (Uss 1V nominal)
1	x	RS422-interface and SSI

Additional to the initialising of the Encoder the circuit must be adept to the wire end resistor.

for encoder with:	**channel 1** Bit13, Bit12	**channel 2** Bit15, Bit14
analog current output	0 0	0 0
analog voltage output	1 1	1 1
RS422-interface	1 1	1 1
SSI	0 1	0 1

The factor of the interpolation is selectable by bits 2, 3, 6 and 7:

IF12 IF22	**IF11 IF21**	**channel 1 / channel 2 / factor:**
0	0	interpolation - 5
0	1	interpolation - 10
1	0	interpolation - 25
1	1	interpolation - 50

By setting of bit 8 the measuring system channel 2 is also adjusted to zero, if a zero pulse occurs at channel 1 (zero-synchronisation for channel 2):

Bit 8	**strobe for channel 2 generated by:**
0	zero-adjustment-input channel 2 ZERO2
1	zero-adjustment of channel 2 via channel 1 synchronisation

Strobe input for channel 2 is selectable by bits 9 and 10.

Bit 10	Bit 9	channel 1	channel 2
0	0	NSTR1 (strobe-input channel 1)	NSTR2 (strobe-input channel 2)
0	1	NSTR1 (strobe-input channel 1)	NSTR1 (strobe-input channel 1)
1	0	NSTR1 (strobe-input channel 1)	timer 1
1	1	CHC1(index track channel 1)*	CHC2 (index track channel 2)*

* Using the strobe registers for reference-strobe: The system index impulse serves to take over the actually counter into the strobe register.

Bit 11: Bit 11= 0 : The board works in the „incremental" mode. It's possible to connect incremental Encoders (sin/cos or TTL).
Bit 11=1 : The board works in the „SSI" mode. It's possible to connect absolute Encoders.

3.2 Control register of the measuring channels

Every measuring system channel contains a 24-Bit control register (offset address: channel 1: 1/8/dec, channel 2: 2/8/dec), which supports the following operating modes: first zero-adjustment, rerun zero-adjustment, set-by-ref, counter stop, edge decoding, strobe-enable, reference-enable, reference compare, input filter, Gray-to-binary conversion, parity, even/odd and filter.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Low-Byte	reserved	set-by - reference	counter-stop	repetition	zero-adjust-ment	reference compare	reference enable	strobe enable
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Middle-Byte	filter	filter	parity even/odd	parity	Gray to binary	Ddd offset	IPF 1	IPF 0
	Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
High-Byte	filter	filter	filter	filter	filter	filter	filter	filter

The following functions can be activated (Dx = high):

D0: strobe allowed
D1: reference-strobe allowed in case of CHA*CHB*CHC
hint: If the status register is reset during active reference pulse, the reference pulse is detected again!
D2: reference-compare allowed: The counter value is compared with the reference value, in case of identity the reference-compare-bit of the status register (bit 2) is set.
D3: zero-adjustment (one time zero-adjustment with CHC*CHD)
D4: repetition allowed (at each CHC*CHD)
D5: switch off counter inputs
D6: set-by-reference allowed (at CHC*CHD)
D8, 9: selection of the pulse edges:

Bit 9	Bit 8	analysis-mode
0	0	pulse-direction-mode
0	1	single edge decode
1	0	two edge decode
1	1	four edge decode

D10: add on of offset allowed (to counter and strobe register value)
D11: Gray-to-binary conversion of serial data stream (SSI)
D12, 13: parity check allowed (bit 13 = 0: even, bit 13 = 1: odd)
D(14:23): depth setting of the filter

The filter programming (define the minimum period for the working signal) is realised in the control register D(23:14).

adjustment of the value [WTsignal] for the desired minimum period of the signal [Tsignal]:

[WTsignal] = (Tsignal / Tsys) - 1
or
[WTsignal] = (fsys / 2*fsignal) - 1

Tsignal - minimum time of the signal
fsignal - maximum frequency of the signal
fsys - system clock frequency
Tsys - cycle duration of the system clock

Example:

To recognise at the signal frequencies 9,766 kHz only (system clock frequency = 20 MHz), 1023/dec has to be written in for Vtsignal to the bits D(23:14) of the control register with 000300/h (4-x decode).

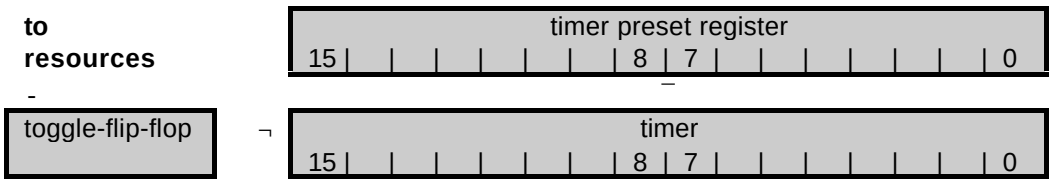
3.3 Timer preset register

Each internal timer unit consists of a 16-Bit timer with toggle-flip-flop and a timer preset register (offset address: channel 1: 1/14/dec, channel 2: 2/14/dec). They serve for representation of an iteration rate of the measuring values (strobe rate, sampling rate). Using the hardware strobe at incremental mode allows copying the actual counter value in to the strobe register. The use of the synchronous serial interface starts the transfer clock (of an absolute encoder).

The timer outputs are internally used to generate either the strobe rate for the counter (incremental mode) or the clock for the absolute encoder (SSI mode). Therefore the hardware strobe inputs „NSTRx" have to be inactive (NSTRx = 1), because NSTRx and the internal timer outputs are combined with functional OR.

It's possible to control channel 2 with timer 1 to synchronise both measuring channels. The timers are programmed with 16-Bit timer preset register. Therefore the timers divide the clock frequency of the system by the adjusted coefficient. The timers are inactive after reset resp. initialisation of the timer preset registers with 0000/h.

Each value unequal 0000/h within the register starts the timer.



Adjustment of the desired divider [TTF]:
The timer preset register should be [WTTF] = TTF/2 - 1.

Example:

To get NSRB of 5 MHz (system frequency is 20 MHz), the timer preset register should be 0001/h.

3.4 Preset registers

At SSI mode the preset registers (offset address: channel 1: 1/2/dec, channel 2: 2/2/dec) serve for adjusting the transmission clock speed data length.

4. RESOURCES OF THE MEASURING SYSTEMS

The IC's MIP200 (interpolator IC) and MAC4124A (interface IC) determine the data logging.

Each MAC4124A makes it possible to connect either one incremental encoder or one absolute encoder (SSI). The IC MAC4124A contains at incremental mode 24-Bit forward and backward counter, strobe register, preset register, reference/offset register, adder, timer and write/read register. Optional the MAC4124A can be utilised as synchronous serial interface (SSI) for absolute encoder. In this case the following resources are available: clock generator (for encoder clock), serial-to-parallel converter, preset register, offset register, adder, timer, write/read register.

The IC MIP200 can increase the measuring resolution with factors 5, 10, 25, 50 using sin/cos-encoder, so that in connection with edge decoding the maximum of the interpolation is 200. Edge-sensitive signals NSTR1 and NSTR2 are hardware strobe inputs, signals NULL1 and NULL2 are for external zero-adjustment. Signal's CHD1 and CHD2 are additional reference signals and assessable via outer mini-DIN-connector MDS6100. Normally they are inactive per 10KOhm's pull-up resistor.

Farther detailed information about register contents and IC programming (MIP200, MAC4124A) can be obtained from the data sheets.

5. EVENTS OF THE DATA LOGGING

5.1 Status register

Each measuring system channel contains one 8-Bit status register (basic address: channel 1: 1/20/dec, channel 2: 2/20/dec). The status registers store information about the different events of data logging.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
parity error	Z-track disturbance *	lost reference	Overwritten strobe	zero-adjustment	reference compare	reference	valid strobe

* Z-track disturbances or too high speed (only for active input filter) or Z-track alternations (CHA and CHB track alternation at the same time)

At SSI mode "valid strobe" and "overwritten strobe" bits of the status register get a new but similar meaning: "valid parallel value" and "overwritten parallel value" (result after serial-to-parallel conversion). The "valid parallel value" bit is set at the end of the transfer. When the next transfer is started and the "valid parallel value "bit is still active, the "overwritten parallel value" bit is set. At SSI mode the "parity error" bit prevents the setting of the "valid parallel value" bit. Reset initialises the status register with 00/h. When the status register is read, all bits are reset except "zero-adjustment" (bit 3). The status bit "zero-adjustment" is reset together with the "zero-adjustment" bit of the control register.

5.2 NAS status register

If the sin/cos signals of the measuring system inputs are outside of the default value range (6µA < Ipp < 16 µA resp. 0.56V < Upp < 1.5V), each bit of the NAS status register (basic address: channel 1: 3/14/dec) is set.

Bit 1	**Bit 0**
NAS 2 (channel 2)	NAS 1 (channel 1)

6. INTERRUPT REQUEST

Each status register bit of both measuring system channels can trigger an interrupt. Each 8-Bit interrupt mask (offset address: 1/24/dec, 2/24/dec) serves for masking the different interrupt sources of the measuring system. If a bit is set, the corresponding interrupt is enabled, i. e. each channel triggers one common interrupt.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
parity error	Z-track disturbance	lost reference	Overwritten strobe	zero-adjustment	reference compare	reference strobe	strobe

Each measuring channel has one interrupt select register (offset address: channel 1: 0/24/dec). With it the above-mentioned common interrupt is assigned to the different interrupt request signals of the AT bus. It's also possible to assign the common interrupt request signals of both channels to one IRQx. If one bit is set, the corresponding connection is switched on.

	channel 2:	channel 1:
	Bit (13:11)	Bit (10:8)
Interrupt not allowed	0	0
IRQ10	1	1
IRQ11	2	2
IRQ12	3	3
IRQ15	4	4

Reset initialises the interrupt mask and the interrupt select register with 00/h.

7. OPTO-COUPLERS

The board has 8 opto-couplers PC 847, Sharp (substitute TIL193 B, Texas Instruments) to drive external devices. The couplers have their own register (basic address: 0/28/dec), which is write-able resp. readable. Four of them (outputs, write-only) can connect external signals. The other four couplers can receive control signals from external devices.

If a bit of the register D(3-0) is set, the adequate switch Opto(3-0) is closed. A logical "high" at the inputs D(7-4) of the opto-couplers sets the corresponding Bit(7-4) of the register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	opto-coupler -inputs				opto-coupler-outputs			
	Read-only				Write-only			
	Opto_7	Opto_6	Opto_5	Opto_4	Opto_3	Opto_2	Opto_1	Opto_0

7.1 Technical data of the opto-coupler inputs

The four inputs (R = 470 0) is combine to a common potential wire X5:11. This wire must be connected to the power supply (+5V up to +12V). If no galvanic division is necessary the power supply X5:14 (protected with F2) will connect to X5:11. On that condition X5:15 is connect to GND = 0V (see example 1).

For control the channels (X5:2, X5:4, X5:6, X5:8) a TTL-signal I=10mA is necessary (e.g. control by 74 ALS 04).

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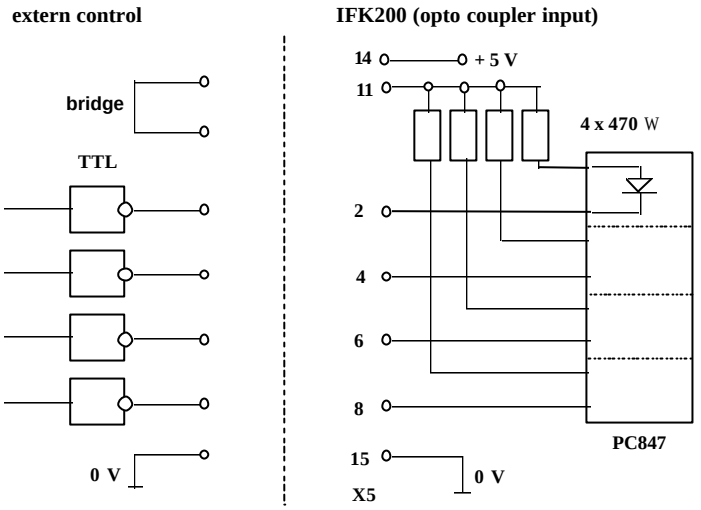
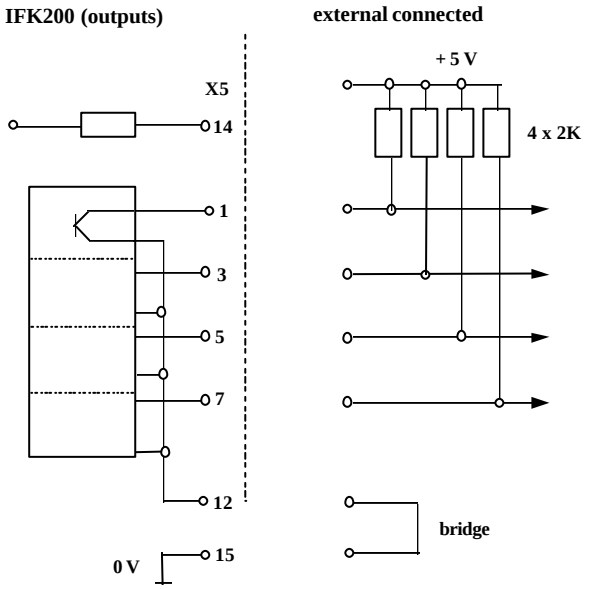
Example 1: (galvanic division)



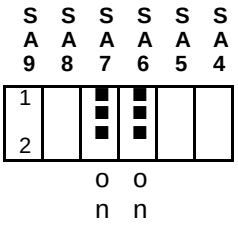
The four outputs has a common pin (X5:12) connected to GND = 0V. The channel outputs (X5:1, X5:3, X5:5, X5:7) are link with a 2K 0 resistor to +5V supply. The outputs supply TTL or CMOS level. The maximum transfer frequency is up to 10 kHz. If no galvanic division is necessary it is possible to use the power supply X5:14 U= +5V and X5:15 GND=OV (see example 2). An external power supply can be used between +5V and +12V. The TTL or CMOS level is only within reach by the power supply of +5V.

Example 2: (no galvanic division)



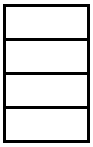
8. PRESETTING

Board address DIL-switch (S1)

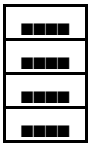


switch off: SAx = H ; e.g. 330/h (default setting)

Selection of the operation mode: jumper X7

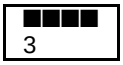


incremental (default setting)



SSI

jumper X8



9. CONNECTORS ALLOCATION

Table 6 shows the signal allocation of both D-SUB9-connectors:

pin-no.	connector X2	connector X3	*specials at SSI*
1	M11_N	M21_N	*data (negative)*
2	GND	GND	
3	M12_N	M22_N	*clock (negative)*
4	GND	GND	
5	M10_N	M20_N	
6	M11	M21	*data*
7	V_{PLUS} (+5V or +12V)	V_{PLUS} (+5V or +12V)	
8	M12	M22	*clock*
9	M10	M20	

Table 6: D-SUB9-connectors allocation

Table 7 shows the signal allocation of the 6-pole Mini-DIN-Connector:

pin-no.	Mini-DIN-Connector MDS6100 X4	
1	NSTR1	pull-up
2	NSTR2	pull-up
3	NULL1	pull-up
4	NULL2	pull-up
5	CHD1	pull-up
6	CHD2	pull-up

Table 7: MDS6100-connectors allocation

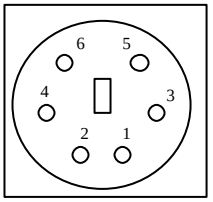


Table 8 shows the signal allocation of both pin rows:

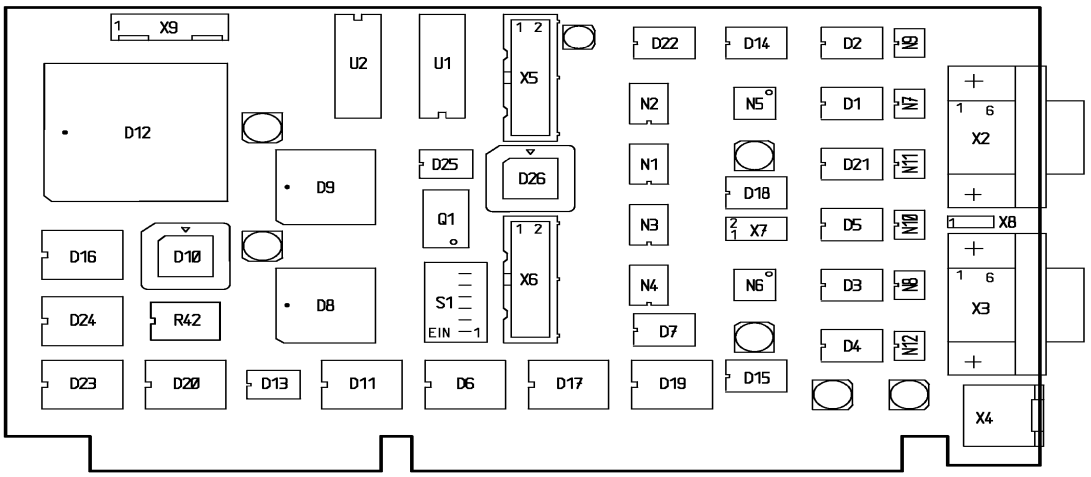
plug	D-SUB		signal
16p X5	15p XH1		
1	1		OPTO_O1
2	9		OPTO_I1
3	2		OPTO_O2
4	10		OPTO_I2
5	3		OPTO_O3
6	11		OPTO_I3
7	4		OPTO_O4
8	12		OPTO_I4
9	5		NSRB1
10	13		NSRB2
11	6		OPTO_I+5V
12	14		OPTO_OM
13	7		
14	15		+5V
15	8		GND
16			

plug	D-SUB		signal
16p X6	15p XH2		
1	1		SIN1_P
2	9		SIN2_P
3	2		SIN1_N
4	10		SIN2_N
5	3		COS1_P
6	11		COS2_P
7	4		COS1_N
8	12		COS2_N
9	5		REF1_P
10	13		REF2_P
11	6		REF1_N
12	14		REF2_N
13	7		UM1_N
14	15		UM2_N
15	8		GND
16			

Table 8: allocation of the pin rows

REVISIONS		
REV.	DESCRIPTION	APPROVED
1	V1.0	1998/04/06

10. CONSTRUCTIVE COMPOSITION



Hardware:

IFK200:	LP-No.: 090 005 -051
ispLSI2064 (D12):	Code: 9B55
GAL16V8 (D10):	Code: 3AFC
GAL16V8Ref (D26)	Code: 2083

The data sheets of the IC's MIP200 and MAC4124A of MAZeT GmbH are general basis of this documentation.

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