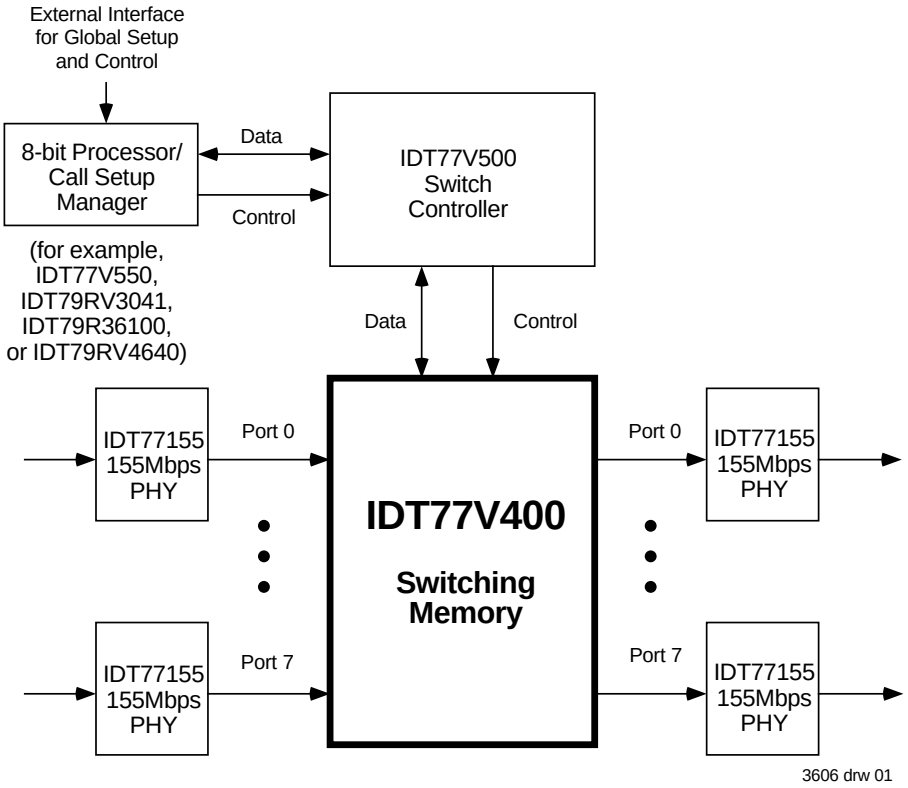
SWITCHStAR™ ATM CELL BASED 8 X 8 1.24Gbps NON-BLOCKING INTEGRATED SWITCHING MEMORY

PRELIMINARY
IDT77V400

Features

- Single chip supports an 8 x 8 port switch at 155Mbps per port
- Fusion Memory™ technology utilized to provide the performance of SRAM with the economy of DRAM
- Central Memory Architecture eliminates Head-of-Line Blocking by sharing the memory array with all ports
- Low power dissipation
  - *330mW (typ.)*
- Data Path Interface (DPI) provides configurable Input and Output ports; up to 8 receive and 8 transmit ports at 155Mbps
- Supports data rates up to 1.24Gbps with a 32-bit wide configuration; 155Mbps per 4-bit port
- Can be cascaded for larger switch configurations
- Fast Input/Output port cycle times
  - *23ns min. (43MHz max.)*
  - *26ns (38.50MHz) typ. with 155Mbps on each 4-bit port*
- Expander and Concentrator function is fully supported by the Input and Output port configuration options
- 8192 cells (52 to 56 bytes each) of on-chip memory capacity
- Configurable cell lengths of 52, 53, 54, 55, or 56 bytes can be independently chosen for Input and Output ports
- Byte Addition or Byte Subtraction for x4/x8 to x16/x32 conversion capability
- Internal header Cyclical Redundancy Check (CRC) and generation logic on-chip
- Header modification, pre-pend, and post-pend operations available as well as Multicasting and Broadcasting capability
- High-bandwidth control port for queue controller system block, up to 36 MHz cycle time
- Can be used with the companion IDT77V500 Switch Controller or custom logic for traffic management
- Industrial temperature range (-40°C to +85°C) is available
- Single +3.3V ± 300mV power supply
- Available in an 208-pin Plastic Quad Flat Pack (PQFP)

Typical 8x8 Switch Configuration using the IDT77V400 Switching Memory



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Description

The IDT77V400 ATM Cell Based Switching Memory provides the logic and memory necessary to perform high-speed buffering and switching operations on ATM cell data. A single IDT77V400 provides a cost effective switching element to implement an 8 x 8 155Mbps switch with 1.24Gbps total switching bandwidth. The user configurable data ports provide an aggregate bandwidth of 1.24Gbps for both receive and transmit functions, and the cell lengths are user programmable to up to 56 bytes.

The memory provides storage for 8192 ATM cells, each of which can be as large as 56-bytes in length. The main cell memory is implemented as a Fusion Memory array, and an on-chip cell address counter keeps track of cell refresh requirements. There are also sixteen double-buffered Serial Access Memories (SAM); eight for receiving and eight for transmitting the ATM cells.

The input data ports and output data ports are configurable from eight ports of 4-bits at 155Mbps each up to one 32-bit wide port at 1.24Gbps. The sixteen data ports are asynchronous with respect to each other, and each port provides an independent data clock and cell framing signal for start of cell indication. The SAMs are double-buffered for each input and each output port to allow one cell to be transferred to or from the internal memory while that data port continues to receive or transmit a second cell. The cell framing and data clock signals implement a simple handshaking and synchronization protocol which allows multiple Switching Memories to be connected to construct larger switch arrays without requiring additional hardware.

The control interface of the IDT77V400 includes a 6-bit Command Bus (CMD0-5), a 32-bit Control Data Bus (IOD0-31), a Chip Select pin (CS), a 4-bit Address field (ADDR0-3), a RESET pin, an Output Enable pin ($\overline{OE}$), a Control Enable pin ($\overline{CTLEN}$) and a $\overline{CRCERR}$ pin. All control operations are synchronized with respect to the System Clock (SCLK), with the exception of RESET, $\overline{CTLEN}$, and $\overline{OE}$, which are fully asynchronous.

The internal configuration register of the IDT77V400 can be accessed through the Control Data Bus to define the cell length and the input and output data port configurations. Internal error and status registers contain status information regarding each SAM and are accessible via the Control Data Bus (IOD0-31). Input SAM full or Output SAM empty status for all SAMs may be obtained in one access operation. Additional information regarding the reception of short or long cells and Input SAM overflow may also be obtained through the Control Data Bus.

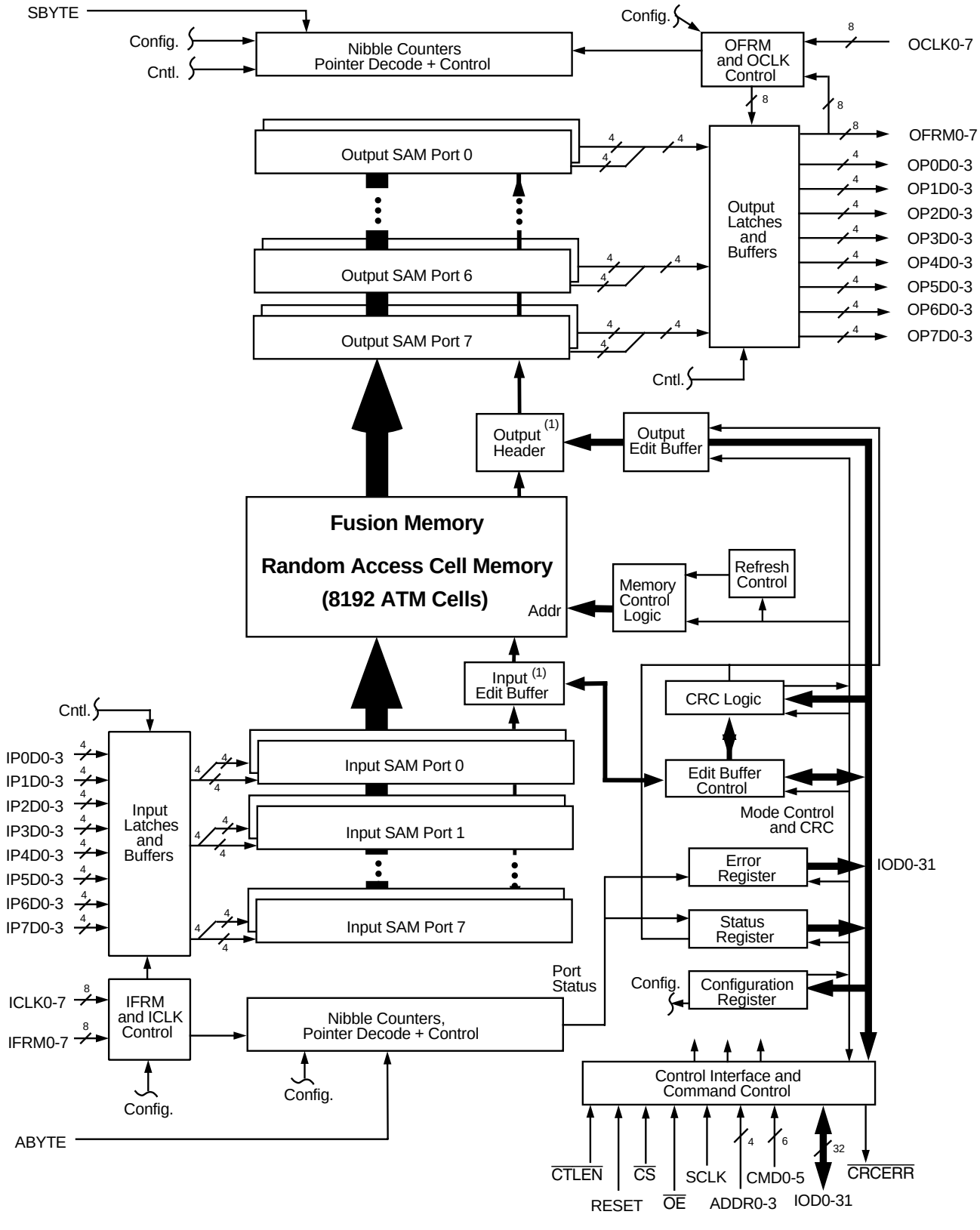
The command set of the Switching Memory provides functions for storing cells in the shared memory, loading Output SAMs, polling the status of the data ports, retrieving and storing original or modified header bytes and pre-pend or post-pend bytes, and refreshing the cell memory. Header $\overline{CRC}$ errors are indicated by a LOW $\overline{CRCERR}$ pin; the $\overline{CRC}$ comparison byte may also be accessed via the status register, which indicates the IPort on which the error was detected. A new $\overline{CRC}$ can be generated upon storing a new header in the PHEC command. Cell headers may be modified upon cell reception at the input ports or upon cell transmit at the output ports. User defined pre-pend and post-pend bytes may also be stored, retrieved, and modified through the Control Data Bus.

The IDT77V400 has a generic control interface which supports a variety of queuing disciplines. By maintaining the memory control in an external controller, system level switching performance may be modified over time as requirements change. In normal operation, the Switching Memory port status is polled by the control function through the Control Data Bus. Upon receiving a cell, the control function can retrieve the header, check the CRC result, and store a new header if needed prior to moving the cell to the shared memory. Pre-pended or post-pended bytes may also be added or retrieved during this time. The output ports are polled at the same time to determine when to send new cells to the Output SAMs. The cell lengths of the input ports do not need to be the same as the output port cell lengths, although all input ports and output ports respectively must be configured to the same cell length.

Please refer to the SWITCHStAR User Manual for additional feature details and implementation information.

The IDT77V400 is fully 3.3V LVTTL compatible, and is packaged in an 208-pin Plastic Quad Flatpack (PQFP).

Functional Block Diagram



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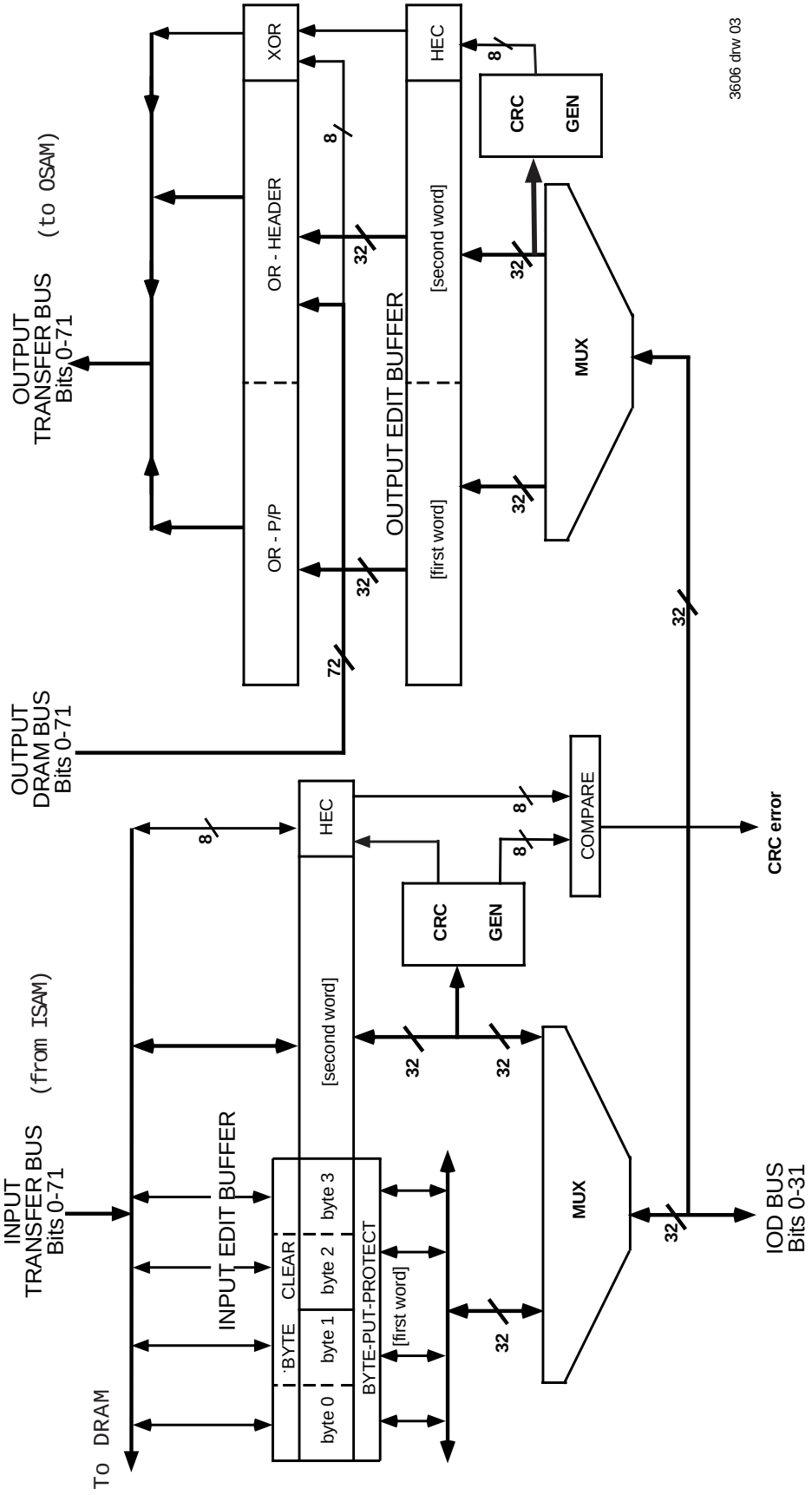
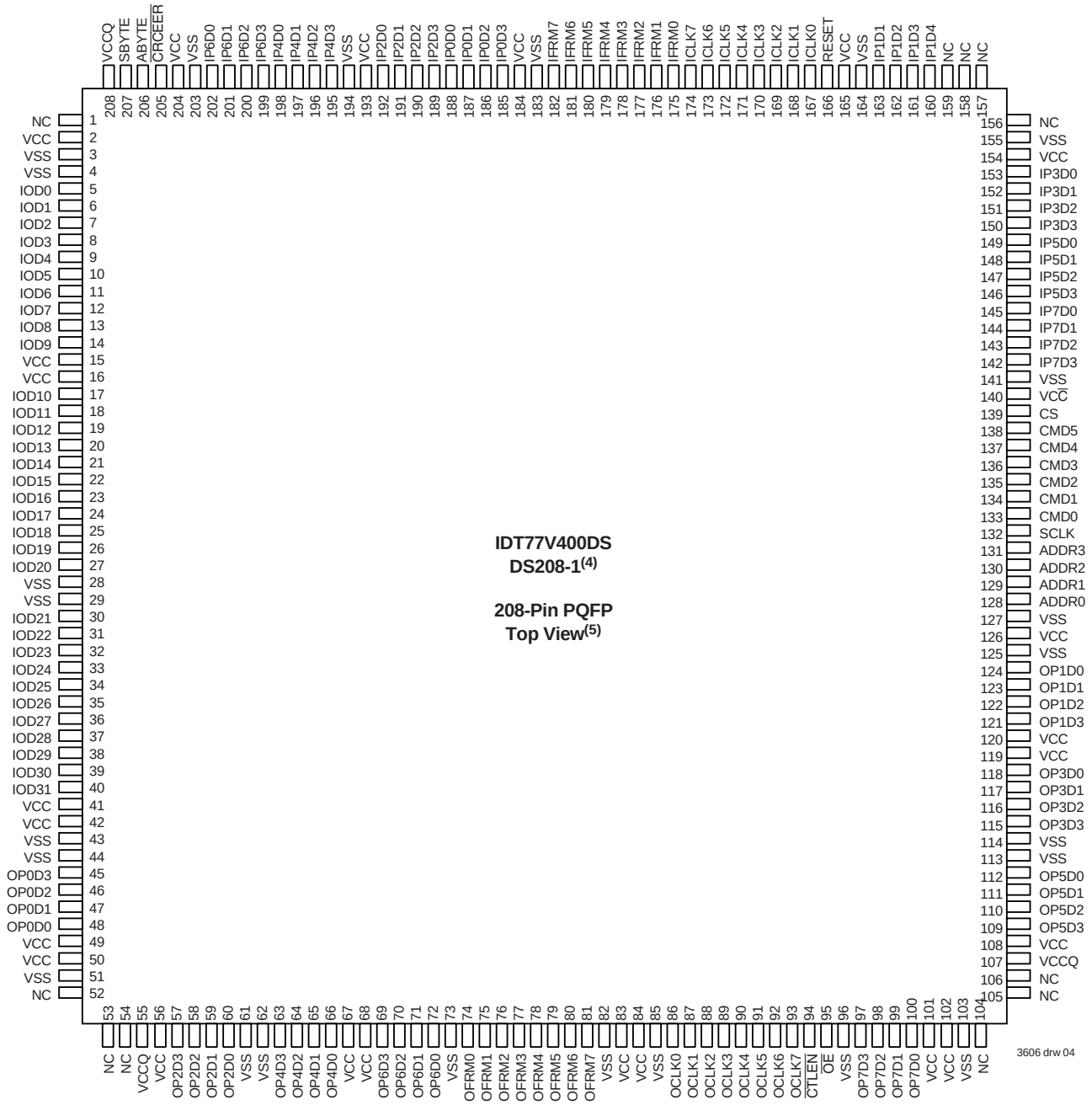
NOTE:
1. See "Input and Output Edit Buffer Block Diagram" for additional detail.

Input and Ouput Edit Buffer Block Diagram



Package Diagram(1,2,3)



NOTES:

1, All V_{CC}/V_{CCQ} pins must be connected to power supply.
2. All V_{SS} pins must be connected to ground supply.
3. Package body is approximately 28mm x 28mm x 3.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part marking.

Pin Description

Pin Number	Symbol	Type	Description
132	SCLK	I	System clock: All bus control signals (CMD0-5, $\overline{CS}$, IOD0-31, $\overline{CRCERR}$) except $\overline{OE}$ are synchronous with respect to SCLK. Control commands are registered on the positive edge of SCLK. The SCLK period must be less than or equal to 200ns during normal operation. Data Port signals are asynchronous with respect to SCLK.
139	$\overline{CS}$	I	Chip Select: Synchronous input which must be LOW at the rising edge of SCLK to enable the Command Bus CMD0-5. Instructions are a NOP when $\overline{CS}$ is HIGH at the SCLK positive edge.
133-138	CMD0-5	I	Command Bus: Synchronized to SCLK, instructions to be executed by the memory are transfered across this 6-bit bus. CMD5 is the MSb of the Command Bus.
95	$\overline{OE}$	I	Output Enable: Asynchronous input that enables all outputs when asserted LOW. All outputs are High-Z when $\overline{OE}$ is HIGH. IOD0-31 and $\overline{CRCERR}$ may also be set to High-Z by a HIGH $\overline{CTLEN}$ bit in the configuration register or a HIGH $\overline{CTLEN}$ pin.
166	RESET	I	Reset: When asserted HIGH, the signal asynchronously allows the initialization of the registers and internal signals of the IDT77V400. RESET should be asserted HIGH and $\overline{OE}$ should be held HIGH upon power-up for the external controller to execute the initialization and insure proper system operation.
128-131	ADDR0-3	I	Chip Address: All ADDR inputs must OR the address in the configuration register bits 26-29 and then must match 1OD13-16 one cycle after the Store or Load command for selection to allow a Store or Load memory cycle to be executed (full flag is cleared regardless of match, and empty must match before clear). ADDR3 is the MSb of the device address bits.
5-14, 17-27, 30-40	IOD0-31	I/O	Control Data Bus: Synchronous with SCLK. Used for external data transfer for the header pre/post-pend bytes, configuration register error and status registers, and the cell memory address. IOD31 is the MSb of the Control Data Bus.
205	$\overline{CRCERR}$	O	Cyclical Redundancy Check Error: Synchronous output on the rising edge of SCLK.$\overline{CRCERR}$ asserted LOW after a Header with CRC operation indicates that a CRC error has occurred on the previous header.
167-174	ICLK0-7	I	Input Port Clock: Synchronizes the input data IPxD(0-3) and IFRMx signal associated with the input data port on the positive clock edge. Each ICLKx is independent of the other seven ICLKs and SCLK. The ICLKs used are determined by the configuration register initialization (see Port Configuration Code Table). The inputting of a cell may be halted by stopping ICLKx.
175-182	IFRM0-7	I	Input Frame: Synchronous input registered on the rising edge of ICLKx. When asserted HIGH this signal denotes the beginning of an input cell for the associated input port. IFRMs used are determined by the configuration register during initialization (see Port Configuration Code Table).
185-188, 160-163, 189-192, 150-153, 195-198, 146-149, 199-202, 142-145	IP(0-7)D(0-3)	I	Input Data: Eight 4-bit input ports. Synchronous with the rising edge of ICLK for the associated data port. IPxD(0-3) can be assigned to different ICLKs and IFRMs via the configuration register during initialization. The ports may be combined in groups to increase bandwidth by factors of 155Mbps (see Port Configuration Code Table). IPxD3 is the MSb of the nibble. Example: IP0D3 is the MSb for port 0.
86-93	OCLK0-7	I	Output Clock: Synchronizes the output data OPxD(0-3) and OFRMx signal associated output data port on the positive clock edge. Each OCLK is independent of the other seven OCLKs and SCLK. OCLKs used are determined by the port configuration register during initialization (see Port Configuration Code Table). The transmission of a cell may be halted by stopping OCLKx.
74-81	OFRM0-7	I/O	Output Frame: Synchronous output on the rising edge of OCLK. The 77V400 marks the beginning of an output cell by taking OFRM HIGH on the rising edge of OCLK. The output SAM nibble counter loads the start byte address from the configuration register when a HIGH signal is sensed at the OFRM pin, thus re-synchronizing other chips connected to the OFRM bus. OFRM is asserted HIGH one OCLK cycle prior to the first nibble of the cell being output from the IDT77V400. OFRMs used are determined by the configuration register initialization (see Port Configuration Code Table). During cell bus operations, the OFRM1-7 are redefined as CBUS1-7 for for arbitration (there is no CBUS0).
45-48, 121-124, 57-60, 115-118, 63-66, 109-112, 69-72, 97-100	OP(0-7)D(0-3)	O	Output Data: Eight 4-bit output ports. Synchronous with the rising edge of OCLK for the associated data port. OPxD(0-3) can be assigned to different OCLKs and OFRMs via the configuration register. The 4 bit ports may be combined in groups to increase the bandwidth by factors of 155Mbps (see Port Configuration Code Table). OPxD3 is the MSb of the nibble. Example: IP0D3 is the MSb for port 0.
94	$\overline{CTLEN}$	I	Control Enable: When asserted LOW, with $\overline{OE}$ LOW and the $\overline{CTLEN}$ bit set LOW in the configuration register, this pin asynchronously enables all Control interface outputs. If $\overline{CTLEN}$ is HIGH all control interface outputs will be High-Z.

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Pin Description (continued)

Pin Number	Symbol	Type	Description
206	ABYTE	I	Add Byte to Input cell: Asynchronous DC signal. If an input port is in a 4-bit or 8-bit DPI mode and ABYTE is asserted HIGH, a dummy byte will be inserted in the ninth byte position (after the HEC byte) to support systems requiring a byte between the last header byte and the payload (otherwise ignored). Not intended for dynamic cycling or operation.
207	SBYTE	I	Subtract Byte to Output cell: Asynchronous DC signal. When and SBYTE is asserted HIGH, the dummy byte in the ninth byte position (after the HEC byte) will be removed prior to transmission to support output port 4-bit and 8-bit DPI modes (otherwise ignored). Not intended for dynamic cycling or operation.
1, 52-54, 104-06, 156-59	NC	—	No Connect
2, 15-16, 41-42, 49-50, 56, 67-68, 83-84, 101-02, 108, 119-20, 126, 140, 154, 165, 184, 193, 204	V_{CC}	Power	Power Supply (+3.3V ±300mV)
55, 107, 208	V_{CCQ}	Power	Output Power Supply (+3.3 ±300mV)
3-4, 28-29, 43-44, 51, 61-62, 73, 82, 85, 96, 103, 113-14, 125, 127, 141, 155, 164, 183, 194, 203	V_{SS}	Power	Ground

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Absolute Maximum Ratings(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to V_{SS}	-0.5 to +3.9	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3606 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.3V.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 300mV
Industrial	-40°C to +85°C	0V	3.3V ± 300mV

3606 tbl 04

NOTE:
1. This is the parameter T_A.

Capacitance
(T_A = +25°C, f = 1.0MHz) PQFP ONLY

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 3dV	10	pF

3606 tbl 06

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

Recommended DC Operating Conditions(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc + 0.3(3)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

3606 tbl 05

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V or Vss – 0.3V.
3. V_{TERM} must not exceed V_{CC} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ VCC + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V400S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, $\overline{OE}$ = V_{IH}, $\overline{CTLEN}$ = V_{IH}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3606 tbl 07

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	77V400S155/6DSI		77V400S155/6DS		Unit
			Typ.	Max.	Typ.	Max.	
I_{CC}	Operating Current	V_{CC} = 3.6V, $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{CTLEN}$ = V_{IH}, RESET = V_{IL} or V_{IH}, f = fmax(1)	100	180	100	160	mA

3606 tbl 08

NOTE:
1. At f = f_{max} SCLK, ICLK, and OCLK are cycling at their maximum frequency and all inputs are cycling at 1/t_{CYC1}, using AC input levels of V_{SS} to 3.0V.

AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3606 tbl 09

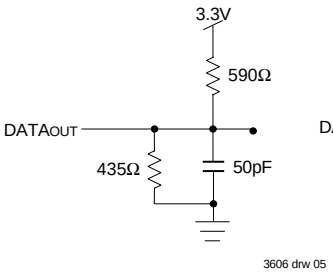

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Figure 1. AC Output Test Load

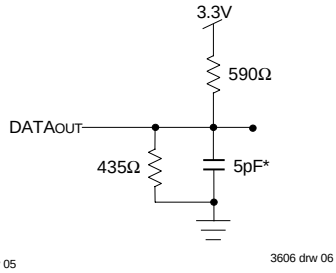

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Figure 2. Output Test Load
(for High-Impedance parameters)
* Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) (Vcc = 3.3V ± 0.3V)

		77V400S156 Com'l & Ind		77V400S155 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	System Clock Cycle Time	25	—	27	—	ns
t_{CH}	Systen Clock High Time	10	—	11	—	ns
t_{CL}	System Clock Low Time	10	—	11	—	ns
t_R	Clock Rise Time	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	ns
t_{SC}	$\overline{CS}$ Setup Time to SCLK High	4	—	4	—	ns
t_{HC}	$\overline{CS}$ Hold Time after SCLK High	1	—	1	—	ns
t_{SCM}	CMD Setup Time to SCLK High	4	—	4	—	ns
t_{HCM}	CMD Hold Time after SCLK High	1	—	1	—	ns
t_{SIO}	IOD Setup Time to SCLK High	4	—	4	—	ns
t_{HIO}	IOD Hold Time after SCLK High	1	—	1	—	ns
t_{CDIO}	SCLK to IOD Valid	—	18	—	20	ns
t_{DCIO}	IOD Output Hold after SCLK High	2	—	2	—	ns
t_{CYCI}	ICLK Cycle Time	23	—	23	—	ns
t_{CHI}	ICLK High Time	9	—	9	—	ns
t_{CLI}	ICLK Low Time	9	—	9	—	ns
t_{SIF}	IFRM Setup Time to ICLK High	4	—	4	—	ns
t_{HIF}	IFRM Hold Time after ICLK High	1	—	1	—	ns
t_{SID}	ID Setup Time to ICLK High	4	—	4	—	ns
t_{HID}	ID Hold Time after ICLK High	1	—	1	—	ns
t_{OE}	$\overline{OE}$ Low to Data Valid	—	15	—	15	ns
t_{OHZ}	$\overline{OE}$ High to Output High-Z[1]	—	15	—	15	ns
t_{OLZ}	$\overline{OE}$ Low to Output Low-Z[1]	2	—	2	—	ns
t_{RST}	RESET High Pulse Width[2]	20	—	20	—	ns
t_{RSTL}	RESET Low to SCLK High	10	—	10	—	ns
t_{CTEN}	$\overline{CTLEN}$ Low to Data Valid	—	15	—	15	ns
t_{CTHZ}	$\overline{CTLEN}$ High to Output High-Z[1]	—	15	—	15	ns
t_{CTLZ}	$\overline{CTLEN}$ Low to Output Low-Z[1]	2	—	2	—	ns
t_{CDCR}	SCLK to $\overline{CRCERR}$ Valid (1 cycle delay)	—	18	—	20	ns
t_{DCCR}	$\overline{CRCERR}$ Output Hold after SCLK High	2	—	2	—	ns
t_{CYCO}	OCLK Cycle	23	—	23	—	ns
t_{CHO}	OCLK High Time	9	—	9	—	ns
t_{CLO}	OCLK Low Time	9	—	9	—	ns
t_{SOF}	OFRM Setup Time to OCLK High	4	—	4	—	ns
t_{HOF}	OFRM Hold Time after OCLK High	1	—	1	—	ns
t_{CDOF}	OCLK to OFRM Valid	—	15	—	18	ns
t_{CDOF}	OFRM Output Hold after OCLK High	2	—	2	—	ns
t_{CDOD}	OCLK to OPxD Valid	—	15	—	18	ns
t_{DCOD}	OD Output Hold after OCLK High	2	—	2	—	ns
t_{CKHZ}	SCLK High to Output High-Z[1]	—	15	—	15	ns
t_{CKLZ}	SCLK High to Output Low-Z[1]	2	—	2	—	ns

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NOTES:

1. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. Although RESET is an asynchronous function, it must be centered around the SCLK so that it will be Low 10ns prior to the next SCLK rising edge to prevent initiating another Reset operation.

Basic Functional Description

Input data is received by the Switching Memory via the four-bit input data ports (IPxD). Each input port is configured as a double buffer with SRAM storage for two complete ATM cells. Each input port also has an independent input clock, (ICLK) and an input framing signal (IFRM).

The external controller may poll the internal status register through the Control Data Bus (IOD Bus) to determine if any of the eight input SAMs (ISAMx) are full and any of the eight Output SAMs (OSAMx) are empty. The status register accessed through the IOD Bus also provides ISAM error status information. If an error is detected for any of the ISAMs, the error register can then be read through the IOD Bus to further determine the presence of short or long cells or SAM overflow. OFRM may also be used to monitor OSAM status.

Upon a Store command, data from the selected ISAM is transferred to the cell memory at the location selected by the controller on the IOD Bus. Similarly, on a Load command data from the specified cell memory location is transferred to the OSAMx specified by the controller on the IOD Bus. The output ports are also individually double buffered and each output port can hold up to two complete ATM cells. A cell output ready signals the status register to allow the loading of the second buffer to begin while the first buffer begins to transmit via the 4-bit output port. Each output port has an independent clock (OCLKx) and output framing signal (OFRMx).

Once a cell has been received in the ISAM, the header bytes and the pre/post-pend bytes, if enabled, may be examined and modified via the IOD bus. The CRC byte may also be modified, although it is modified internally to the switching memory and is not read on the IOD Bus. The IOD Bus is also used to set the internal configuration register at initialization, determining the input and output cell length and the input and output port configurations. The input edit buffer provides the means to modify the cell header or pre/post-pend data of a cell in the ISAM before storing the cell in the Fusion Memory portion of the IDT77V400. The command selected (GHE or GPE, for example) will determine which bits are transferred to the control logic across the IOD bus. Two features are included to eliminate the need for an extra step in the edit sequences of the input edit buffer. A Byte Protect function, which prevents a PUT instruction from changing any protected bytes stored in the input edit buffer, and a Clear Byte function, which clears bytes in the input edit buffer in preparation for ORing at the output, are described in the Input Ports section of this data sheet. See the Input and Output Edit Buffer Block Diagram for additional details of the functionality and data path of this circuitry.

The output edit buffer provides a means to modify the cell contents at the last possible moment prior to transmission of a cell out an output port. The output edit buffer provides data to an OR function between the Fusion Memory and the OSAMs, allowing the IOD bus to set selected bits in the cell header and pre/post pend data immediately before transmission.

The following basic functional description is divided into three sections—the control interface, the input ports, and the output ports. For clarity we will use an 8x8 Switching Memory configuration, with each port being 4-bits wide. Higher port bandwidth can be obtained by combining multiple 4-bit wide ports into 8, 16, or 32-bit wide ports during device initialization and configuration (see Configruation Codes Table).

Control Interface

The control interface consists of 48 pins. The 32-bit control data bus (IOD0-31) is used to transfer address, data, and header information. The 6-bit command bus (CMD0-5) is used when $\overline{CS}$ is LOW to issue commands to the Switching Memory. When $\overline{CS}$ is HIGH, all issued commands become invalid (no operation is performed) (see the Control Interface Command Table for a listing of commands). The $\overline{CRCERR}$ output pin indicates that a CRC error has occurred on the last header when asserted LOW. The asynchronous $\overline{OE}$ input pin is the master output enable for all outputs; all output drivers will be in a high-impedance state when $\overline{OE}$ is driven HIGH. Upon power-up initialization the $\overline{OE}$ pin should be held HIGH and the RESET pin should be asserted HIGH to allow proper device initialization by the controller. The asynchronous $\overline{CTLEN}$ input pin controls the Control Interface outputs. When the $\overline{CTLEN}$ pin is LOW, the $\overline{OE}$ pin is LOW, and the $\overline{CTLEN}$ bit of the configuration register is LOW, the Control Interface outputs are enabled. If the $\overline{CTLEN}$ pin or the $\overline{CTLEN}$ bit of the configuration register is HIGH, all control Interface outputs will be in the High-Z state(see Control Enable Timing Waveform). The ADDR0-3 pins are used in conjunction with the configuration register to selectively enable Switching Memories that are sharing a control bus. All inputs and outputs of the control interface, with the exception of $\overline{OE}$, RESET, and ADDR0-3 are synchronous with the system clock input (SCLK).

As shown in the Control Interface Timing Waveform, the control interface provides access to five internal registers — the configuration register, the status register, the error register, the input edit buffers, and the output edit buffers. The control interface is implemented as a pipeline. Commands are registered on the rising edge of SCLK, and in general, the Switching Memory either expects data or will output data on IOD0-31 on the subsequent SCLK rising edge. The Control Interface Protocol Waveform shows an example of this protocol for the GHI (Get Header from ISAMx) and GST (Get Status Register) instructions.

The bus width and clock rate of the control interface has been carefully matched to the internal bandwidth of the Switching Memory, and to the control requirements for high-speed multiport traffic. Additionally, many of the commands which require multiple SCLK cycles to execute, allow other commands to overlap the command cycles. In this manner, the commands can be pipelined. The control interface of the Switching Memory provides sufficient bandwidth to keep pace with the control operations required of all sixteen data ports, the memory refresh activities, and the other associated overhead.

Control Interface Commands(1)

		COMMAND Bus Bit (CMD5:0)					
		MSb					LSb
Command	Command Description	5	4	3	2	1	0
GPIx	Get Pre/Post Pend Data from ISAMx(2)	0	0	0	n(3)	n(3)	n(3)
GHIx	Get Header from ISAMx(2)	0	0	1	n(3)	n(3)	n(3)
GPE	Get Pre/Post Pend Data from Edit Buffer	0	1	0	0	0	0
GHE	Get Header from Edit Buffer	0	1	0	1	0	0
GST	Get ISAM and OSAM Status Register Bits	0	1	0	0	1	0
GER	Get Error Register Bits	0	1	0	1	1	0
STEx	Store Cell in ISAMx(2) and Input Edit Buffer in Memory	1	0	0	n(3)	n(3)	n(3)
STIx	Store Cell in ISAMx(2) in Memory	1	0	1	n(3)	n(3)	n(3)
LDOx	Load Cell from Memory into OSAMx(2)	1	1	0	n(3)	n(3)	n(3)
PPE	Put new Pre/Post Pend in Input Edit Buffer	1	1	1	0	0	0
PHE	Put new Header in Input Edit Buffer	1	1	1	1	0	0
PHEC	Put new Header and new CRC byte in Input Edit Buffer	1	1	1	1	0	1
REF	Refresh Fusion Memory	0	1	0	1	1	1
LDC	Load Configuration Register	1	1	1	0	1	0
OPE	Put Pre/Post Pend Data in Output Edit Register	1	1	1	0	1	1
OHE	Put new Header in Output Edit Register	1	1	1	1	1	0
OHEC	Put new Header and new CRC byte in Output Edit Register	1	1	1	0	0	1
NOP	No Operation	1	1	1	1	1	1

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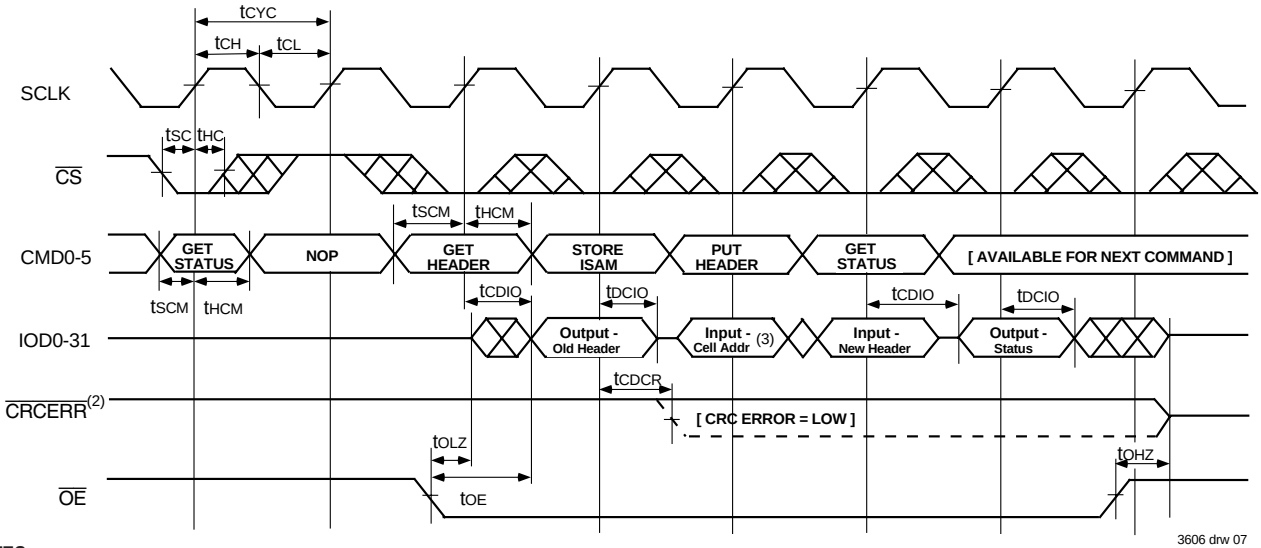
NOTES:
1. CMD bus commands not defined in this table are undefined and not to be implemented.
2. "x" represents the specific ISAM or OSAM being accessed (IP0-IP7 or OP0-OP7 respectively).
3. "n" represents the appropriate bit of the binary representation of the ISAM or OSAM being accessed (000 to 111).

Control Interface Timing Waveform(1)



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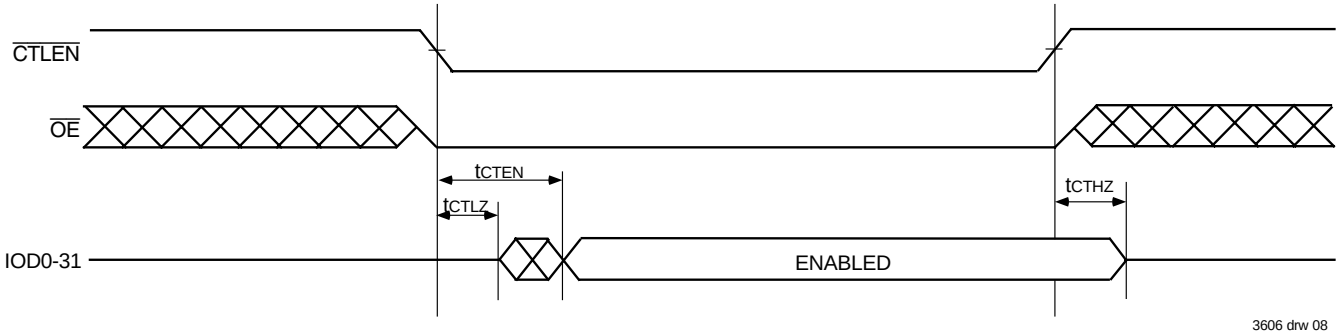
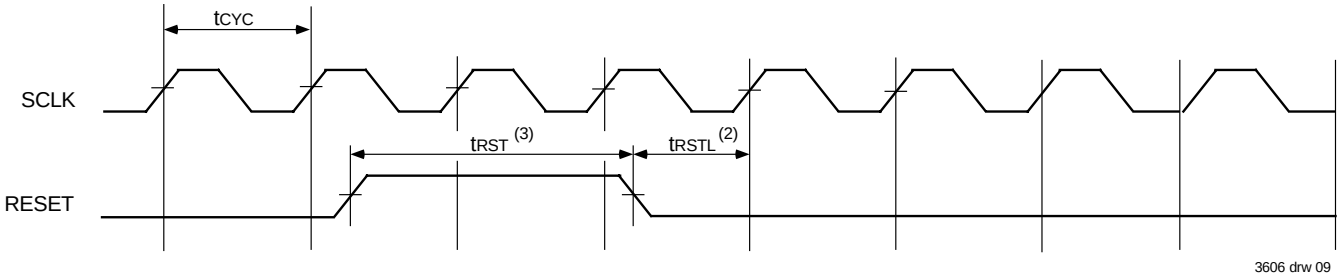
NOTES:
1. $\overline{\text{CTLEN}}$ is LOW and the $\overline{\text{CTLEN}}$ bit of the configuration register (Bit 31) is LOW for this waveform.
2. All output signals except $\overline{\text{CRCERR}}$ are controlled by OE.
3. The 13-bit cell address, 4-bit selected Switching Memory address, and the 5-bit Edit Buffer Protect and Clear control bits are valid at this time.

Control Enable Timing Waveform(1)



NOTE:
1. The CTLEN bit of the configuration register (Bit 31) is LOW for this waveform. If the CTLEN bit of the configuration register is set HIGH at device initialization the IOD bus will always be in input mode for multiple Switching Memory configurations.

Reset Waveform(1)



NOTES:
1. Reset function can also be accomplished by holding the RESET bit [Bit 30] HIGH on the IOD bus during a LDC (Load Configuration Register) command.
2. RESET must be LOW 10ns prior to the next rising SCLK edge to insure that the Reset function is not repeated.
3. tRST must be greater than two SCLK cycles. Any glitch could cause an erroneous reset operation.

Input Ports

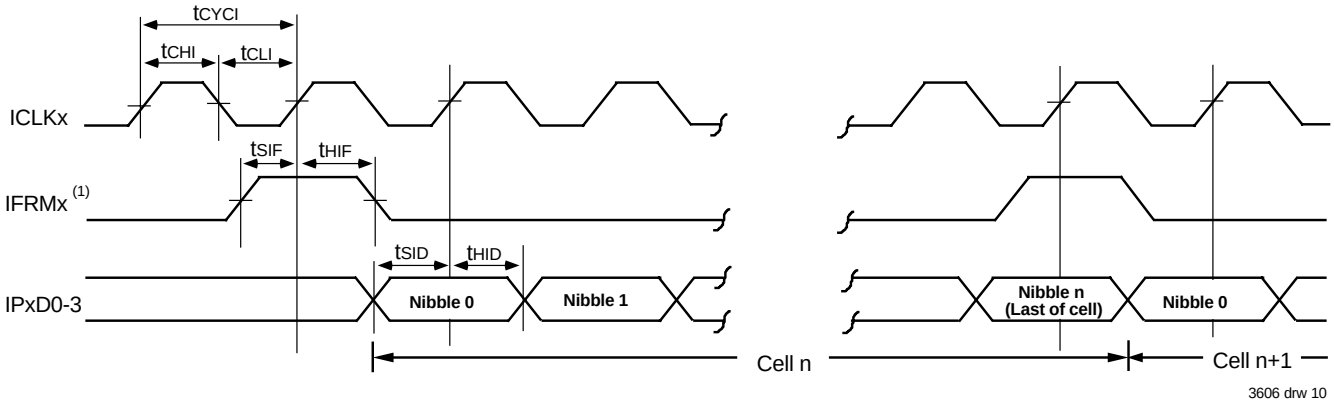
A 155Mbps input Data Path Interface(DPI) consists of six pins – four data bits (IPxD0-3), an input clock (ICLKx), and an input framing signal (IFRMx). A further definition of the DPI interface is available in Technical Note 34, available on the IDT Web Site (www.idt.com). The "x" in the signal name corresponds to a port number (0 through 7 for the 8 x 8 port configuration). IPxD0-3 and IFRMx are synchronous inputs with respect to the rising edge of ICLKx. Each Input SAM (ISAMx) is double buffered, with each ISAM buffer able to store a single ATM cell of up to 56 bytes in length. The 32-bit Header and up to 32 bits of Pre-Pend and/or Post-Pend bytes may be accessed and modified via the Control Data Bus interface.

The Input Port Timing Waveform assumes that the Switching Memory has been initialized and the ISAMs are empty. An active HIGH IFRMx signal indicates that the first nibble of a new cell will be received on the next rising edge of ICLKx and the cell counter is initialized. Data will be sequentially clocked into the ISAM buffer on each subsequent ICLKx rising edge after IFRMx goes LOW. The status register bit indicating ISAMx buffer is full will be set HIGH when the ISAM counter reaches the stop address. The ISAM start and stop address is programmed via the configuration register at initialization to establish the input cell length and protocol. If IFRMx input goes HIGH before the stop position address is reached, the start byte position address will be reloaded, the ISAM Full Status indicator will not be set, a Short Cell error status indicator will be set in the error register, and the cells will be overwritten. If the IFRMx does not go HIGH when the stop position address is reached, the ISAM Full status indicator and a Long Cell error status indicator will be set. A Long Cell error results in the begining portion of the long cell being kept, the last portion being discarded, and the next cell being accepted in the other half of the ISAM on the next IFRMx HIGH. When the IFRMx input stays HIGH, the load start byte position address process will repeat for every ICLKx and the actual count will not start until IFRMx goes LOW. A subsequent cell may be input back-to-back (no dead cycle on the IOD bus). In this case the IFRMx of the second cell will occur on the same ICLKx rising edge as the last data nibble of the first cell.

When the control logic returns 32-bits of information across the IOD bus during a STORE command, the five most significant bits provide the Byte Edit control for the first word of the input edit buffer. These four bytes are either cleared, protected, or unaffected depending on the value of the bits IOD27-31. These five bits are updated each time a STORE command is executed. IOD31 determines if the function is clear or protect; IOD 27-30 select which bytes in the first word of the Input edit buffer are affected. The Edit Buffer Protect/Clear Codes table defines the possible combination of these bits.

Each of the eight 4-bit input ports is capable of receiving 155Mbps data; however, the ports can be combined in groups of four bits to receive data rates up to 1.24Gbps. For example, four 4-bit ports can be combined to receive 622Mbps traffic. The output ports can also be combined, via the configuration register, independent of the input data ports. This allows the Switching Memory to be configured as a concentrator, expander, or cell buffer with multiple bus widths. When combining ports, the chip is internally reconfigured to accept a single master ICLK for the grouped ports (always using the least significant ICLK/IFRM of those combined), and the datapath is internally switched to correctly align the ports for CRC generation and Header/Pre-Post Pend comparison. See the Port Configuration Code Table for option definitions. By varying the input and output port options, one hundred different port configurations are available to the user to optimize design flexibility.

Input Port Timing Waveform



NOTE:
1. t_{SIF} and t_{HIF} (ICLK Setup and Hold) must be met for each ICLK rising edge for IFRM LOW and HIGH.

Output Ports

The output data ports are similar in operation to the input data ports. There are eight 155Mbps DPI ports, six pins each. Data is transmitted out the 4-bit data bus (OPxD0-3), synchronous with the output clock (OCLKx). An output framing signal (OFRMx) is provided which is also synchronous with respect to OCLKx.

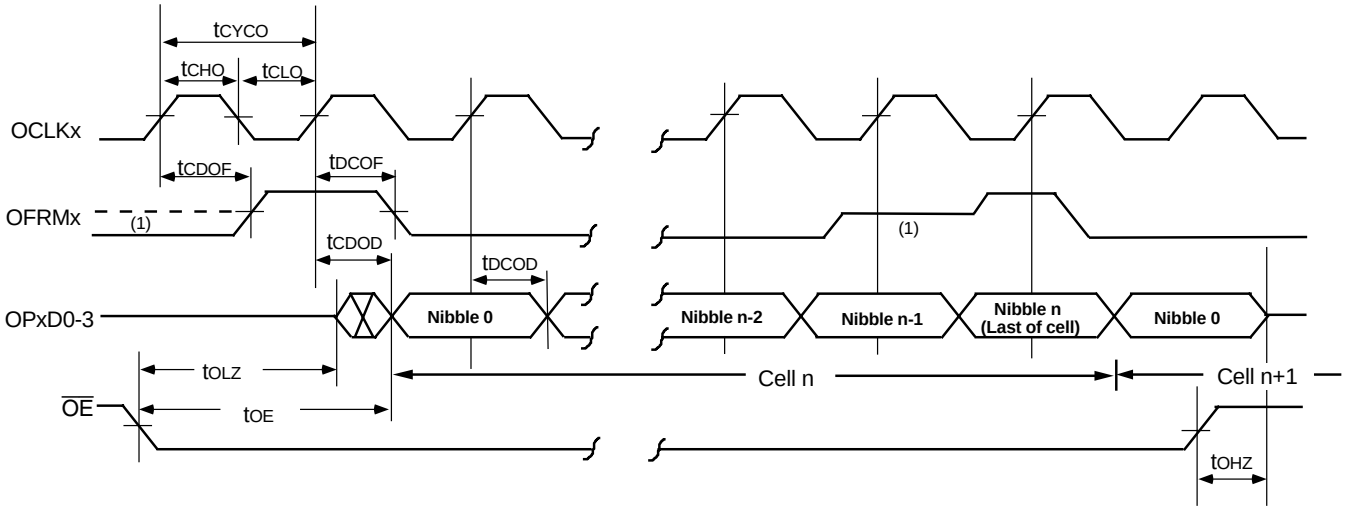
The output port protocol was designed to interface directly with the input port of another Switching Memory without requiring additional logic. This allows cascading of multiple Switching Memory chips to implement wider multiplexers or larger capacity cell buffers without additional logic. To facilitate cascading, OFRMx has been implemented as a tri-statable I/O, while OPxD pins are tri-statable outputs. All chip outputs can be disabled to a high impedance state by asserting the $\overline{OE}$ pin HIGH.

Output ports of a single device or of multiple devices may share an output bus if they are configured in the cell bus mode, where control logic performs the arbritration between IDT77V400s, or are externally controlled via the $\overline{OE}$. In the cell bus mode configuration, one external controller would typically drive the control interface of multiple Switching Memory chips and use the OFRMx to arbitrate the shared bus.

Output SAM (OSAMx) control logic must receive a LDx (Load OSAMx) instruction from the external controller via the Command Bus to dispatch a cell. The LDx instruction initiates a cell transfer from the memory location specified on the IOD Bus to the specified OSAMx. At this point the user has the option of modifying the Header and the Pre-Post Pend bytes. When the output buffer has a cell loaded to send, Switching Memory will immediately assert the specific OFRMx HIGH for one OCLKx cycle prior to transmitting data. When the OFRMx is then asserted LOW, the first data nibble of the new cell will appear prior to the next rising edge of OCLKx. The output port will continue to assert OFRMx LOW (while the cell is output from OSAMx) for a minimum of two cycles before the end of the cell transmission. At that time (if in cell bus mode) OFRMx is released to a high-impedance state during the cycle before the end of the frame to allow collision free control transfer to another Switching Memory. After asserting OFRMx HIGH, the OSAMx EMPTY bit in the status register will be set, indicating that an OSAM buffer is available for a new cell to be loaded from the memory. The EMPTY bit is reset when a LDx command is performed and after the cell is transmitted. It is recommended that a pull down resistor be used on OFRMx pin to eliminate the possibility of an invalid OFRMx HIGH. The value of this pull down resistor will be determined by a specific board design or noise issues. A 5KΩ resistor is recommended for this pull down function, although 50-100KΩ may be sufficient in most applications.

The OFRM pin is always monitored internally by the Switching Memory. The OFRMx output is released to a High-impedance state when it is in cell bus mode and a cell is not ready for dispatch. Upon receiving a HIGH OFRMx input, the Switching Memory will hold if a transmission was beginning. When an output port asserts OFRMx HIGH all of Switching Memories on the bus, including the transmitting Switching Memory, reset the internal start of frame count. The transmitting IDT77V400 then places the data on the output bus and all Switching Memories on the bus count to the end of the frame. If OFRMx is an output, the internal OSAMx counter is set to the starting address. The counter will count up to the stop address for each subsequent OCLKx rising edge after OFRMx goes LOW. In this manner, all devices sharing the output bus must be set to the same nibble count. If a Switching Memory receives a LDx command while any port is transmitting on the output bus, it will continue counting and wait for the stop address to be reached before asserting OFRMx and dispatching a cell. This will avoid collisions on the bus; however, it is the responsibility of the external controller to issue only one LDx command for a shared cell bus within a single cell transmit time.

Output Port Timing Waveform



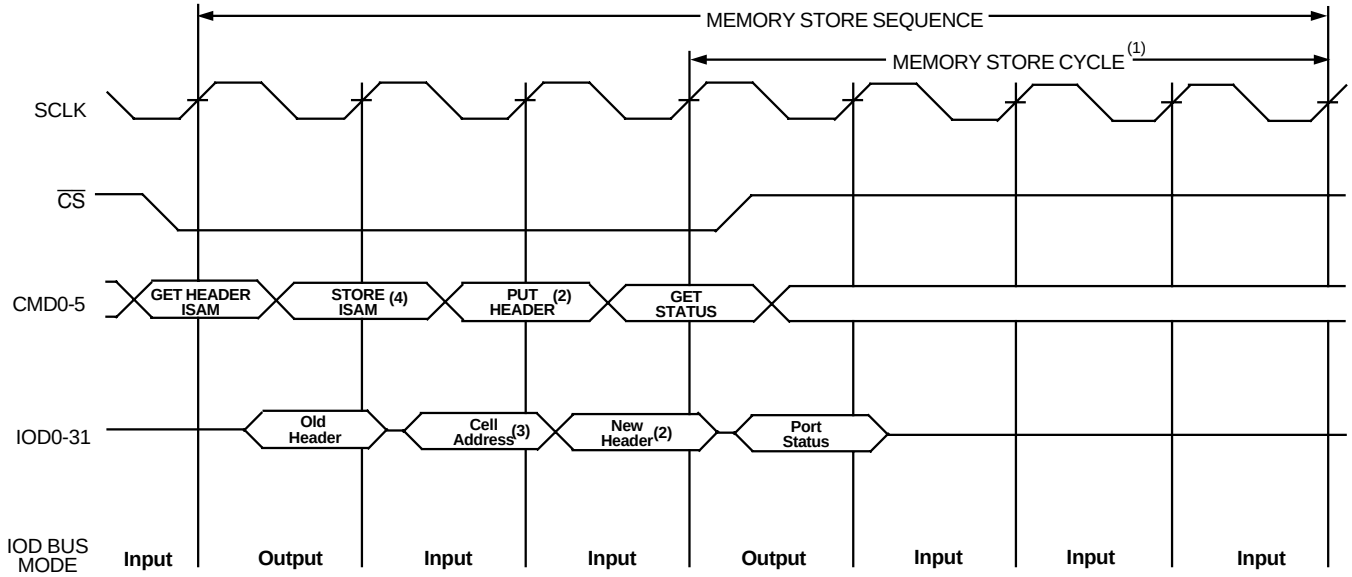
3606 drw 11

NOTE:

1. OFRMx is actually tri-stated by the device one cycle before the end of the frame; the logic LOW level is due to the recommended 5k ohm resistor on the OFRMx line.

Functional Waveforms

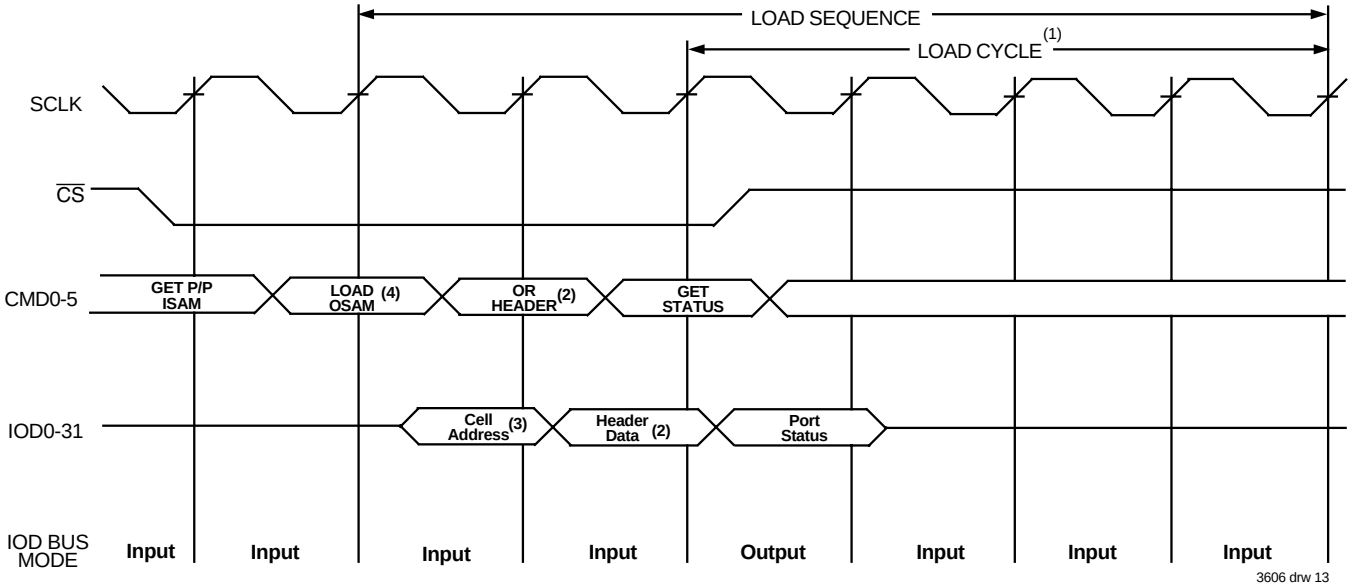
Functional Waveform - Store Instruction Sequence



3606 drw 12

NOTES:
1. The Memory Store Cycle requires four cycles to write the cell from the ISAM to the Fusion Memory.
2. The PPE or PHEC commands can be executed at this point in the sequence instead of the PHE command. The IOD bus would then reflect the appropriate bytes in the cell based on the command used.
3. The 13-bit cell address, 4-bit selected Switching Memory address, and 5-bit Edit Buffer Protect and Clear control bits are valid at this time.
4. STORE ISAM command can only be valid for one cycle during a Memory Store Cycle. Issuing more than one STORE ISAM will cause Fusion Memory write failure.

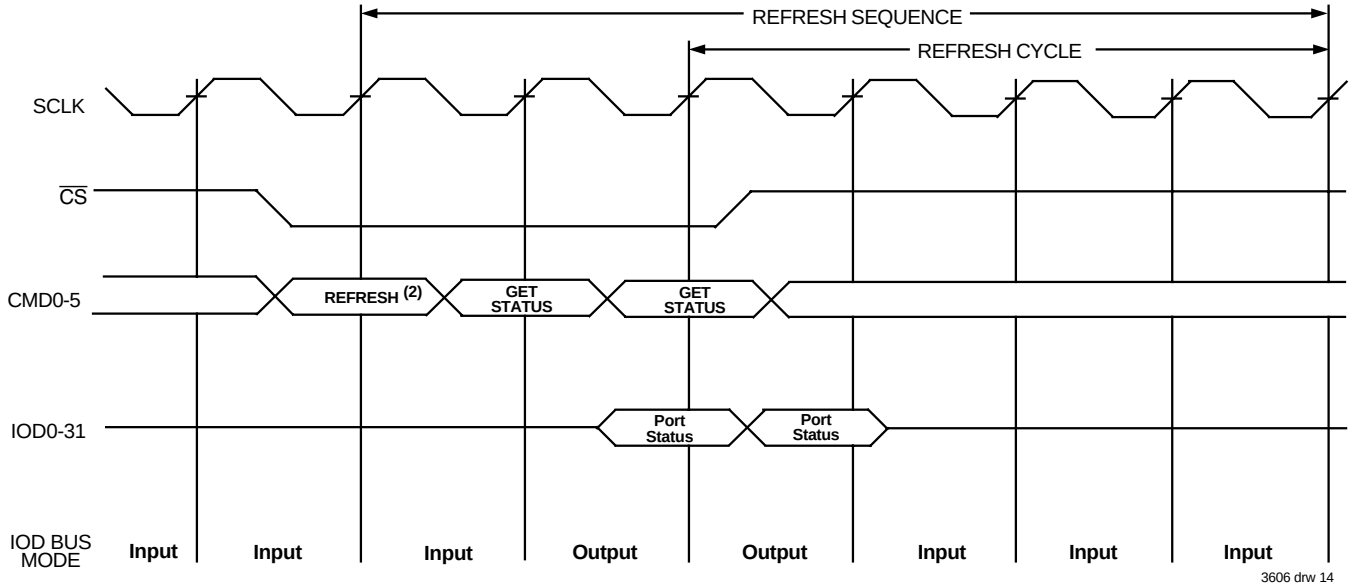
Functional Waveform - Load Instruction Sequence



3606 drw 13

NOTES:
1. The Memory Load Cycle requires four cycles to write the cell from the Fusion Memory to the OSAM.
2. The OPE or OHEC commands can be executed at this point in the sequence instead of the OHE command. The IOD bus would then reflect the appropriate cell bytes based on the command used.
3. The 13-bit cell address and 4-bit selected Switching Memory address are valid at this time
4. LOAD OSAM command can only be valid for one cycle during a Load Sequence. Issuing more than one LOAD OSAM will cause Fusion Memory read failure.

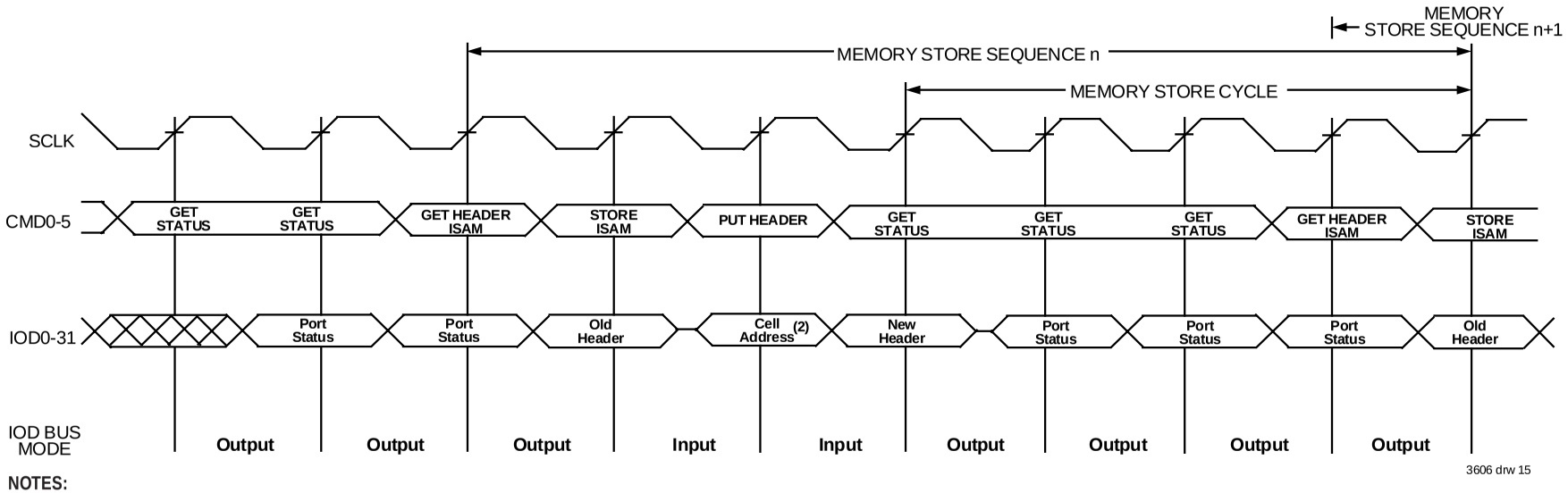
Functional Waveform - Refresh Sequence(1)



NOTES:

1. The Refresh sequence begins with the REF command and ends when the four cycle Fusion Memory Refresh has completed.
2. REFRESH command can only be valid for one cycle during a Refresh Sequence. Refresh must be completed prior to another command to avoid data corruption.

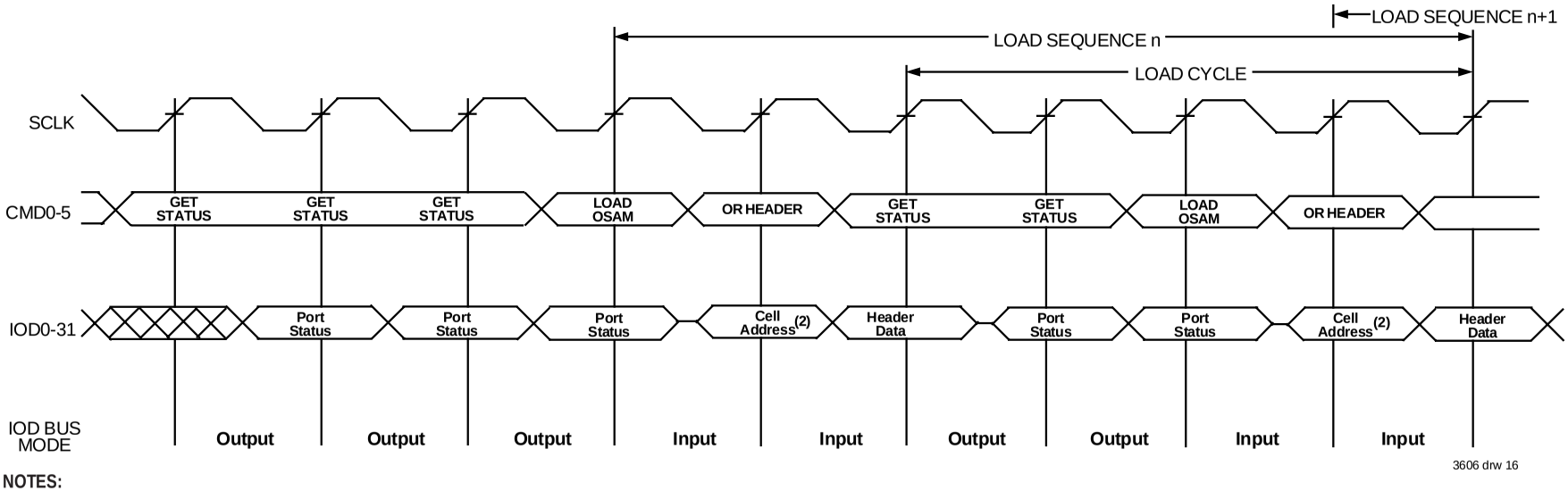
Multi-Sequence Functional Waveform Example - Idle, Memory Store, Initiate Memory Store(1)



3606 drw 15

NOTES:
1. $\overline{CS}$ is LOW.
2. The 13-bit cell address and 4-bit selected Switching Memory address and 5-bits Edit Buffer Protect and Clear control bits are valid at this time.

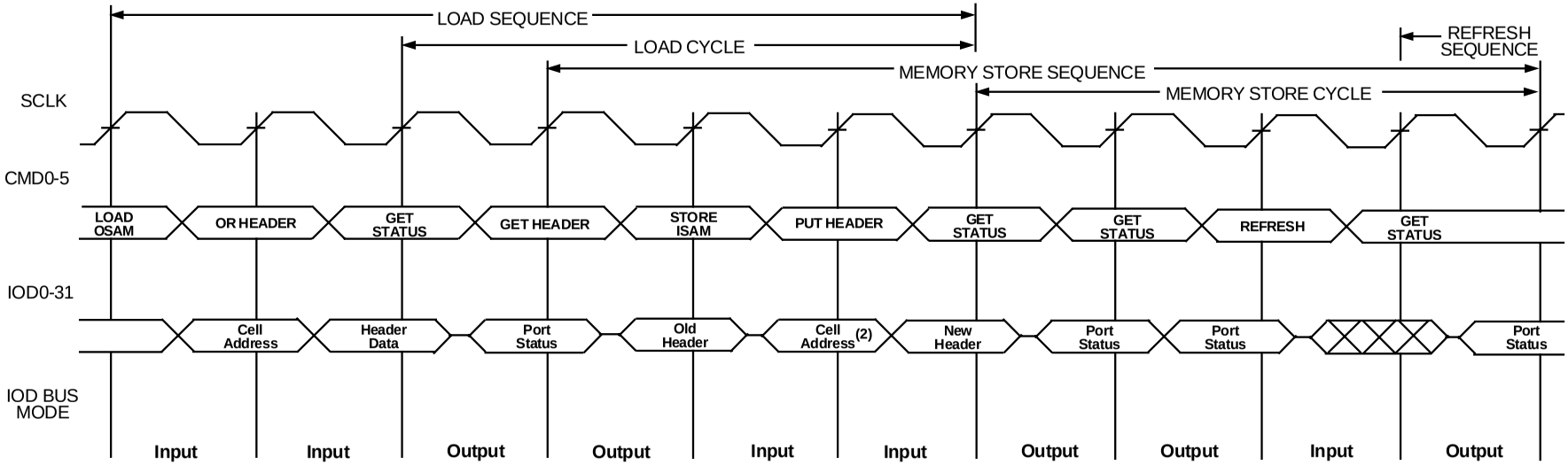
Multi-Sequence Functional Waveform Example - Idle, Load, Initiate Load(1)



3606 drw 16

NOTES:
1. $\overline{CS}$ is LOW.
2. The 13-bit cell address and 4-bit selected Switching Memory address are valid at this time.

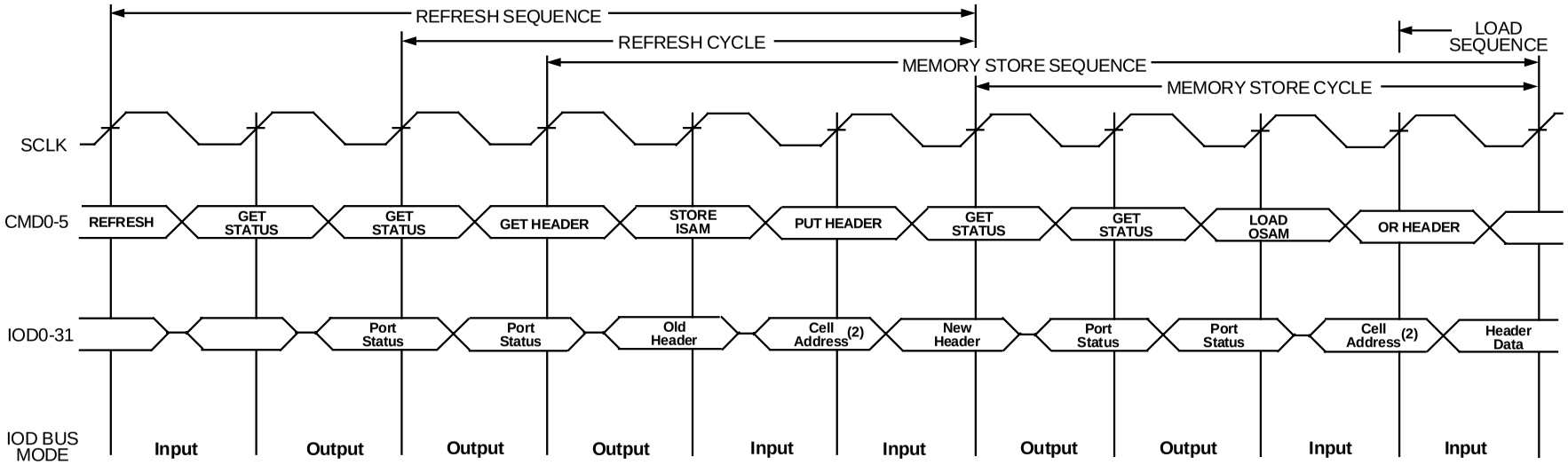
Multi-Sequence Functional Waveform Example - Load, Memory Store, Initiate Refresh(1)



3606 drw 17

NOTES:
1. $\overline{CS}$ is LOW.
2. The 13-bit cell address and 4-bit selected Switching Memory address and 5-bits Edit Buffer Protect and Clear control bits are valid at this time.

Multi - Senquence Functional Waveform Example - Refresh, Memory Store, Initiate Load(1)



3606 drw 18

NOTES:
1. $\overline{CS}$ is LOW.
2. The 13-bit cell address and 4-bit selected Switching Memory address and 5-bits Edit Buffer Protect and Clear control bits are valid at this time.

Configuration Register Definition[1]

Register Bits	Field Name	Field Description
0-3	ISAM Configuration	Four bit configuration code for the input ports as defined in the Table of configuration codes.
4-7	OSAM Configuration	Four bit configuration code for the output ports as defined in the Table of configuration codes.
8-10	ISAM Start	Three bit starting byte position for the ISAMs.
11-16	ISAM Stop	Six bit stop byte position for the ISAMs.
17-19	OSAM Start	Three starting byte position for the OSAMs.
20-25	OSAM Stop	Six bit stop byte position for the OSAMs.
26-29	Chip Address	Four bit field for multiple device configurations.
30	Reset[2]	One bit used to reset the status and output waiting bits.
31	$\overline{\text{CTLEN}}$	One bit used for the Control Interface outputs during parallel operation.

3606 tbl 12

NOTES:
1. Configuration Register Bit number corresponds to the same bit position on the IOD bus. Bit 0 is the LSb bit; bit 31 is the MSb.
2. This bit is not stored in the Configuration Register. It must be asserted on the IOD bus to generate asynchronous reset operation.

Port Configuration Codes[1,2]

CONFIG CODE	PORT CONFIGURATION							
MSb LSb	0	1	2	3	4	5	6	7
0000	4 bit	4 bit	4 bit	4 bit	4 bit	4 bit	4 bit	4 bit
0001	8 bit, CLK/FRM 0		4 bit	4 bit	4 bit	4 bit	4 bit	4 bit
0010[3]	4 bit	4 bit	4 bit	4 bit	4 bit	4 bit	8 bit, CLK/FRM 6	
0011	8 bit, CLK/FRM 0		8 bit, CLK/FRM 2		4 bit	4 bit	4 bit	4 bit
0100[3]	4 bit	4 bit	4 bit	4 bit	8 bit, CLK/FRM 4		8 bit, CLK/FRM 6	
0101	8 bit, CLK/FRM 0		8 bit, CLK/FRM 2		8 bit, CLK/FRM 4		4 bit	4 bit
0110[3]	4 bit	4 bit	8 bit, CLK/FRM 2		8 bit, CLK/FRM 4		8 bit, CLK/FRM 6	
0111	8 bit, CLK/FRM 0		8 bit, CLK/FRM 2		8 bit, CLK/FRM 4		8 bit, CLK/FRM 6	
1000[3]	4 bit	4 bit	4 bit	4 bit	16 bit, CKL/FRM 4			
1001	16 bit, CLK/FRM 0				4 bit	4 bit	4 bit	4 bit
1010[3]	4 bit	4 bit	8 bit, CKL/FRM 2		16 bit, CLK/FRM 4			
1011	16 bit, CLK/FRM 0				8 bit, CLK/FRM 4		4 bit	4 bit
1100[3]	8 bit, CLK/FRM 0		8 bit, CLK/FRM 2		16 bit, CLK/FRM 4			
1101	16 bit, CLK/FRM 0				8 bit, CLK/FRM 4		8 bit, CLK FRM 6	
1110	16 bit, CLK/FRM 0				16 bit, CLK/FRM 4			
1111	32 bit, CLK/FRM 0							

3606 tbl 13

NOTES:
1. Configuration codes are used to initially configure the IDT77V400. These codes are applicable to both the input and output ports, and do not have to be configured the same for both input and output ports.
2. The Data Path Interface (DPI) used by the input and output ports provides the option to combine the four bit data widths together to achieve a higher bandwidth port. The entries in the table are expressed in bus width, and represent the following maximum data rates per port based on ICLK or OCLK frequency:
   4 bit: 155Mbps • 8 bit: 311Mbps • 16 bit: 622Mbps • 32 bit: 1.24Gbps
   When four bit busses are combined to obtain a higher bandwidth port, the specific CLK and FRM pin to be used for the new wider port is specified. If not specified the CLK and FRM pins match the port number. It is suggested that unused ICLK and IFRM pins be pulled up to Vcc through a resistor, and that unused OCLK and OFRM pins be pulled down to Vss through a resistor. The resistor value is not critical; 5K ohm or less is recommended.
3. This configuration is not supported by the IDT77V500 Switch Controller. Please use the alternate port assignment option immediately prior to this one in the Port Configuration Codes table.

Status Register Definition

Register Bit	Port	ISAM Full (1)	ISAM Error (2)	OSAM Empty (3)	CRC Error (4)
IOD0	0	X	—	—	—
IOD1	0	—	X	—	—
IOD2	1	X	—	—	—
IOD3	1	—	X	—	—
IOD4	2	X	—	—	—
IOD5	2	—	X	—	—
IOD6	3	X	—	—	—
IOD7	3	—	X	—	—
IOD8	4	X	—	—	—
IOD9	4	—	X	—	—
IOD10	5	X	—	—	—
IOD11	5	—	X	—	—
IOD12	6	X	—	—	—
IOD13	6	—	X	—	—
IOD14	7	X	—	—	—
IOD15	7	—	X	—	—
IOD16	0	—	—	X	—
IOD17	1	—	—	X	—
IOD18	2	—	—	X	—
IOD19	3	—	—	X	—
IOD20	4	—	—	X	—
IOD21	5	—	—	X	—
IOD22	6	—	—	X	—
IOD23	7	—	—	X	—
IOD24	0	—	—	—	X
IOD25	1	—	—	—	X
IOD26	2	—	—	—	X
IOD27	3	—	—	—	X
IOD28	4	—	—	—	X
IOD29	5	—	—	—	X
IOD30	6	—	—	—	X
IOD31	7	—	—	—	X

3606 tbl 14

NOTES:
1. Logic 1 (HIGH) indicates the ISAM is full.
2. Logic 1 (HIGH) indicates an ISAM error. Error register should be accessed to identify type of error.
3. Logic 1 (HIGH) indicates the OSAM is empty.
4. Logic 1 (HIGH) indicates CRC error on the ISAM.

Error Register Definition(1)

Register Bit	Port	ISAM Short Cell Error	ISAM Long Cell Error	ISAM Overflow
IOD0	0	X	—	—
IOD1	0	—	X	—
IOD2	0	—	—	X
IOD3	1	X	—	—
IOD4	1	—	X	—
IOD5	1	—	—	X
IOD6	2	X	—	—
IOD7	2	—	X	—
IOD8	2	—	—	X
IOD9	3	X	—	—
IOD10	3	—	X	—
IOD11	3	—	—	X
IOD12	4	X	—	—
IOD13	4	—	X	—
IOD14	4	—	—	X
IOD15	5	X	—	—
IOD16	5	—	X	—
IOD17	5	—	—	X
IOD18	6	X	—	—
IOD19	6	—	X	—
IOD20	6	—	—	X
IOD21	7	X	—	—
IOD22	7	—	X	—
IOD23	7	—	—	X
IOD24-31	N/A	—	—	—

3606 tbl 15

NOTE:
1. When the Register Bit is a logic 1(High), the type of error is indicated by an "X".

RAM Address Definition(1)

IOD Bit	Description
0-12	Cell address in Fusion Memory
13-16	Switching Memory ID address (in multiple 77V400 device configurations)
17-26	Unused
27-31	Edit Buffer Protect/Clear Control Bits(2)

3606 tbl 16

NOTES:
1. Used for Store Commands (STEx, STIx) and Load Command (LDOx).
2. Updated during STEx and STIx operation.

Edit Buffer Protect/Clear Codes(1)

IOD Bit					
31 Mode	30 Byte 0(1)	29 Byte 1(1)	28 Byte 2(1)	27 Byte 3(1)	Description
0	0	0	0	0	No Bytes Selected - No Bytes Cleared
0	0	0	0	1	Clear Byte 3
0	0	0	1	0	Clear Byte 2
0	0	0	1	1	Clear Bytes 2 and 3
0	0	1	0	0	Clear Byte 1
0	0	1	0	1	Clear Bytes 1 and 3
0	0	1	1	0	Clear Bytes 1 and 2
0	0	1	1	1	Clear Bytes 1, 2 and 3
0	1	0	0	0	Clear Byte 0
0	1	0	0	1	Clear Bytes 0 and 3
0	1	0	1	1	Clear Bytes 0 and 2
0	1	0	1	1	Clear Bytes 0, 2 and 3
0	1	1	0	0	Clear Bytes 0 and 1
0	1	1	0	1	Clear Bytes 0, 1 and 3
0	1	1	1	0	Clear Bytes 0, 1 and 2
0	1	1	1	1	Clear Bytes 0, 1, 2 and 3
1	0	0	0	0	No Bytes Selected - No Protection Done
1	0	0	0	1	Protect Byte 3
1	0	0	1	0	Protect Byte 2
1	0	0	1	1	Protect Byte 2 and 3
1	0	1	0	0	Protect Byte 1
1	0	1	0	1	Protect Bytes 1 and 3
1	0	1	1	0	Protect Bytes 1 and 2
1	0	1	1	1	Protect Bytes 1, 2 and 3
1	1	0	0	0	Protect Byte 0
1	1	0	0	1	Protect Bytes 0 and 3
1	1	0	1	1	Protect Bytes 0 and 2
1	1	0	1	1	Protect Bytes 0, 2 and 3
1	1	1	0	0	Protect Bytes 0 and 1
1	1	1	0	1	Protect Byes 0, 1 and 3
1	1	1	1	0	Protect Byes 0, 1 and 2
1	1	1	1	1	Protect Bytes 0, 1, 2 and 3

3606 tbl 17

NOTE:
1. Byte 0 represents bits 0-7 of the Input Edit Buffer
   Byte 1 represent bits 8-15 of the Input Edit Buffer
   Byte 2 represent bits 16-23 of the Input Edit Buffer
   Byte 3 represent bits 24-31 of the Input Edit Buffer
   Bit 31 is the MSb of the Input Edit Buffer

Cell Alignment Options[1]

Cell Configuration	Byte Location in Cell				
	Without HEC		With HEC		
	SAM Start	SAM Stop	SAM Start	SAM Stop no-skip	SAM Stop skip
No Pre/Post Pend Data	4	55	4	0	1
1 byte prepended	3	55	3	0	1
1 byte postpended	4	0	4	1	2
2 bytes prepended	2	55	2	0	1
1 byte prepended and 1 byte postpended	3	0	3	1	2
2 bytes postpended	4	1	4	2	3
3 bytes prepended	1	55	1	0	1
2 bytes prepended and 1 byte postpended	2	0	2	1	2
1 byte prepended and 2 bytes prepended	3	1	3	2	3
3 bytes postpended	4	2	4	3	—
4 bytes prepended	0	55	—	—	—
3 bytes prepended and 1 byte postpended	1	0	—	—	—
2 bytes prepended and 2 bytes postpended	2	1	—	—	—
1 byte prepended and 3 bytes postpended	3	2	—	—	—
4 bytes postpended	4	3	—	—	—

3606 tbl 18

NOTE:
1. Byte locations are decimal values.

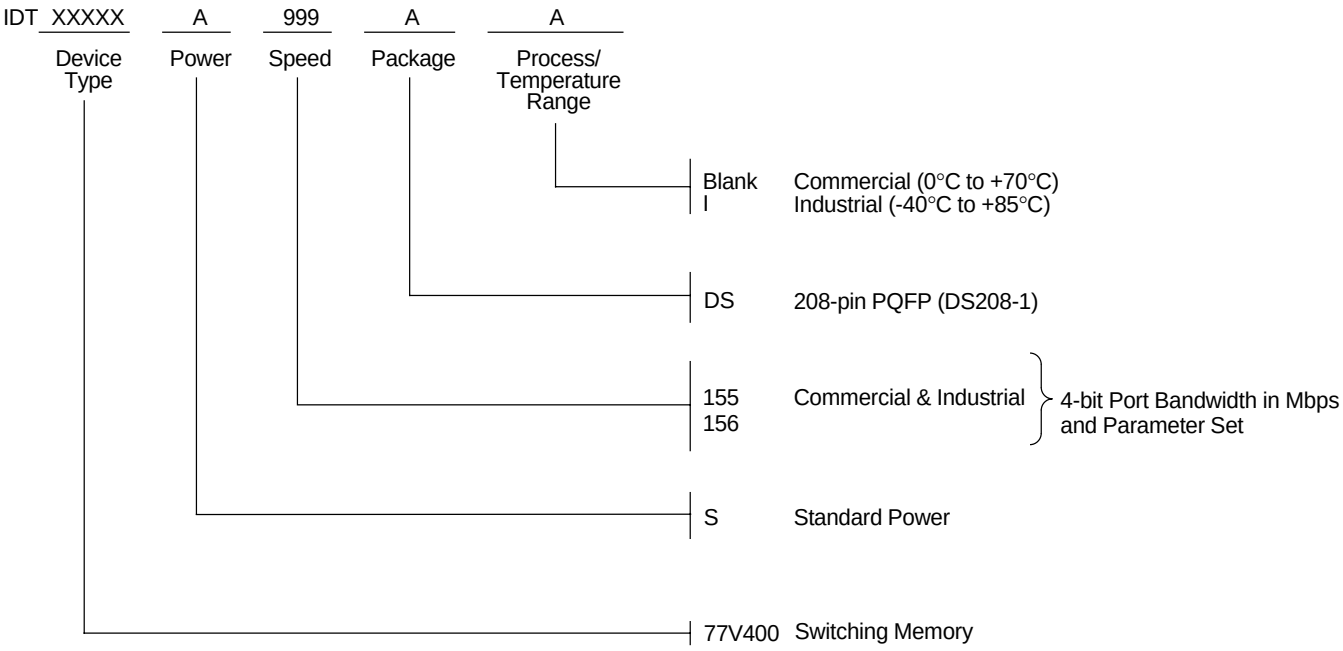
Fusion Memory Refresh Requirements[1,2]

Grade	Maximum Refresh Interval	77V500[3] INIT Command Value (Decimal)	77V500[3] INIT Command Value (Hex)
Commercial	32ms	9	1FF
Industrial	16ms	9	1FF

3606 tbl 19

NOTES:
1. The Fusion Memory of the IDT77V400 must be refreshed by the Control Logic periodically to guarantee data retention. This table defines the maximum refresh interval; that is, the REFRESH command (see "Control Interface Command" Table) must be executed at least 2048 times during each interval.
2. Refresh rate numbers are calculated using a 36MHz SCLK. Refresh is only required for systems which utilize extended cell storage due to queuing requirements above 155Mbps.
3. This information is provided for applications using the IDT77V500 Switch Controller.

Ordering Information



3606 drw 19

Preliminary Datasheet: Definition

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

Datasheet Document History

3/1/99: Updated to new format.
Added Industrial Specifications.
Added S156 Speed Grade.

Pg. 2 Updated Description to clarify CRC error operation.
Pg. 3 Block diagram detail updated for clarity.
Pg. 4 Figure 2, Edit Buffer Block Diagram corrected to include Output CRC path.
Pg. 5 Package Diagram notes added for clarification.
Pg. 6 Pin description table descriptions expanded. IP and OP pin number corrections made.
Pg. 7 Pin description table descriptions expanded. V_{TERM} in Maximum ratings table reduced to 3.9V. V_{IH} Max reduced to V_{CC}+0.3V.
Pg. 8 Reset Current parameter removed.
Pg. 14 Pull down resistor valules specified in Output Ports section.
Pg. 17 Function Sequence Figures modifed to remove first IOD identification (state is really unknown).
Pg. 19 Modified Port Configuration Code Table to clearly identify the subset supported by IDT77V500.
Pg. 20 Improved explanation of Status Register definition and Table and made significant correction and explanation of Error Register definition and Table.
Pg. 22 Recommended Refresh specification added.
Pg. 23 Updated Ordering Information for S156 speed grade and Industrial temperature product.
Pg. 24 Added Preliminary Datasheet definition and Datasheet Document History.

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