Intel® Media Switch IXE2412 10/100 Device

Data Sheet

Product Features/Benefits

- Single-chip, 24-port 10/100 and 2-port Gigabit Ethernet switch/router with Layer 2/3/4 support
  - —High integration, compact footprint and low power dissipation enable the design of high-port density systems at the lowest per-port cost
- Wire-speed performance across all ports in switching or IP/IPX routing modes
  - —Delivers congestion-free performance through Enterprise switches during peak load periods
- Link aggregation of groups up to 8 ports for 10/100 and 2 ports for Gigabit Ethernet
  - —Enables meshed configurations with redundant paths for fail-safe networks
- Advanced traffic prioritization, QoS, and bandwidth management
  - —Enables convergence of voice, video, and data traffic of Ethernet/IP networks
- Supports VLAN based on IEEE 802.1Q standards, ports, and addresses
  - —Enables flat plug-and-play networks that are easy to maintain
- Advanced multicast, broadcast, and filtering capabilities
  - —Enables video and voice multicasting on IP networks, protects from broadcast storms, and allows the building of high-performance intranet firewalls
- IXE2412EE version supports extended temperature range of -40°C to 85°C
  - —Operates at the very high and low temperatures required for telecommunications applications
- Low power dissipation
  - —Allows for low heat dissipation, leading to low cost-per-port in high port density designs

Note: *Key features and benefits for the IXE2412 device are given above. Please refer to Section 11.0 for a complete feature list.*

Contents

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Tables

1.0 General Description

The Intel® Media Switch IXE2412 10/100 Device supports twenty-four 10/100 Mbps ports and two Gigabit ports, integrating the MACs, switching, routing, and queuing logic on-chip. The IXE2412 device is capable of wire-speed Layer 2 switching and wire-speed IP/IPX Layer 2/3/4 switching/routing on all ports. It provides advanced filtering, quality of service, mirroring, and prioritizing capabilities and Layer 4 bandwidth management features.

A system designed using an IXE2412 device requires transceivers on the 10/100 Mbps and Gigabit ports, memory for storing switching data structures, memory for storing packets, and a CPU subsystem. The IXE2412 device interfaces to the CPU subsystem via a 32-bit PCI bus.

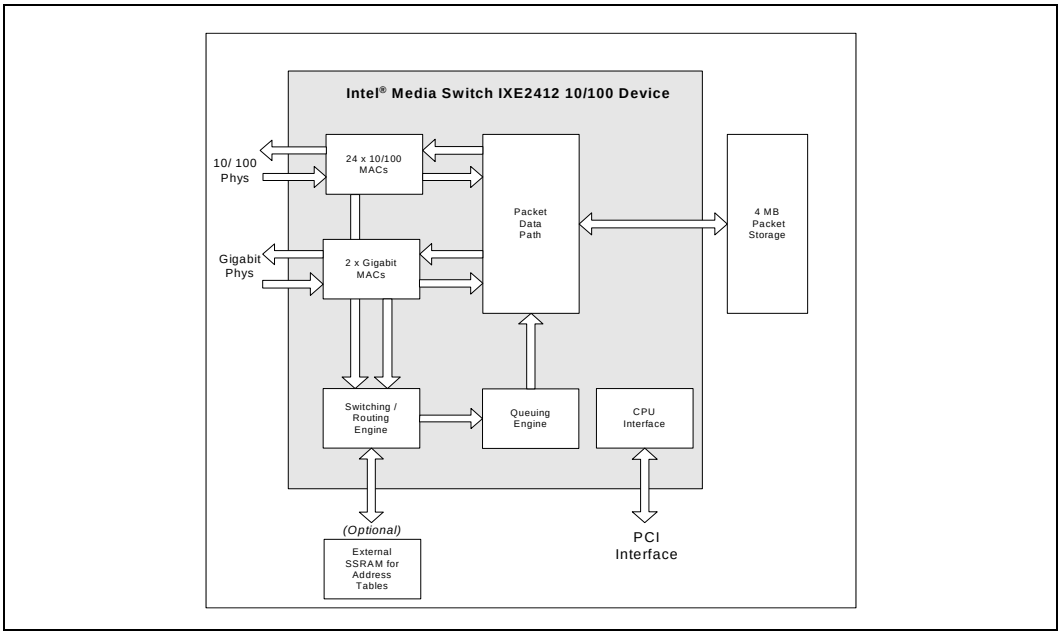
The IXE2412 is available in two parts:

- IXE2412EA: Temperature range of 0°C to 55°C
- IXE2412EE: Temperature range of -40°C to 85°C

2.0 Applications

- 24 + 2 Layer 2 workgroup switch
- Cascadable high port count Layer 2 switch
- Layer 3/4 switch/router with Gigabit uplinks and advanced bandwidth management
- Cascadable high port count Layer 3/4 switch/router
- 3rd generation DSLAMs, cellular switching systems, voice and data integration gateways, edge routers, and packet-based video distribution systems

Figure 1. IXE2412 Block Diagram



3.0 Functional Description

3.1 Introduction

The IXE2412 device is a highly integrated Layer 2 switch and Layer 2/3/4 switch/router. It supports twenty-four 10/100 Mbps ports and 2 Gigabit ports with on-chip MACs. It also supports integrated switching and routing logic and on-chip packet queuing memory. The IXE2412 is capable of switching and routing packets at wire-speed on all ports regardless of packet size.

In Layer 2 mode, the IXE2412 supports:

- IEEE 802.1D, 1998 Edition standard, including 802.1P, 802.1Q

It also supports the IEEE 802.3, 1998 Edition standard, which includes:

- 802.3x flow control
- 802.3u Fast Ethernet
- 802.3z Gigabit Ethernet standards
- 802.3ad Link Aggregation standards

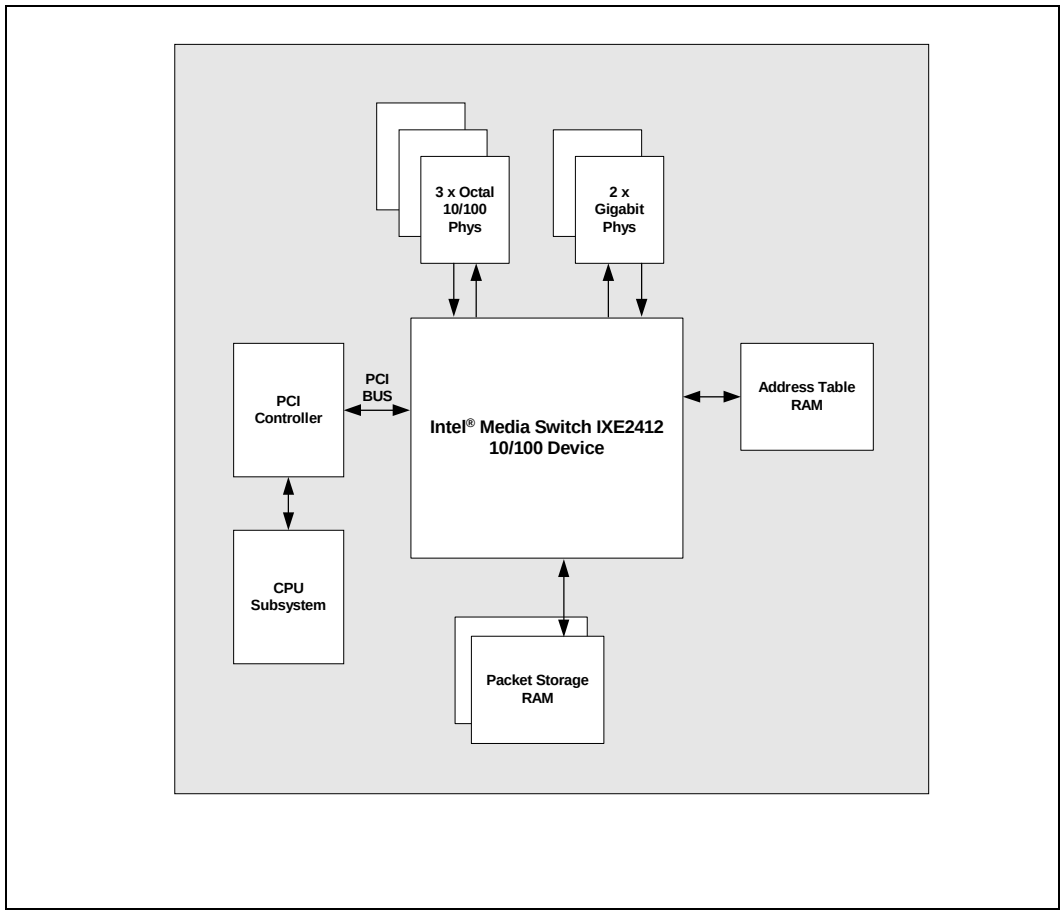
The IXE2412 provides on-chip 32-bit statistics counters to support the Etherstats group of RMON standards. In addition, it provides counters for monitoring flow-based statistics.

In addition to the IEEE standards support, the IXE2412 provides many advanced features such as Filtering, Mirroring, Bandwidth Management, Broadcast, and Multicast Storm Control, all in a single device.

The IXE2412 connects to other devices using standards based interfaces such as SERDES/GMII, SMII, CPU, and SSRAM. This simplifies the system design and provides flexibility when used with other devices.

Figure 2 illustrates a system block diagram of the IXE2412 device.

Figure 2. IXE2412 System Block Diagram



4.0 Interface Descriptions

Table 1 provides a description of the IXE2412 interfaces.

Table 1. IXE2412 Interfaces

Interface	Description
CPU	PCI compliant interface with bus mastering capability for packet and unresolved entry transfers to CPU.
SMII	Two pin interface that allows the IXE2412 to communicate to the external 10/100 Mbps transceivers and provides three separate SYNC signals for point -to-point connections to three 8-port transceivers.
GMII/SERDES	Configurable interface used to link the IXE2412 to the two Gigabit ports.
Address Table SRAM	External 64-bit wide Synchronous SRAM that is used for address storage.
Packet Storage	Two 64-bit wide Pipelined Burst Synchronous Storage SRAM devices that are used for packet storage.
MDIO Phy	Serial MDIO interface for management of up to 32 Phy devices.
LED	Transfers the Gigabit ports' LED status. Can be attached to an external 74HC595-type shift register.

5.0 Data Structures

5.1 Switching Block Entries

The switching engine block of the IXE2412 device uses a group of data structures when making its forwarding decisions. These data structures, called “entries” are linked to each other via pointers and are usually stored in an external Address SRAM (some of them can also be stored on-chip), as shown below in Figure 3.

Each type of “entry” contains different information that allows the IXE2412 to support its diverse set of features. Multiple addresses can point to the same entry type, unless they use different features. This results in compact and efficient memory usage, with memory requirements increasing only as more of these features are enabled.

Figure 3. IXE2412 Data Structures

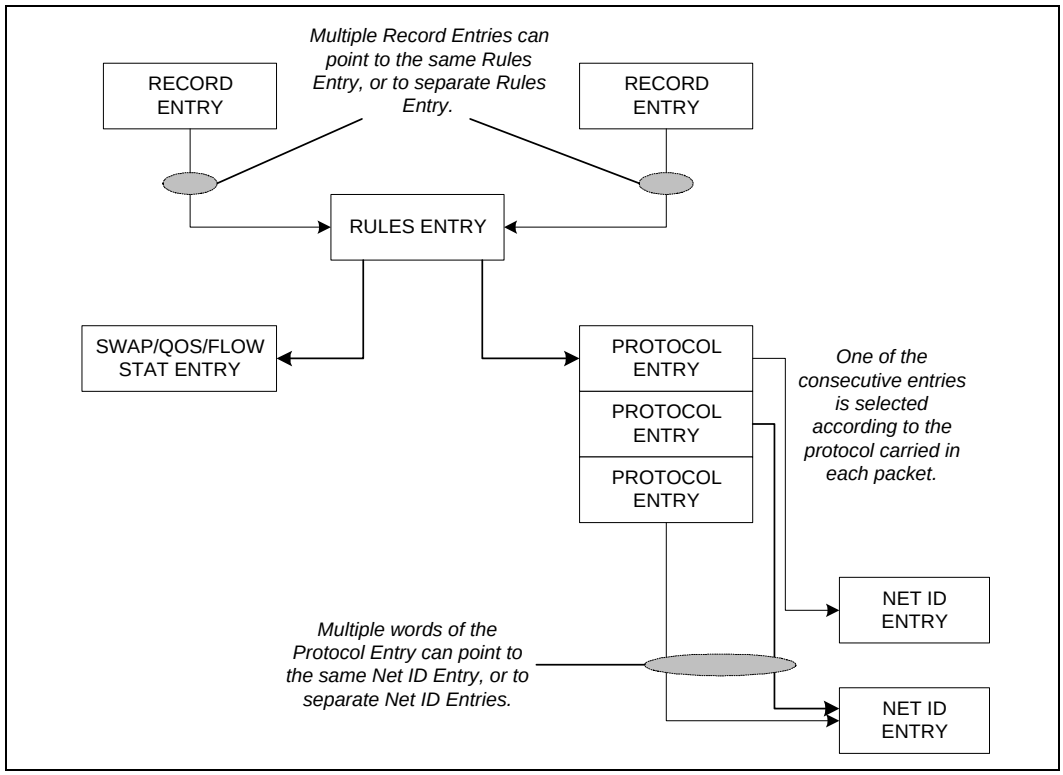


Table 2 entries are maintained by the Switching Engine block for Layer 2, IP, and IPX addresses.

Table 2. Switching Block Entries

Entry Type	Description
Record Entry	The basic entry associated with every address. Contains a pointer directing to another entry called the Rules Entry.
Rules Entry	Contains information about the port on which this address resides, as well as some of the filter, mirror, and priority rules. Contains further pointers to a QoS/Flow Stat Entry and a Protocol Entry.
QoS/Flow Stat Entry	Contains information that allows configuration of QoS flows and configuration of flow based statistics gathering (source address to destination address). For IP and IPX addresses, this QoS/Flow Stat Entry also contains the Destination Swap Address and therefore is called the Dst Swap/ QoS/ Flow Stat Entry.
Protocol Entry	Contains further filter, mirror, and priority configuration information and can be configured as a list of one or more words with different protocols selecting to different words in the same entry. Contains one or more pointers to a Net ID Entry.
Net ID Entry	This entry contains the source address and destination address based mirror port information for Global Source and Global Destination address-based mirroring.

5.2 Enabled Layer 2 Protocols

The Layer 2 protocols enabled are: ARP, RARP, AppleTalk, DECNet, SNA, NetBios, DLC/LLC.

5.3 IP Switching/Routing Features

The IXE2412 will forward the first packet of the flow to the CPU if it does not find a forwarding entry in its tables.

The CPU programs the outgoing port number and the Ethernet address of the next hop or destination address into the IXE2412 tables. The first packet must then be routed on the port that has the destination node connected through it.

Once the entries are created in the IXE2412 tables for the source and destination, all the packets belonging to the flow are routed in hardware at wire speed. Packets belonging to protocols other than IP and IPX will be switched in hardware at wire speeds using the Layer 2 switching algorithm.

5.3.1 Routing Domains

A routing domain is an IP network. An IP address and a subnet mask identify an IP routing domain.

Multiple routing domains can exist on the same port (in which case, they are identified by 802.1Q VLAN tags) or multiple ports can belong to a routing domain. All the ports that belong to a routing domain have the same IP address. Associated with each IP network is a routing domain number.

The IXE2412 device supports up to 32 routing domains. Each routing domain has an Ethernet address associated with it.

5.3.2 Enabled IP Protocols

The IP protocols enabled are: TCP, UDP, ICMP, IGMP, EGP, OSPF, RSVP, and IGRP.

5.4 IPX Switching/Routing Features

5.4.1 Network and Node Addresses

For IPX packet processing, the IXE2412 uses network or node addresses to perform the switching feature.

The IXE2412 maintains a separate address table for IPX network addresses and another address table for IPX node addresses, supporting one routing domain per port for IPX networks.

5.4.2 Enabled IPX Protocols

There are registers provided for each protocol that indicate the increment from the Protocol Offset where the protocol specific information for that protocol may be obtained.

The IPX protocols enabled are: SPX, RIP, NCP, NLSP, and SAP.

5.5 Port-based VLAN Features

The IXE2412 provides Port-based VLAN features by allowing each port to specify the group of ports that belong in that VLAN. The Port based VLANs are the default means of creating VLANs when no other type of VLANs (for example, 802.1Q Tag) have been programmed.

A separate VLAN per port is provided for:

- Layer 2 packets
- IP packets
- IPX packets

5.6 Protocol-based VLAN Features

Protocol-based VLANs can be configured on the IXE2412 by having different protocols point to different words in the Protocol Entry. This allows the protocols to use different Net ID Entries, and thus create different VLANs.

The Protocol Entry used by each protocol is programmed in the Protocol Registers.

5.7 802.1Q VLAN and 802.1D, 1998 Edition Priority and Class of Service Features

The IXE2412 provides extensive support for VLANs and priorities based on the 802.1Q and 802.1D, 1998 Edition specifications.

It provides four levels of queues for all ports. The 3-bit Tag Priority field from the tagged packet can be mapped into the four priority levels, by using the Map Priority Level register. The outgoing packet can be modified to regenerate Tag Priority by using the per port Port Regenerate Priority Entry. Map Priority Level register is a global mapping applying to all ports, while there is a per port Regenerate Priority Entry. The Regenerate Priority Entry is indexed using the receive port number.

Also supported is regenerating the priority the packet should go out on. If there is not a need for regenerating the priority, then the user can program the outgoing priority to be the same as the incoming priority. The outgoing priority is also used to determine which internal queue the packet will be queued to.

5.8 Port Aggregation Features

The IXE2412 supports port aggregation on all ports in groups of up to eight ports for the 10/100 Mbps ports, and in a group of two ports for the Gigabit ports.

The two modes of port aggregation supported are:

- Ingress aggregation only (the default mode),
- Ingress and Egress aggregation.

5.9 Interrupt Generation and Handling

The IXE2412 provides flexible interrupt generation mechanisms. It provides two interrupt pins and two on-chip mask registers that enable the CPU to map any interrupt to either of the interrupt pins. This allows the CPU to treat certain interrupts as high priority and others as low priority.

The CPU can also mask off any interrupt from both registers and effectively convert the bit into a poll bit.

5.10 Packet Transfers to CPU

The IXE2412 provides extensive packet processing support in its hardware in order to reduce the burden of the CPU.

It provides four queues for packets that are to be sent to the CPU. Each queue can be individually turned on or off to start and stop the CPU from receiving packets from that queue, and can be assigned a guaranteed bandwidth. This allows the CPU to prioritize the types of packets that it wants to process.

The DMA engines that are provided per queue allow the IXE2412 to directly transfer data into the CPU memory without CPU intervention.

5.11 Unresolved Packet Transfers to CPU

The IXE2412 also maintains four queues for unresolved packets. Each queue can be individually turned on or off and assigned a guaranteed bandwidth. This allows the CPU to prioritize the types of packets that it wants to process. The DMA engines provided per queue allow the IXE2412 to directly transfer data into the CPU memory without CPU intervention.

The only difference between “unresolved packet transfers to CPU” versus “resolved packet transfers to CPU”, is that unresolved packets have an option to not send the whole packet, but only part of the packet to the CPU. The value by which the read pointer should be incremented, and the value that should be written to the Level Counter register can be determined from the Unres Xfer Size field of the header.

For example, if the Unres Xfer Size field contains 0, then the Read Pointer should be incremented by 32 + 32 = 64 bytes, and the Level Counter register should be written with a value of 64.

5.12 Packet Transfers From CPU

The IXE2412 provides two queues, which are supported by DMA, for packet transfers from the CPU.

Queue 1 is treated as the high priority queue, and is always processed before queue 0, unless a packet transfer had already started for queue 0. In this case, the complete packet from queue 0 is fetched from the CPU memory first, and then the packet from queue 1 is processed. The two queues allow a high priority process (for example, Spanning tree BPDUs) to not have its packets stuck behind other lower-priority packets.

6.0 Hardware Assisted Features

This section describes the hardware assisted features provided in the IXE2412.

6.1 Address Learning

The IXE2412 facilitates address learning by using a hardware engine that provides a content addressable memory-like interface to the CPU.

6.2 Learning of Socket Address

The IXE2412 provides a separate address learning interface for Layer 4 Socket Addresses in order to speed up the process of application based rules generation. The IXE2412 also provides an add, delete, and lookup state machine called the Layer 4 processor. This simplifies the adding and deleting of socket addresses. Finally, the IXE2412 has a separate aging state machine for aging Layer 4 Record Entries.

6.3 Address Aging

The IXE2412 contains hardware assistance for the entry aging process. It has three fundamental modes of operation: automatic, manual, and sparse manual. In all modes, the aging controller steps through a programmable number of zones, broadcasting the current zone (also known as the “age zone”) throughout the device.

6.4 MDIO/MDC Scanning

The IXE2412 provides a controller (called the MMIMOD) to manage up to 32 devices via the MDIO and MDC pins. Up to thirty-two 16-bit registers per device can be addressed. The MMIMOD allows the CPU to use the PCI bus to communicate with these devices, performing all serialization and deserialization. In addition, it allows the CPU to perform “gang” operations that work on several devices at a time. Finally, the MMIMOD can be set to continuously scan the devices looking for a change in their status, interrupting the CPU only when it detects such a change. The MMIMOD uses an internal RAM for all gang operations. There is one location per device, for a total of 32 locations of 16 bits each. Although the RAM is 16 bits wide, each location is accessed at a word (32-bit) boundary, as are all registers within IXE2412.

6.5 Statistic Counters

The IXE2412 provides MAC-based and switch-based statistics gathering support on chip.

6.6 Bandwidth Management

When performing bandwidth management, it is necessary to account for the size of the packets being arbitrated, not just the number of packets. Also, latency can become a problem. The IXE2412 supports two types of algorithms per port: the Credit Algorithm and the Strict Priority Algorithm.

6.7 QoS

The QoS logic in the IXE2412 allows certain flows to be mapped as QoS. These flows can be queued to a certain priority that has been assigned a guaranteed bandwidth. In addition, the rate at which the flow is sending is constantly monitored, and this is compared to the configured rate for this flow. If the rate is exceeded, then the packets that caused this exception are dropped. Thus, multiple flows can be mapped to the same transmit queue, and still be guaranteed the required bandwidth for that flow—the bandwidth management feature takes care of guaranteeing the bandwidth for the queue, and the QoS feature takes care of guaranteeing the bandwidth for all the flows mapped to the same queue.

6.8 Broadcast and Multicast Storm Control

The IXE2412 provides a per port configuration on the incoming port basis that allows broadcast and/or multicast storm control. The CPU can program a threshold value per port that indicates the number of broadcast and/or multicast packets that are allowed in a given time interval.

6.9 IP Multicast Routing

The IXE2412 supports up to 32 routing domains without placing any per port limitations. A port can have one or more routing domains (or IP networks) associated with it. An IP multicast packet that must be forwarded on such a port may need to be sent out multiple times, each time with a different 802.1Q tag associated with that routing domain. The number of times the packet must sent depends on the number of routing domains on that port that have members that belong to that multicast group. The IXE2412 allows up to three multicast group members on a port.

7.0 Electrical and Environmental Specifications

This section summarizes the electrical and environmental specifications for the IXE2412. The IXE2412 supports both 5V and 3.3V signaling environments.

7.1 Absolute Maximum Rating

Applying stresses beyond the absolute maximum may cause unrecoverable damage to the device. Operation of this product is not implied for any condition beyond the ranges specified in the functional operation range described in Section 7.3, "Functional Operating Range" on page 13. Operating this product at the absolute maximum rating for a prolonged period can negatively impact device reliability. The following table, Table 3, "Absolute Maximum Ratings" on page 12 lists the absolute maximum ratings for the IXE2412.

Table 3. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply Voltage Core	VDDCORE	-0.3	2.75	V
Supply Voltage IO	VDDIO	-0.3	3.6	V
Operating Temperature	T_{op}	0	70	^{o}C
Storage Temperature	T_{st}	-65	+150	^{o}C

Caution: **Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.**

7.2 Thermal Resistance

Table 4. Thermal Resistance

Thermal Resistance	Parameter	Value
θ_{JC}	Junction to case	0.4
θ_{CA}	Case to ambient	7.1

Table 5. Thermal Resistance with Airflow

Thermal Resistance	Package	0 LFPM	100 LFPM	200 LFPM	300 LFPM	500 LFPM
θ_{JA} (^{o} C/W)	TBGA Type IA	7.50	6.51	5.92	5.58	5.18
Note: Heat Sink may be required depending on the air flow in the system.						

7.3 Functional Operating Range

The following table, Table 6, "Operating Conditions" on page 13 lists the functional operating range. Please refer to Section 7.1, "Absolute Maximum Rating" on page 12 for details about the absolute maximum ratings.

Table 6. Operating Conditions

Parameter	Sym	Min	Typ[1]	Max	Units
Recommended Supply Voltage VDDCORE	VDDCORE	2.375	2.50	2.625	V[2]
Recommended Supply Voltage VDD	VDD	3.135	3.3	3.456	V[2]
Recommended Operating Temperature (IXE2412EA)	T_{op}	0		55	^{o}C
Recommended Operating Temperature (IXE2412EE)	T_{op}	-40		85	^{o}C
IDDAnalog			8	20	mA
IDDIO			600	800	mA
IDDCORE			1.45	2.0	A
3.3V/2.5V	P_{tot}		6	8	W
Maximum Junction Temperature	T_{jmax}			125	^{o}C

1. Typical values are at 25 ^{o}C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

7.4 Clock Interface

7.4.1 Signal Timing

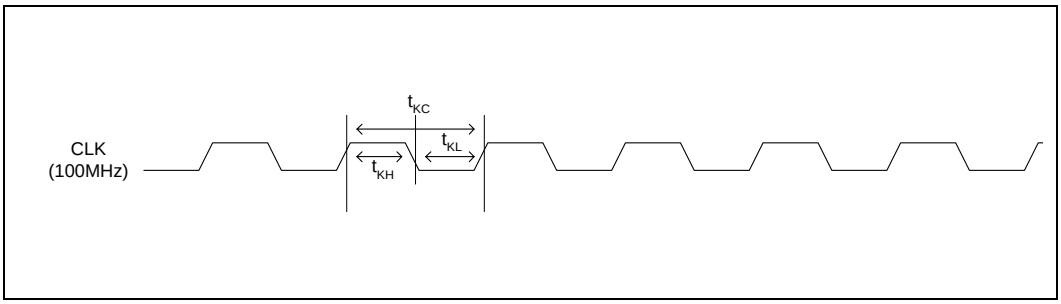
Table 7 describes the clock interface timing specifications.

Table 7. Clock Interface Timing

Symbol	Parameter	Min	Max
f_{FREQ}	Frequency		100MHz
	Duty Cycle	32%	68%
	Cycle-to-Cycle Jitter		400ps
t_{KH}	Time High	3.2ns	
t_{KL}	Time Low	3.2ns	
t_{R}	Rise Time		1.5ns
t_{F}	Fall Time		1.5ns

Figure 4 illustrates the Clock interface timing diagram.

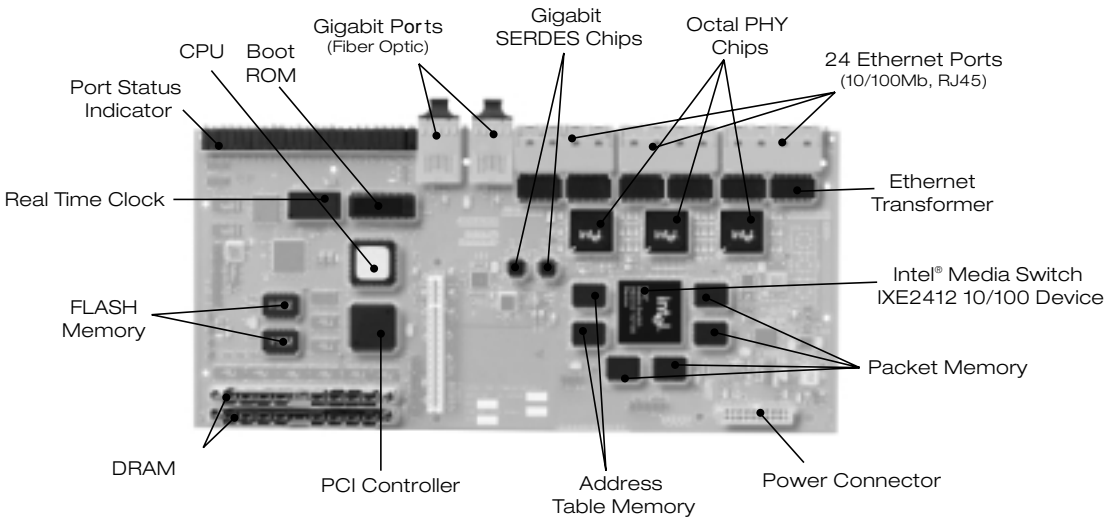
Figure 4. Clock Interface Timing Diagram



8.0 Hardware Support

Figure 5 illustrates the hardware supported in the IXC2412 reference design.

Figure 5. IXC2412 Reference Design



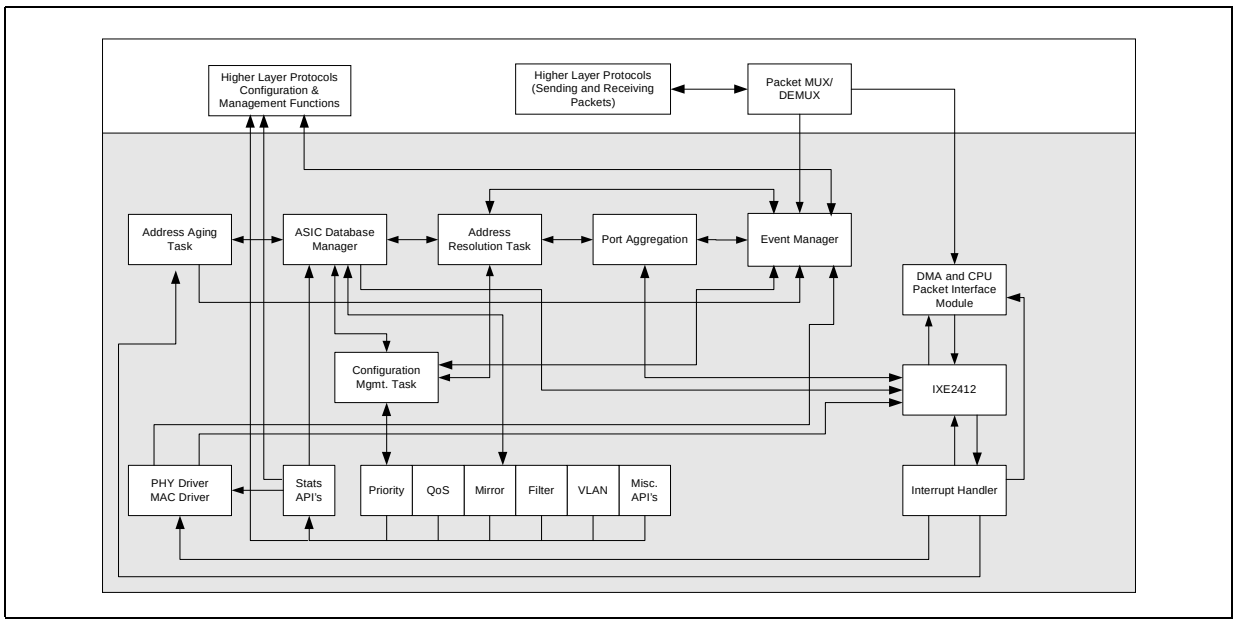
9.0 Software Support

9.1 APIs Supported

The software Application Programming Interfaces (APIs) provided with the IXE2412 allow for integration with OEM software development environments. These APIs enable OEMs to access the IXE2412 features and port their hardware independent software quickly.

The IXE2412 supports the APIs illustrated in the software architecture block diagram shown in Figure 6.

Figure 6. Software Architecture Illustrating APIs Supported by the IXE2412



Summary descriptions and use of APIs supported by the IXE2412 are provided in Table 8.

Table 8. APIs Supported by the IXE2412

API Module	Description/Use
Interrupt Handling	Handles the interrupt from the IXE2412.
OS Wrapper	Provides services needed from the underlying real time operating system. You can port these wrappers to your target operating system.
Notification Manager	Provides a generic method for distributing information within a system. Allows different software modules to register for events of interest and makes the information distribution transparent, modular, and flexible.
ASIC, MAC, and Phy	Enables you to program the performance of different functions. Provides functions for the ASIC, MAC, and Phy initialization, configuration, and management which include functions for ASIC initialization and routines for bit level manipulations of the IXE2412 registers for various configurations. MAC and Phy provide functions to initialize the Ethernet controllers built into the IXE2412 and the LXT9782 Phy (such as functions to change the speed, functions to change the duplex mode, etc.).
Address Resolution	Contains functions used for learning IP, IPX, and Layer 2 addresses.
IP and IPX Configuration and Management	Include the ability to perform a routing table lookup (for IP and IPX Address Resolution—call into IP and IPX routing modules), determine the Ethernet address of the destination station or the next-hop (for routed packets whose destination is unresolved to determine the address programmed into swap entry—call into ARP module for IP or SAP module for IPX), etc.
DMA Interface	Provides functions to send and receive packets between the IXE2412 and the CPU. The ASIC Driver provides a full set of functions supporting packet send and packet receive, and a separate set of functions that allow higher level software to manage the receive and send DMA buffer pools directly.
Address Aging	Provides functions for configuring an ageing interval. The IXE2412 tracks the address record entries that have been accessed over the ageing interval. Different aging time intervals can be specified for Layer 2, Layer 3, and Layer 4 entries.
Address Learning	Provides functions for address learning in the software. The hardware provides a CAM interface to facilitate fast learning of addresses.
Filters, Mirrors, Priorities, and Quality of Service	Supports configuring filters, mirrors, priorities, and quality of service for networks, nodes and ports. These APIs can be called from higher-layer software modules (such as SNMP agent) to configure these special rules for addresses.
VLAN	Provides APIs (based on ports, 802.1Q tags, and multicast addresses) to make VLAN configuration and management easier for higher-layer software modules such as GVRP, GMRP, or SNMP agent (for user-configured VLANs).
Statistics Gathering	Provides counters that count different events required for both standard and draft MIB implementations and functions for gathering MAC, Phy, and ASIC statistics, including RMON stats. The APIs provided for higher-layer software modules are for reading these counters.
Link Aggregation Configuration and Management	Support for port aggregation on all ports in groups of up to eight ports for the 10/100 Mbps ports, and in a group of two ports for the Gigabit ports. Supports Ingress Aggregation Only and Ingress and Egress Aggregation modes of which Ingress Aggregation Only mode is the default.
Miscellaneous	Provides functions for all other miscellaneous configurations, such as adding static entries to address tables, creating static routes, creating default routes, broadcast and multicast storm control, etc. The Miscellaneous API module interfaces to various modules including ASIC Database Manager, Configuration Management task, Address Resolution task, etc., to provide these functionalities to higher-layer protocol stacks.

9.2 Protocols

The IXE2412 can perform extensive packet parsing and can obtain packet type (Type II, SNAP, etc.) and protocol (IP, IPX, GxRP, STP, etc.) information directly from the packet header.

Enabled protocols are summarized in Table 9.

Table 9. Protocols Enabled by the IXE2412

Protocol	Description/Use
GxRP	GxRP family protocols enabled include GARP, GARP Multicast Registration Protocol (GMRP), and GARP VLAN Registration Protocol (GVRP), which comprise a task within a MAC bridge system that interacts with other tasks and the driver through messages and events. GARP services are the basis for implementing GMRP and GVRP. GMRP provides the ability to register (and de-register) Group Address membership in a MAC bridge. GVRP provides the functionality to register (and de-register) VLANs dynamically.
IP	Enabled IP protocol modules are the: • Internet Protocol (IP) • Address Resolution Protocol (ARP) • Internet Control Message Protocol (ICMP) • Internet Group Management Protocol (IGMP) • Routing Information Protocol (RIPv1 and RIPv2) • Internet Control Message Protocol (ICMP) • User Datagram Protocol (UDP) • Trace Route utility IP modules can be organized as independent tasks or be grouped together into a single task depending upon the target environment and user requirement.
Spanning Tree	Spanning Tree Algorithm and Protocol (STAP) functionality, which computes single spanning tree of all nodes in the arbitrary bridged network.
Stacking Control	Enables multiple Ethernet switches to be interconnected and managed as if they were a single larger switching device. All features supported as it would for a stand-alone system.

10.0 Feature List

- Twenty-four 10/100 Mbps ports and 2 Gigabit port switching/routing in a single 600 pin TBGA chip
- Integrated Gigabit and 10/100 Ethernet MACs
- On-chip storage for port transmit queues
- 10/100 Mbps ports configurable to half or full duplex
- Wire speed switching and routing on every port
- Hardware assisted address learning and aging
- Link aggregation of all ports in groups up to 8 for 10/100 Mbps ports and 2 for Gigabit ports
- Broadcast and multicast storm control with configurable per port settings

10.1 Interfaces

- SERDES and GMII interface for Gigabit ports and SMII interface for 10/100 Mbps ports
- PCI compliant CPU interface with bus mastering capability for packet and unresolved entry transfers to CPU
- SSRAM interface for address table sizes up to 40,000 entries (16,000 each for Layer 2, IP, and 8,000 IPX entries) with no per port limits. Address table sizes can be as large as 40,000 entries. in Layer 2 mode only

10.2 Layer 3/Layer 4

- Packet by packet IP and IPX routing in hardware
- Layer 4 application level intelligence for IP switching and routing
- Layer 2 switching for protocols other than IP and IPX
- Automatic recognition of Ethernet Type II and 802.3 packets
- 32 IP networks per device with no per port limit. The same IP network can span multiple ports.
- Maximum of three IP multicast groups supported per port

10.3 IEEE Standards

Supported:

- 802.1D, 1998 edition which includes 802.1p Priority and Class of Service standard
- 802.1Q VLAN standard
- 802.3, 1998 edition which includes 802.3u Fast Ethernet standard, 802.3z Gigabit standard, and 802.3x Flow control standard
- Proposed 802.1ad standard

10.4 VLAN Configuration

Based on:

- 802.1Q tags
- Ports
- Multicast Ethernet address
- Protocols

10.5 Filtering

Based on:

- Ports
- Source Ethernet, IP, or IPX address
- Destination Ethernet, IP, or IPX address
- Source-destination Ethernet, IP, or IPX address pairs
- End to end IP applications
- Protocols

10.6 Class of Service

Based on:

- 802.1p tags
- Ports
- Source Ethernet, IP, or IPX address
- Destination Ethernet, IP, or IPX address
- Source-destination Ethernet, IP, or IPX address pairs
- End to end IP applications
- Protocols

10.7 Port Mirroring

Based on:

- Ports
- Source Ethernet, IP, or IPX address
- Destination Ethernet, IP, or IPX address
- Source-destination Ethernet, IP, or IPX address pairs

- End to end IP applications
- Protocols

10.8 Bandwidth Management

Based on:

- Source Ethernet, IP, or IPX address
- Destination Ethernet, IP, or IPX address
- Source-destination Ethernet, IP, or IPX address pairs
- End to end IP applications

10.9 Queues

- Four queues for CPU packets; to allow prioritizing of packet types
- Four queues for unresolved packets to CPU; to allow prioritizing of unresolved types
- Four queues per port with user configurable priorities and weighted fair queuing

10.10 Counters

Based on:

- EtherStats group of RMON
- RFC 1573 and Ethernet interfaces MIB (RFC 1643)

10.11 Protocols

- Hardware enabling for BPDU, GVRP, GMRP, IGMP packets
- Hardware enabling for routing protocols such as RIP, IPX/RIP, IPX/SAP, OSPF, DVMR