PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8432-101

700MHz, Low Phase Noise, LVPECL Frequency Synthesizer

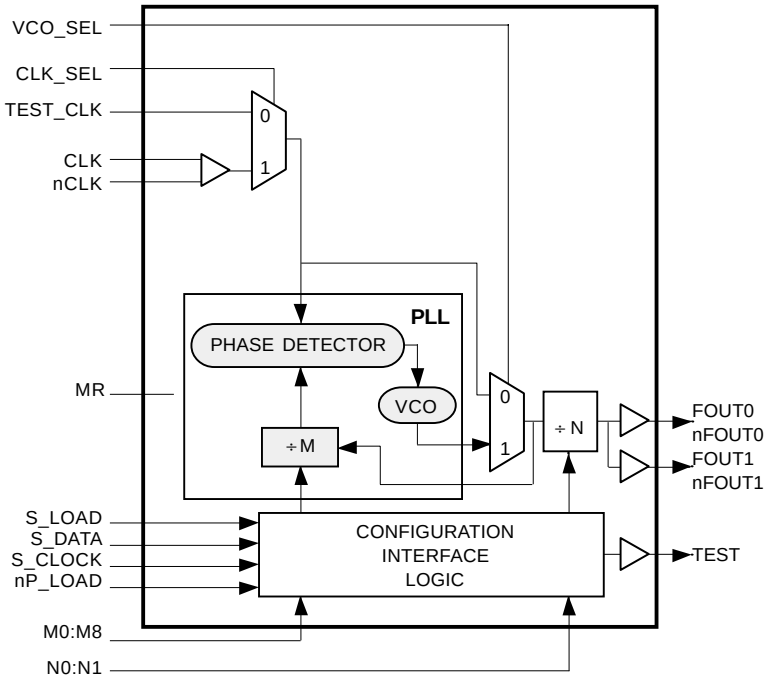
General Description

The ICS8432-101 is a general purpose, dual output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input differential or single ended reference frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics of the ICS8432-101 makes it an ideal clock source for Gigabit Ethernet, Fiber Channel 1 and 2, Infiniband and Sonet OC3 and OC12 applications.

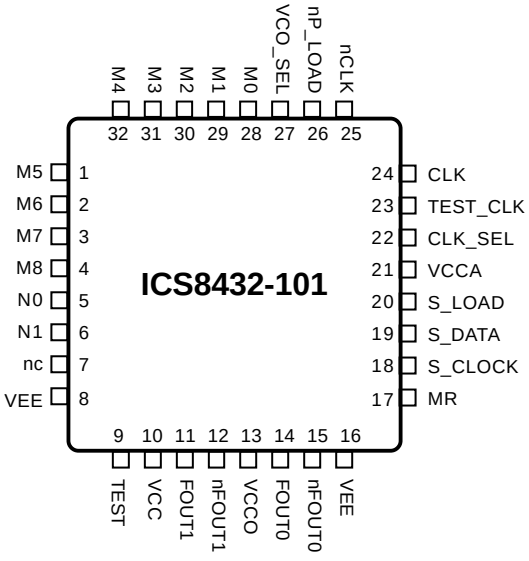
Features

- FOUT0 and FOUT1 differential 3.3V LVPECL outputs
- Selectable CLK, nCLK and LVCMOS reference inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVHSTL, LVDS, SSTL
- Maximum output frequency: 31.25MHz to 700MHz
- Differential input or reference input frequency: 14MHz to 25MHz
- VCO range: 250MHz - 700MHz
- Accepts any single-ended input signal to LVCMOS with resistor bias on nCLK input
- Parallel interface for programming counter and output dividers
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm Package Body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

Functional Description

NOTE: The functional description that follows describes operation using a 25MHz clock input. Valid PLL loop divider values for different input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8432-101 features a fully integrated PLL and therefore requires no external component for setting the loop bandwidth. A differential clock input is used as the input to the ICS8432-101. This input is fed into the phase detector. A 25MHz clock input provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8432-101 support two input modes and programmable PLL loop divider and output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the ripple counter. On the LOW-to-HIGH transition of the nP_LOAD input the data is latched and the ripple counter remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result the M and N bits can be hardwired to set the ripple counter to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the input frequency and the loop divider is defined as follows:

$$fVCO = fIN \times M$$

The M count and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function. Valid M values for which the PLL will achieve lock are defined as $10 \leq M \leq 28$. The frequency out is defined as follows:

$$fOUT = \frac{fVCO}{N} = fIN \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the ripple counter when S_LOAD transitions from LOW-to-HIGH. The ripple counter divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH data at the S_DATA input is passed directly to the ripple counter on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data
1	0	Output of M divider
1	1	CMOS Fout

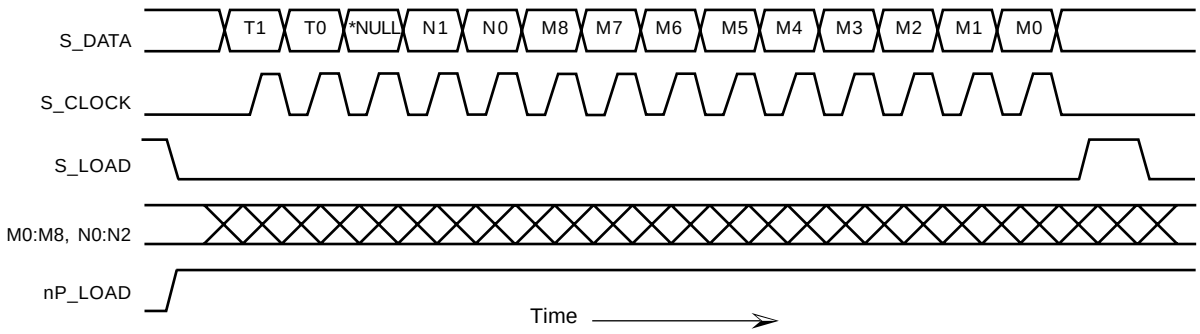


Figure 1. Parallel & Serial Load Operations

*NOTE: The NULL timing slot must be observed.

Table 1. Pin Descriptions

Number	Name	Type		Description
1	M5	Input	Pullup	M counter/divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4 28, 29 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C Function table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	V_{EE}	Power		Negative supply pin. Connect to ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS interface levels.
10	V_{CC}	Power		Positive supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin. Connect to 3.3V.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Forces outputs LOW, but does not effect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLK.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLK.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the ripple counter. LVCMOS / LVTTL interface levels.
21	V_{CCA}	Power		Analog supply pin. Connect to 3.3V.
22	CLK_SEL	Input	Pullup	Clock select input. Selects between differential clock input or test input as the PLL reference source. When HIGH, selects CLK, nCLK inputs. When LOW, selects TEST_CLK input. LVCMOS / LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTL interface levels.
24	CLK	Input	Pulldown	Non-inverting differential clock input.
25	nCLK	Input	Pullup	Inverting differential clock input.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into ripple counter, and when data present at N1:N0 sets the output divide value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characterisitics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	TEST_CLK, CLK, nCLK				4	pF
		M0:M8, S_LOAD, N0:N1, S_DATA, VCO_SEL, MR CLK_SEL, nP_LOAD, S_CLOCK				4	pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

Table 3A. Parallel and Serial Modes Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. M and N counters reset.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to ripple counter and output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the ripple counter and output divider.
L	H	X	X	↓	L	Data	Ripple counter and output divide values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
300	12	0	0	0	0	0	1	1	0	0
325	13	0	0	0	0	0	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M count values and the resulting frequency correspond to differential input or test clock input frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

Absolute Maximum Ratings

Supply Voltage, V_{CCx}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	46°C/W
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}, V_{CCA}, V_{CCO}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				110	mA
I_{CCA}	Analog Power Supply Current					mA

Table 4B. Differential DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{IN} = 3.465V			150	µA
		nCLK	V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{IN} = 0V	-5			µA
		nCLK	V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage						V
V_{CMR}	Common Mode Input Voltage						V

NOTE 1: For single ended applications the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as the V_{IH}.

Table 4C. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	VCO_SEL, CLK_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, N0:N1, M0:M8, MR	V_{CCI} = 3.465V	2		3.765	V
		TEST_CLK	V_{CCI} = 3.465V	1.7		3.765	V
V_{IL}	Input Low Voltage	VCO_SEL, CLK_SEL, S_LOAD, S_DATA, S_CLOCK, nP_LOAD, N0:N1, M0:M8, MR	V_{CCI} = 3.135V	-0.3		0.8	V
		TEST_CLK	V_{CCI} = 3.135V			1.3	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD, MR	*V_{CCx} = V_{IN} = 3.465V			150	µA
		M5, CLK_SEL, VCO_SEL	*V_{CCx} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD, MR	*V_{CCx} = 3.465V, V_{IN} = 0V	-5			µA
		M5, CLK_SEL, VCO_SEL	*V_{CCx} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST	*V_{CCx} = 3.135V, I_{OH} = -36mA	2.6			V
V_{OL}	Output Low Voltage	TEST	*V_{CCx} = 3.135V, I_{OL} = 36mA			0.5	V

*NOTE 1: V_{CCx} denotes V_{CC}, V_{CCA}, and V_{CCO}.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1	FOUT0, nFOUT0 FOUT1, nFOUT1	*V_{CCx} = 3.3V	V_{CC} - 2.1			V
V_{OL}	Output Low Voltage; NOTE 1	FOUT0, nFOUT0 FOUT1, nFOUT1	*V_{CCx} = 3.3V			V_{CC} -	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	FOUT0, nFOUT0 FOUT1, nFOUT1	3.135V ≤ *V_{CCx} ≤ 3.465V	0.6		0.85	V

NOTE 1: FOUT0, nFOUT0, FOUT1, nFOUT1 outputs terminated with 50 Ω to V_{CCO} - 2V.
The power dissipation of a terminated output pair is 32mW.
*NOTE 2: V_{CCx} denotes V_{CC}, V_{CCA}, and V_{CCO}.

Table 5. Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Maximum Input Frequency	TEST_CLK; NOTE 1		14		25	MHz
		CLK, nCLK; NOTE 1		14		25	MHz
		S_CLOCK				TBD	MHz
t_R	Input Rise Time	TEST_CLK	Measured at 20% to 80% points			TBD	ns
		CLK, nCLK				TBD	ns
t_F	Input Fall Time	TEST_CLK	Measured at 20% to 80% point			TBD	ns
		CLK, nCLK				TBD	ns
t_{DC}	Input Reference Duty Cycle	TEST_CLK		TBD		TBD	%
		CLK, nCLK		TBD		TBD	%

NOTE 1: For the differential input and reference frequency range the M value must be set for the V_{CO} to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 14MHz valid values of M are $18 \leq M \leq 50$. Using the maximum frequency of 25MHz valid values of M are $10 \leq M \leq 28$.

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
FOUT	Maximum Output Frequency			31.25		700	MHz
*t*jit(acc)	Accumulative Period Jitter, RMS; NOTE 1						ps
*t*jit(per)	Period Jitter, RMS; NOTE 1						ps
*t*sk(o)	Output Skew; NOTE 2					10	ps
odc	Output Duty Cycle			47		53	%
t_R	Output Rise Time	FOUT0, nFOUT0 FOUT1, nFOUT1	20% to 80%	300		800	ps
t_F	Output Fall Time	FOUT0, nFOUT0 FOUT1, nFOUT1	20% to 80%	300		800	ps
t_S	Setup Time	M, N to nP_LOAD		TBD			ns
		S_DATA to S_CLOCK		TBD			ns
		S_CLOCK to S_LOAD		TBD			ns
t_H	Hold Time	M, N to nP_LOAD		TBD			ns
		S_DATA to S_CLOCK		TBD			ns
		S_CLOCK to S_LOAD		TBD			ns
t_{LOCK}	PLL Lock Time					TBD	ms
t_{PW}	Pulse Width	nP_LOAD				TBD	ns
		S_LOAD				TBD	ns

NOTE 1: Jitter performance using TEST_CLK input.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross point.

Package Outline - Y Suffix

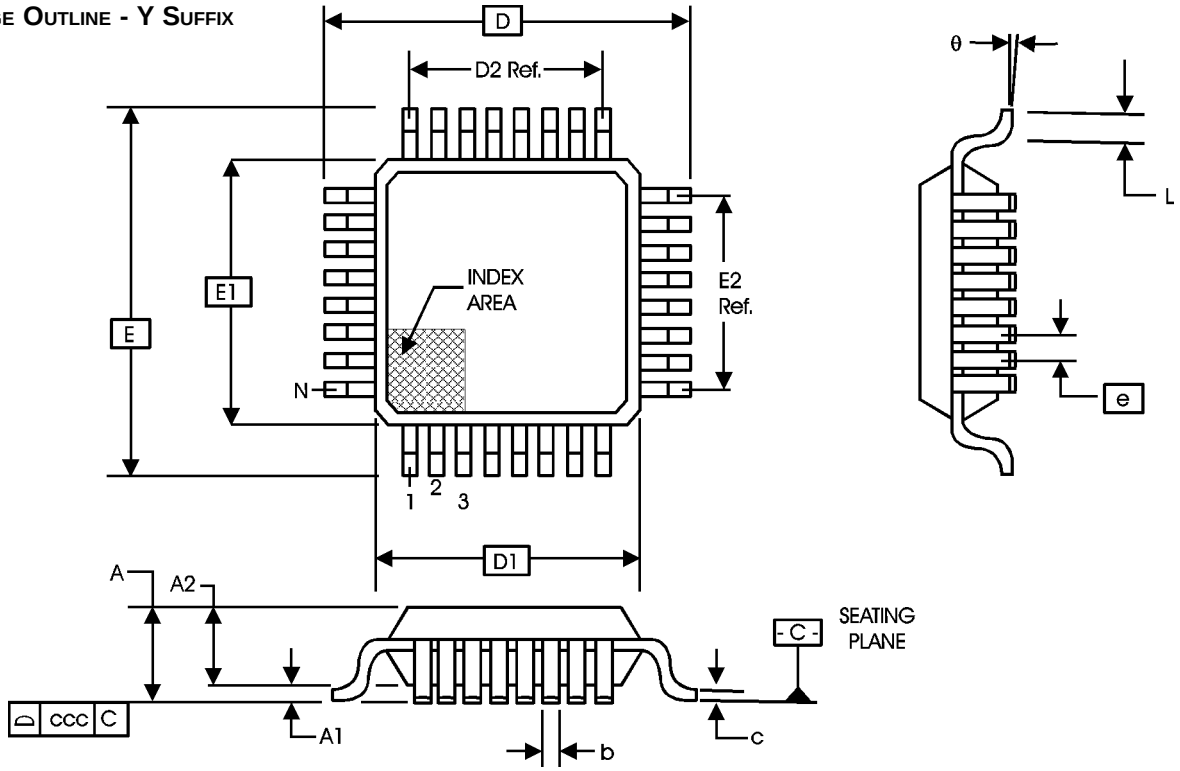


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Table 8. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8432AY-101	ICS8432AY-101	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8432AY-101T	ICS8432AY-101	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C