Integrated
Circuit
Systems, Inc.

ICS8344-01

LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

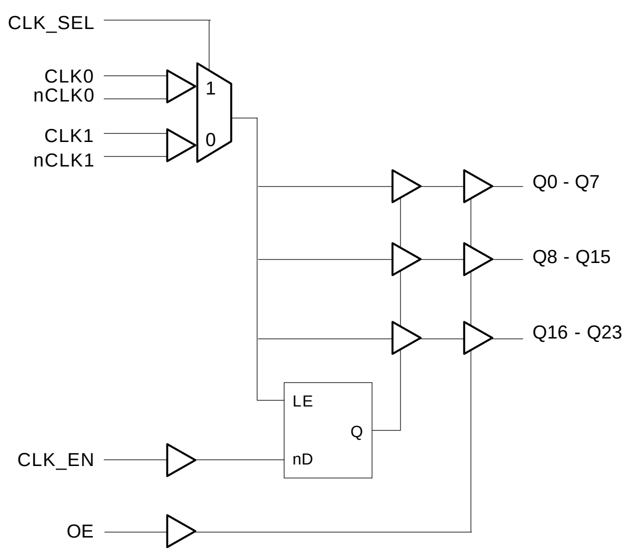
The ICS8344-01 is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8344-01 has two selectable clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. The ICS8344-01 is designed to translate any differential signal levels to LVCMOS levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The outputs are driven low when disabled. The ICS8344-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

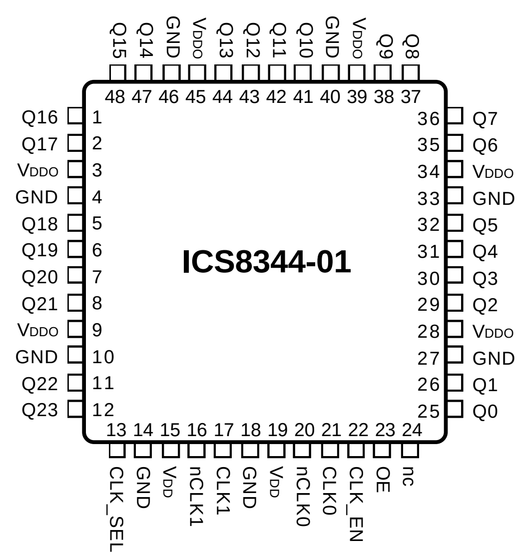
FEATURES

- 24 LVCMOS outputs, 7Ω typical output impedance
- 2 selectable CLKx, nCLKx inputs
- CLK0, nCLK0 and CLK1, nCLK1 pairs can accept the following input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Output frequency up to 250MHz
- Translates any single ended input signal to LVCMOS with resistor bias on nCLK input
- Synchronous clock enable
- Output skew: 200 ps (maximum)
- Part-to-part skew: 900ps (maximum)
- Bank skew: 85ps (maximum)
- Propagation delay: 5ns (maximum)
- 3.3V, 2.5V or mixed 3.3V, 2.5V operating supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q16 thru Q23 outputs. 7Ω typical output impedance.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins. Connect 3.3V or 2.5V.
4, 10, 14,18, 27, 33, 40, 46	GND	Power		Power supply ground. Connect to ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK inputs, When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levelss.
15, 19	V_{DD}	Power		Positive supply pins. Connect 3.3V or 2.5V.
16	nCLK1	Input	Pullup	Inverting differential LVPECL clock input.
17	CLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
20	nCLK0	Input	Pullup	Inverting differential LVPECL clock input.
21	CLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
22	CLK_EN	Input	Pullup	Synchronizing control for enabling and disabling clock outputs. LVCMOS interface levels.
23	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q23.
24	nc	Unused		No connect.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Q0 thru Q7 outputs. 7Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Q8 thru Q15 outputs. 7Ω typical output impedance.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK0, nCLK0, CLK1, nCLK1				4	pF
		CLK-SEL, CLK_EN, OE				4	pF
C_{PD}	Power Dissipation Capacitance (per output)						pF
							pF
							pF
R_{PULLUP}	Input Pullup Resistor				51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		KΩ
R_{OUT}	Output Impedance				7		Ω

TABLE 3A. OUPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	**Output**	**Input**	**Output**	**Input**	**Output**
OE	**Q0-Q7**	**OE**	**Q8-Q15**	**OE**	**Q16-Q23**
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Enabled	1	Enabled	1	Enabled

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	**CLK0, nCLK0**	**CLK1, nCLK1**
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUT FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE	**CLK0, CLK1**	**nCLK0, nCLK1**	**Q0 thru Q23**		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 11, Figure 8, which discusses wiring the differential input to accept single ended levels.

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Quiescent Power Supply Current				95	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, CLK_EN, OE		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO}$ = 3.135V I_{OH} = -36mA	2.7			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO}$ = 3.135V I_{OL} = 36mA			0.5	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-toPeak Input Voltage			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage: NOTE 1, 2			0.9		2	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

TABLE 4E. LVCMOS DC CHARACTERISTICS, VDDI = V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, CLK_EN, OE		2		3.8	V
V_{IL}	Input Low Voltage	CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OH} = -27mA	1.9			V
V_{OL}	Output Low Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OL} = 27mA			0.4	V

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.9		2	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD+} 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Quiescent Power Supply Current				95	mA

TABLE 4H. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, CLK_EN, OE		2		2.9	V
V_{IL}	Input Low Voltage	CLK_SEL, CLK_EN, OE		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, OE	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	CLK_EN, OE	$V_{DD} = 2.625$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625$, $V_{IN} =0V$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO} = 2.375V$ $I_{OH} = -27mA$	1.9			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO} = 2.375V$ $I_{OL} = 27mA$			0.4	V

TABLE 4I. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V±5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK0, CLK1	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
		CLK0, CLK1	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.9		2	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%; V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%;
$V_{DD} = V_{DDO}$ = 2.5V ± 5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency					250	MHz
t_{PD}	Propagation Delay, NOTE 1		0MHz ≤ f ≤ 200MHz	2.5		5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Q0 - Q7	Measured on the rising edge of $V_{DDO}/2$			85	ps
		Q8 - Q15				180	ps
		Q16 - Q23				100	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the rising edge of $V_{DDO}/2$			200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6		Measured on the rising edge of $V_{DDO}/2$			900	ps
t_R	Output Rise Time; NOTE 5		30% to 70%	200		800	ps
t_F	Output Fall Time; NOTE 5		30% to 70%	200		800	ps
odc	Output Duty Cycle		0MHz ≤ f ≤ 200MHz	tCYCLE/2 - 0.25	tCYCLE/2	tCYCLE/2 + 0.25	%
			f = 200MHz	2.25	2.5	2.75	ns
t_{EN}	Output Enable Time; NOTE 5		f = 10MHz			5	ns
t_{DIS}	Output Disable TIme; NOTE 5		f = 10MHz			4	ns

All parameters measured at 200MHz and VPPtyp unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output crossing point.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as between outputs at the same supply voltages ane with equal load conditions. Measured at the output differential cross points.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

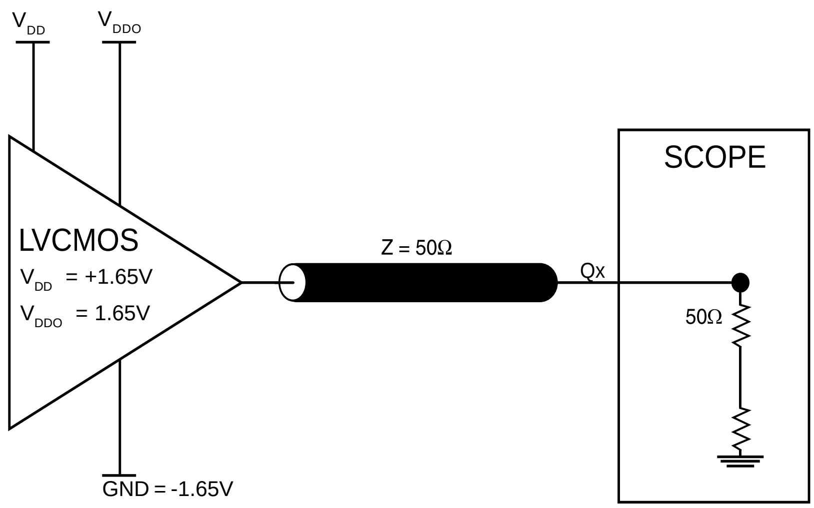


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

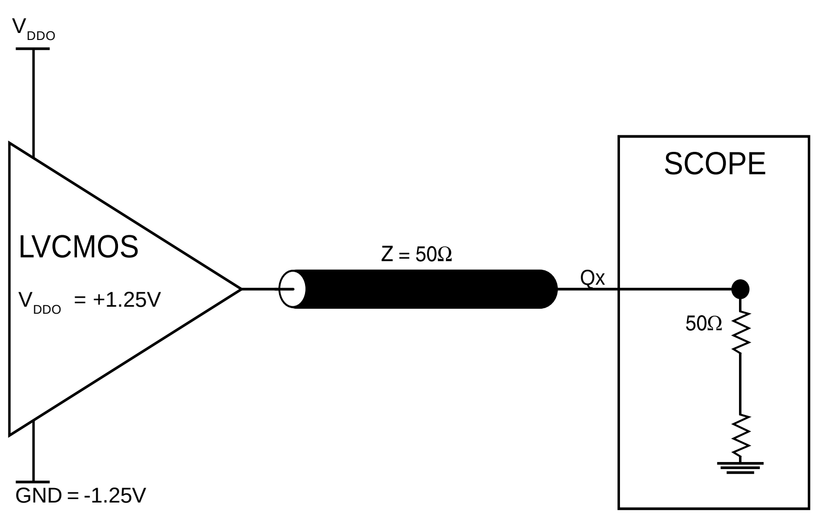


FIGURE 1B - 2.5V OUTPUT LOAD TEST CIRCUIT

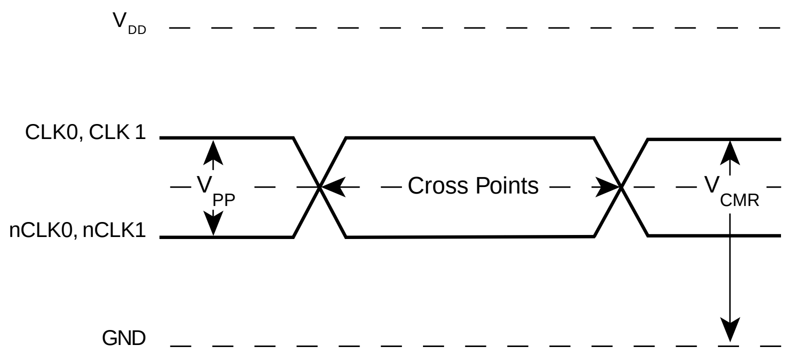


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

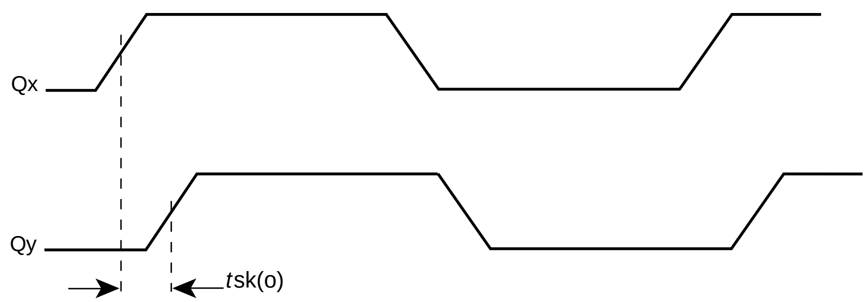


FIGURE 3 - OUTPUT SKEW

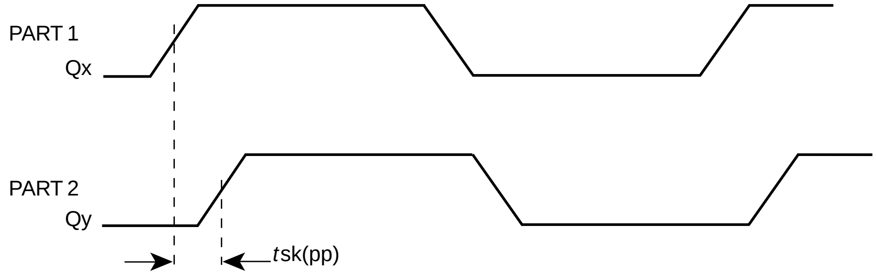


FIGURE 4 - PART-TO-PART SKEW

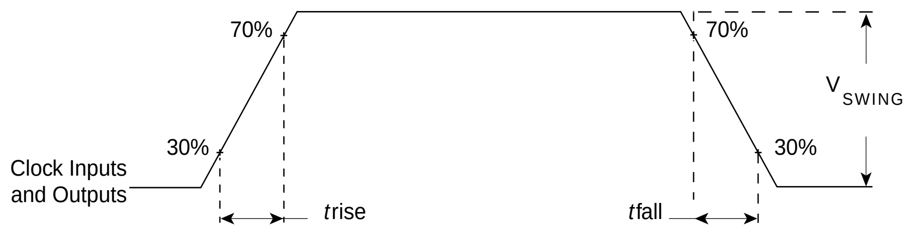


FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

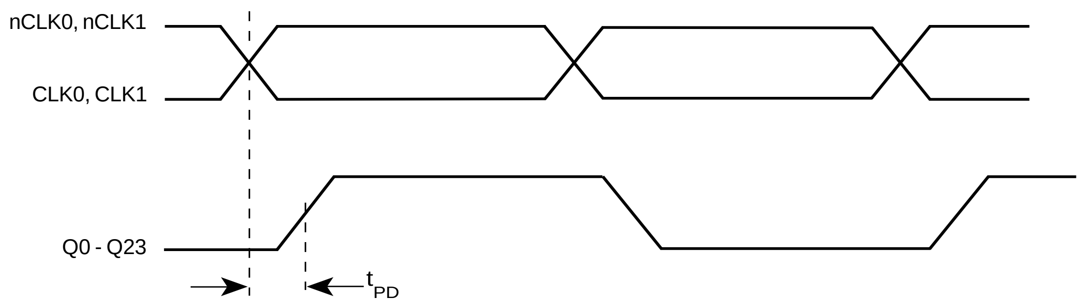
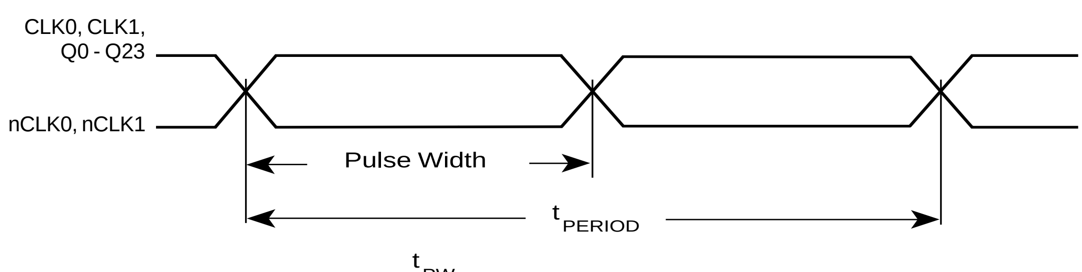


FIGURE 6 - PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

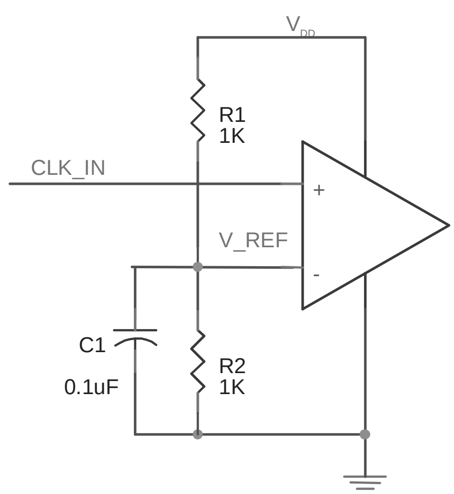


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8344-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8344-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 95mA = **329.2mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 24* 32mW = **768mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 329.2mW + 768mW = **1097.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used . Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.
Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.1097W * 42.1°C/W = 74.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48-pin LQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVCMOS output driver circuit and termination are shown in *Figure 9.*

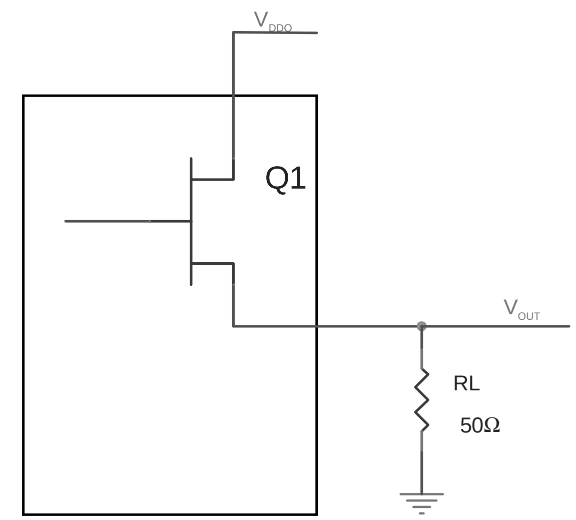


FIGURE 9 - LVCMOS DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DD\_MAX} - 1.2V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DD\_MAX} - 0.4V}$

Pd_H = (1.2V/50Ω) * (2V - 1.2V) = **19.2mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8344-01 is: 1503

PACKAGE OUTLINE - Y SUFFIX

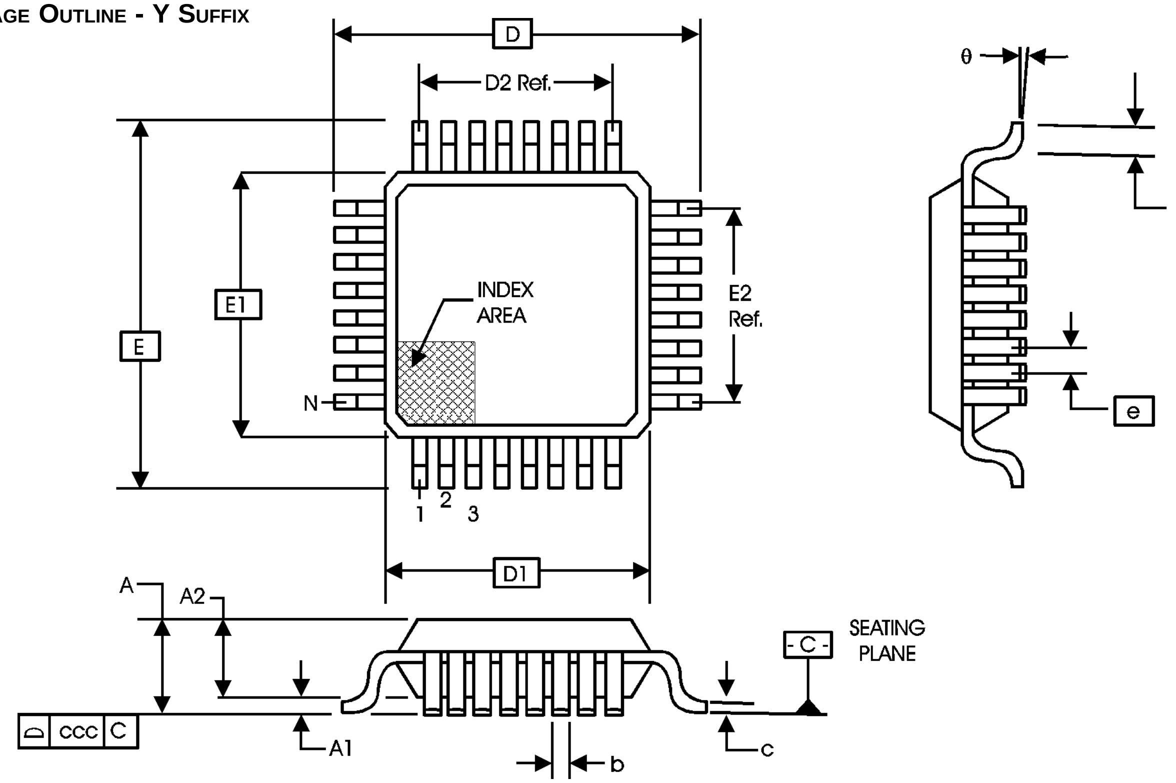


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8344AY-01	ICS8344AY-01	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8344AY-01T	ICS8344AY-01	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C