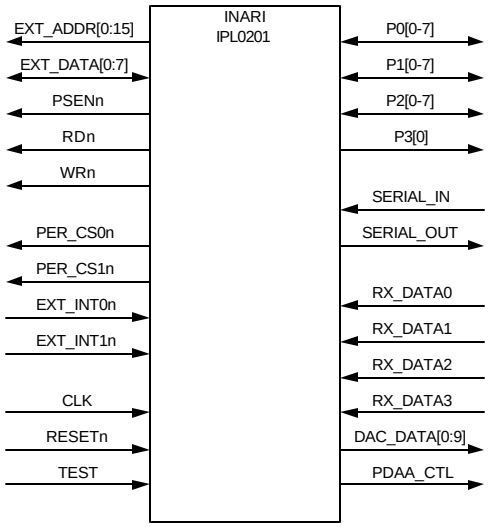
IPL0201 2 Mbps Powerline Network Controller

2 Mbps Integrated Powerline Networking MAC/PHY

FEATURES



- *Inari's Digital Powerline (DPL™) Transceiver*
  - Customized for powerline environment
  - Includes 4 channel transceiver
  - Variable data rates up to 2 Mbps
- *Microcontroller*
  - 8051 instruction set compatible
  - Industry standard development tools
  - 8-10 MIPS
  - 4 clock/instruction cycle
  - Three 8-bit I/O ports
  - Two 8-bit timer/counters
  - 256 bytes scratchpad RAM
  - 2 KB buffer RAM
  - Addresses 64 KB external ROM and 64 KB external RAM
- *Generic Host Application Interface*
  - Two programmable chip selects
  - Two external interrupt inputs
  - Non-multiplexed address/data bus
  - Can be used as a "bridge" to other protocols using external peripherals
  - Parallel Port (IEEE 1284) software handshake component
  - USB firmware support interfacing to the Philips PDIUSBD12D
  - Generic Inari adapted Common Application Language (iCAL) interface
- *Security and Error Detection*
  - 32-byte encryption array
  - 256-bit Diffie-Hellman public key exchange
  - Packet level authentication
  - 16-bit hardware CRC
- *Inari's Powerline Exchange (PLX) Embedded Protocol*
  - Firmware Application Programming Interfaces (APIs) including QoS
  - MAC layer packet pacing (throttling)
  - Guaranteed time slots for isochronous communications
  - 32-bit device addressing capabilities
  - Automatic transmit packet formatting
  - Automatic address recognition and packet reception

1 Overview of the IPL0201 Chip

The IPL0201 ASIC is a primary component in a high-speed, low cost networking solution that allows devices to communicate using ordinary powerlines as the transmission media. Figure 1 depicts an overview of this system.

The IPL0201 connects to the powerline through an external **P**owerline **D**ata **A**ccess **A**rrangement (PDAA). Line coupling components isolate the powerline's high voltage. Data is transmitted via four modulated carriers using binary phase-shift keying or quadrature phase-shift keying.

In the transmit direction, the PDAA is comprised of filters and a linear line driver. In the receive direction, the PDAA separates the receive signal into four carriers, which are then mixed with four local oscillator signals to generate four signals. These signals are driven to the IPL0201 receiver.

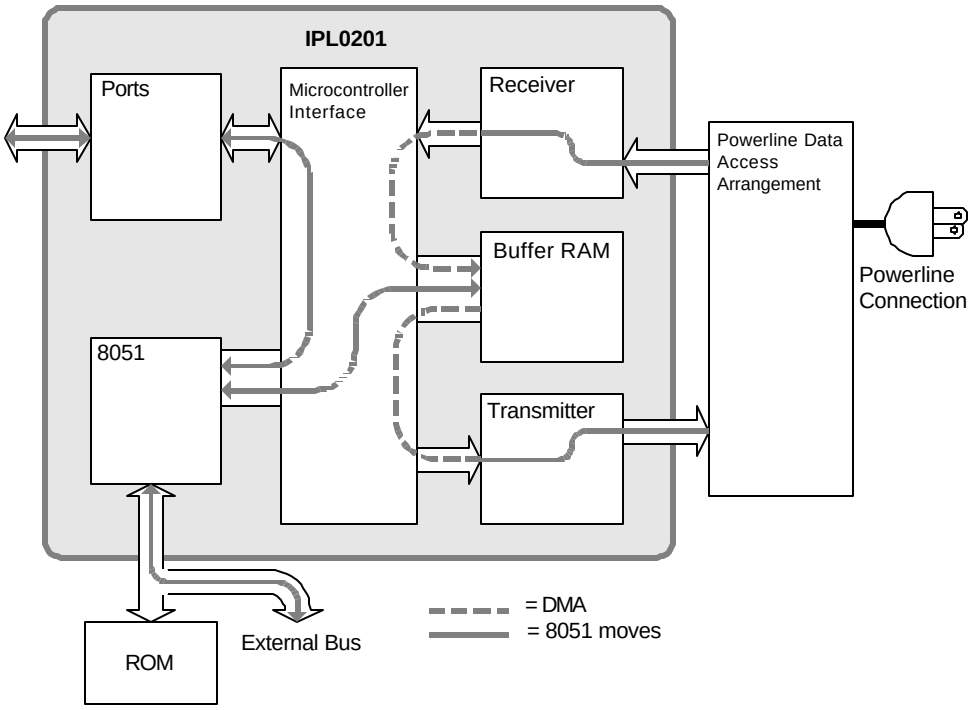


Figure 1 – IPL0201 Data Flow Block Diagram

The system is supervised by an internal 8051 microcontroller. The 8051 controls all the elements of the IPL0201 and executes code from an external ROM. The 8051 is supported by the microcontroller interface block, which is a collection of functions supporting data flow.

In the IPL0201, the microcontroller interface is also responsible for moving data on and off chip. The 8051 reads data to be transmitted from external peripherals connected to the ports or external data bus and stores this data in the on-board buffer RAM. Then, the microcontroller interface activates the transmitter block, which transfers the data without processor intervention. For receive data, the receiver block places data directly into the buffer RAM, then interrupts the 8051, which in turn formats the data for transfer to external peripherals.

Transmitter

The 8051 assembles data to be transmitted in the buffer RAM and commands the transmission to begin. The transmitter hardware handles all tasks of transmission until they are completed, transmitting four channels of data simultaneously on the powerline.

Each byte of data is converted from parallel to serial form and encoded into differential phase shift keying (PSK). Two types of modulation are supported: binary phase-shift keying, or quadrature phase-shift keying at selectable symbol times.

The transmitter is responsible for sending the preamble, encrypting the packet (if enabled), and generating a 16-bit CRC. The CRC is appended to and sent at the end of the packet.

The transmitter interrupts the 8051 with a transmit packet interrupt after all four packets are sent.

1.1 Receiver

The receive data is driven to the IPL0201 as four digital input signals, one for each carrier used on the powerline, extracted by the PDAA. The IPL0201 receives all channels in parallel.

The 8051 is not involved with the actual reception of packets beyond enabling them to begin.

A valid packet consists of a valid preamble and a destination address to which this node responds.

Each byte of data is decrypted as it is received (if decryption is enabled by the 8051, and if the packet is marked as an encrypted packet). The packet's data is also checked against its CRC.

Each data byte is stored in the internal buffer RAM for later access by the 8051.

After a valid packet is received, a receive packet interrupt is generated. After a successful reception, the hardware stops hunting for new receive packets.

The receiver gives status about each channel which is guaranteed valid after a receive packet interrupt is generated. The status stays valid until the receiver is again enabled to receive packets.

Status shows which address match occurred, which errors occurred in the reception of the packet, and at what symbol time the packet was received.

1.2 Microcontroller Interface

The microprocessor interface contains the registers necessary to interface the 8051 microcontroller with the buffer RAM, receiver, and transmitter modules. It also interfaces the 8051 with external ports and external peripherals.

1.3 8051

The microcontroller core runs the standard 8051 instruction set. It provides similar resources to the standard 8051 including timers, a full-duplex asynchronous serial port, and 256 bytes of scratchpad memory. It runs a machine cycle in 4 clock cycles (versus 12 clock cycles for a standard 8051). The Inari firmware uses some 8051 resources.

1.4 Firmware APIs

The IPL0201 comes with a PLX firmware kernel, which interfaces with the hardware. Packets are sent and received under direction of this kernel.

Customized applications can be written using the provided PLX APIs to access core protocol (kernel) functions.

2 Functional Block Diagram

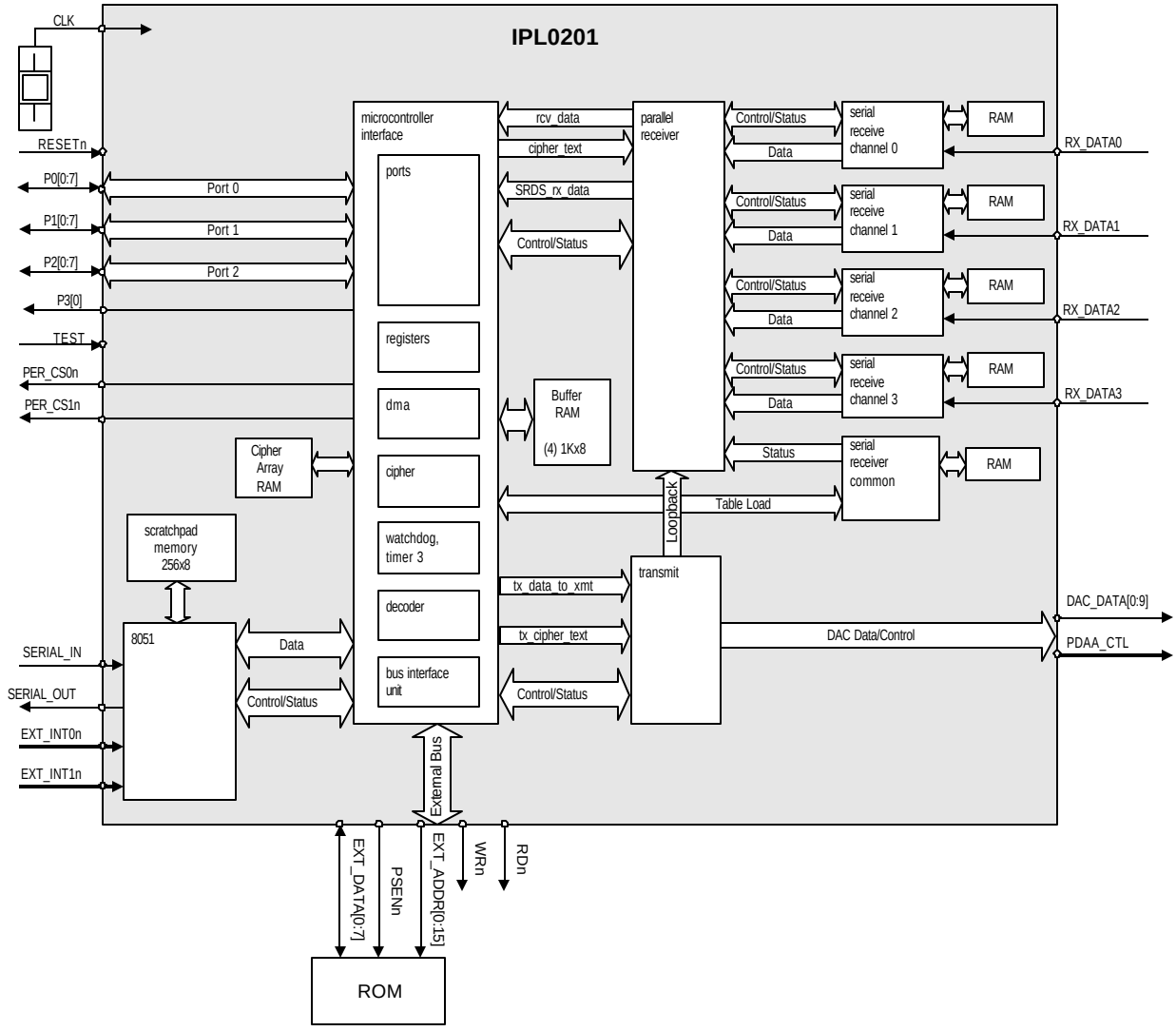


Figure 2 – Functional Block Diagram

3 Pinout

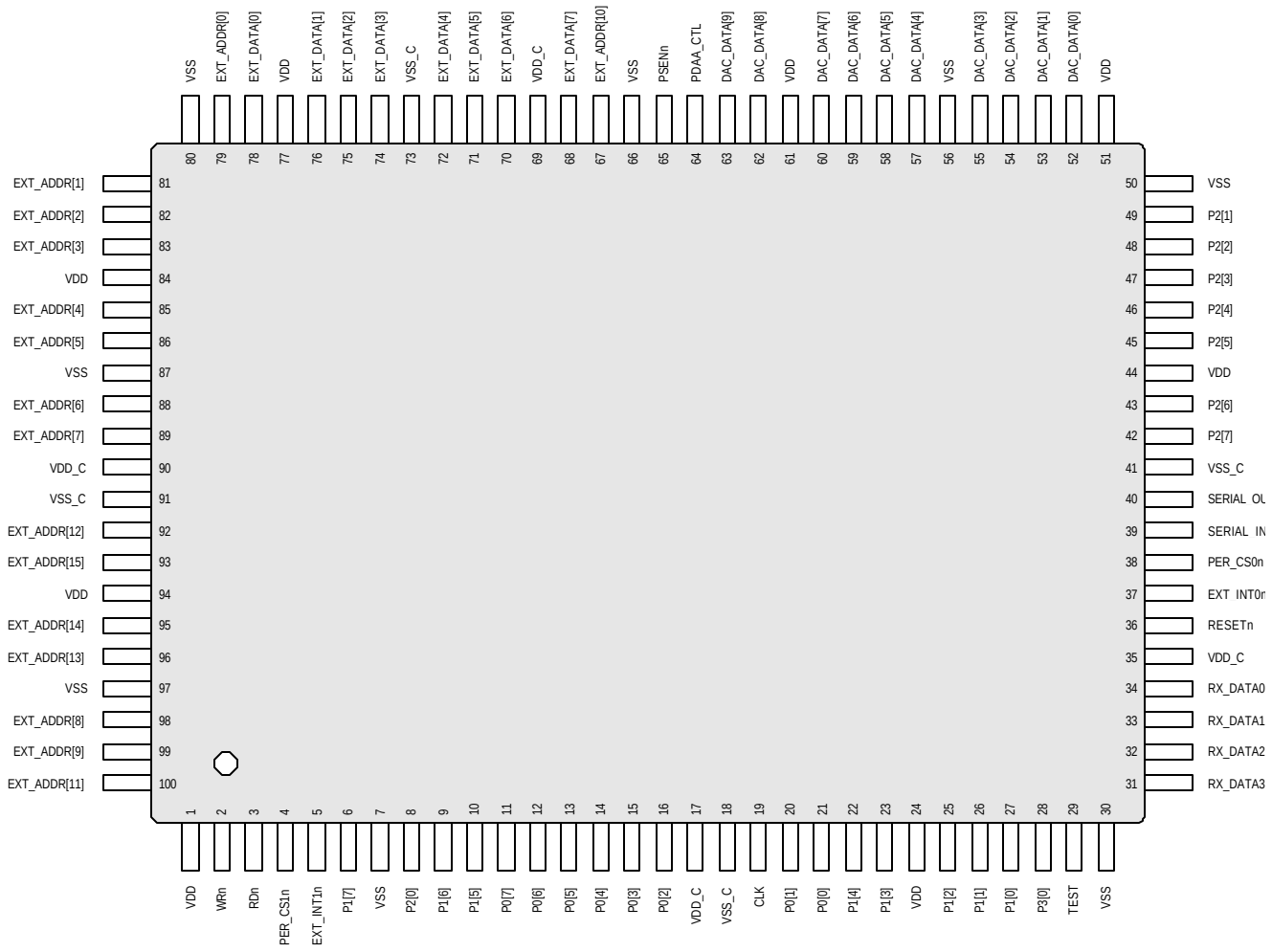


Figure 3 - Pinout Diagram

4 Pin Description

Signal Name	Function	I/O	Pin No.	Description
Ports				
P0[0:7]	Port 0 bits	Bi-directional	P0[0] – 21 P0[1] – 20 P0[2] – 16 P0[3] – 15 P0[4] – 14 P0[5] – 13 P0[6] – 12 P0[7] – 11	Port 0 functions as an 8-bit I/O port. Each input has an internal pullup resistor and a Schmitt voltage input. Each output has a 4 mA driver.
P1[0:7]	Port 1 bits	Bi-directional	P1[0] – 27 P1[1] – 26 P1[2] – 25 P1[3] – 23 P1[4] – 22 P1[5] – 10 P1[6] – 9 P1[7] – 6	Port 1 functions as an 8-bit I/O port. Each input has an internal pullup resistor and a Schmitt voltage input. Each output has a 4 mA driver.
P2[0:7]	Port 2 bits	Bi-directional	P2[0] – 8 P2[1] – 49 P2[2] – 48 P2[3] – 47 P2[4] – 46 P2[5] – 45 P2[6] – 43 P2[7] – 42	Port 2 functions as an 8-bit I/O port. Each input has an internal pullup resistor and a Schmitt voltage input. Each output except P2[2] has a 4 mA driver. P2[2] has an 8 mA driver.
P3[0]	Port 3 bit	Output	28	This signal is a programmable output. It has a 4 mA driver.
DAC				
DAC_DATA[0:9]	Data to the DAC	Output	DAC_DATA[0] – 52 DAC_DATA[1] – 53 DAC_DATA[2] – 54 DAC_DATA[3] – 55 DAC_DATA[4] – 57 DAC_DATA[5] – 58 DAC_DATA[6] – 59 DAC_DATA[7] – 60 DAC_DATA[8] – 62 DAC_DATA[9] – 63	This bus is to be wired to the inputs of an external 10 bit DAC. Each output has a 4 mA driver.
PDAA_CTL	Turn on Transmit amplifier	Output	64	This signal is to be wired to logic controlling the transmit amplifier. Its polarity is programmable. 4 mA output.

Signal Name	Function	I/O	Pin No.	Description
External Bus				
EXT_ADDR[0:15]	External address	Output	EXT_ADDR[0] – 79 EXT_ADDR[1] – 81 EXT_ADDR[2] – 82 EXT_ADDR[3] – 83 EXT_ADDR[4] – 85 EXT_ADDR[5] – 86 EXT_ADDR[6] – 88 EXT_ADDR[7] – 89 EXT_ADDR[8] – 98 EXT_ADDR[9] – 99 EXT_ADDR[10] – 67 EXT_ADDR[11] – 100 EXT_ADDR[12] – 92 EXT_ADDR[13] – 96 EXT_ADDR[14] – 95 EXT_ADDR[15] – 93	External address bus. 4 mA outputs.
EXT_DATA[0:7]	External data	Bi-directional	EXT_DATA[0] – 78 EXT_DATA[1] – 76 EXT_DATA[2] – 75 EXT_DATA[3] – 74 EXT_DATA[4] – 72 EXT_DATA[5] – 71 EXT_DATA[6] – 70 EXT_DATA[7] – 68	External data bus. Inputs have Schmitt voltage levels. Each output has 4 mA drivers. Unlike the standard 8051, this bus is not multiplexed between address and data – it is only a data bus.
WRn	8051 write	Output	2	Write enable output. Asserted low to indicate an external bus write. 4 mA output.
RDn	8051 read	Output	3	Read enable output. Asserted low to indicate an external bus read. 4 mA output.
PSENn	8051 PSEN	Output	65	Program store enable output. This asserted low signal is tied to the output enable of external ROM. 4 mA output.
EXT_INT0n	Peripheral Interrupt 0	Input	37	Interrupt input has an internal pullup resistor and a Schmitt voltage input. Asserted low.
PER_CS0n	Peripheral chip select	Output	38	Programmable asserted low chip select 0. 4 mA output.
EXT_INT1n	Peripheral Interrupt 1	Input	5	Interrupt input has an internal pullup resistor and a Schmitt voltage input. Asserted low.
PER_CS1n	Peripheral chip select	Output	4	Programmable asserted low chip select 1. 4 mA output.
Serial Port				
SERIAL_IN	Serial port in	Input	39	Serial port input has an internal pullup resistor and a Schmitt voltage input.
SERIAL_OUT	Serial port out	Output	40	Serial port output. 4 mA output.

Signal Name	Function	I/O	Pin No.	Description
Receiver				
RX_DATA0	Receive data input	Input	34	Receive data for channel 0 has an internal pullup resistor and a Schmitt voltage input.
RX_DATA1	Receive data input	Input	33	Receive data for channel 1 has an internal pullup resistor and a Schmitt voltage input.
RX_DATA2	Receive data input	Input	32	Receive data for channel 2 has an internal pullup resistor and a Schmitt voltage input.
RX_DATA3	Receive data input	Input	31	Receive data for channel 3 has an internal pullup resistor and a Schmitt voltage input.
Miscellaneous				
CLK	Clock oscillator input	Input	19	The 40.282353 MHz clock input has a Schmitt voltage input.
RESETn	Reset input.	Input	36	This active low reset input has an internal pullup resistor and a Schmitt voltage input. It must be active for at least 4 clock cycles after power is stable and within operating conditions.
TEST	Test mode	Input	29	Asserted high test pin for manufacturing use only. It is recommended that this input be tied low through a 4.7 k – 10 k ohm resistor.
Power				
VSS	Digital Ground	Ground	7, 30, 50, 56, 66, 80, 87, 97	Digital I/O Ground.
VDD	Digital Supply	Power	1, 24, 44, 51, 61, 77, 84, 94	Digital I/O 3.3 Volt Supply.
VSS_C	Ground for Core	Ground	18, 41, 73, 91	Digital Ground for core logic.
VDD_C	Power Supply for Core	Power	17, 35, 69, 90	Digital 3.3 Volt Supply for core logic.

5 Electrical Specifications

5.1 CLK Cycle Timing

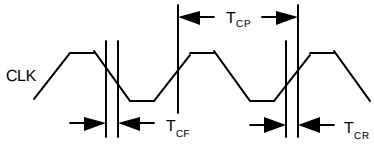


Figure 4 –CLK Cycle Timing

Parameter	Symbol	Min	Typical	Max	Units
Clock Fall Time	T_{CF}			5	ns
Clock Rise Time	T_{CR}			5	ns
Clock Frequency	$1/T_{CP}$		40.282353		MHz

5.2 Oscillator Specification (40.282353 MHz Oscillator)

Parameter	Condition	Min	Typical	Max	Units
Frequency Tolerance	25° C			± 25	ppm
Frequency Stability	0° to 70°C			± 25	ppm
Aging	Per Year			± 5	ppm

5.3 Program Memory Read Cycle Timing

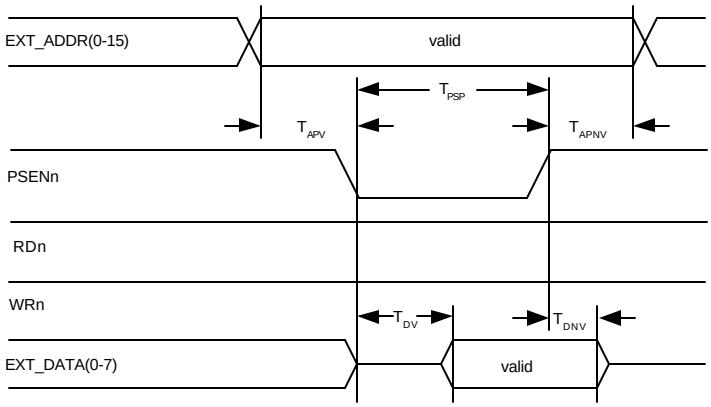


Figure 5 – Program Memory Read Cycle Timing

Parameter	Symbol	Min	Max	Units
Address Valid to PSENn Valid	T_{APV}	15		ns
Address Hold Time from PSENn Not Valid	T_{APNV}	15		ns
PSENn Valid to Data Valid	T_{DV}		28	ns
Data Hold Time from PSENn Not Valid	T_{DNV}	0		ns
PSENn Width	T_{PSP}	$2*T_{CP}$		ns

5.4 External Data Memory Read Cycle Timing

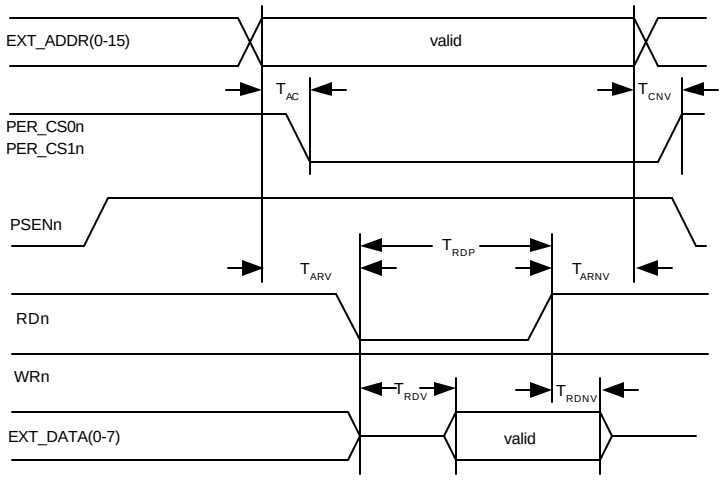


Figure 6 –External Data Memory Read Cycle Timing

Parameter	Symbol	Min	Max	Units
Address Valid to RDn Valid	T_{ARV}	15		ns
Address Hold Time from RDn Not Valid	T_{ARNV}	15		ns
Address Valid to PER0_CSn Valid	T_{AC}		5	ns
Address Not Valid to PER0_CSn Not Valid	T_{CNV}		5	ns
RDn Valid to Data Valid	T_{RDV}		28	ns
Data Hold Time from RDn Not Valid	T_{RDNV}	0		ns
RDn Width	T_{RDP}	$2*T_{CP}$		ns

5.5 External Data Memory Write Cycle Timing

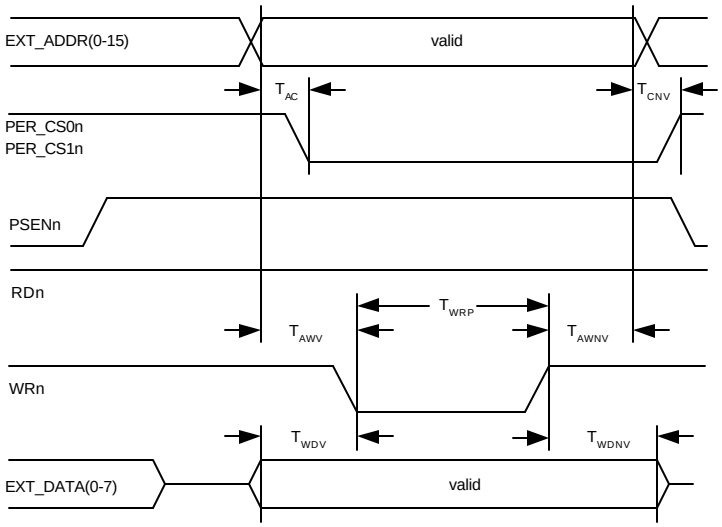


Figure 7 – External Data Memory Write Cycle Timing

Parameter	Symbol	Min	Max	Units
Address Valid to WRn Valid	T_{AWV}	15		ns
Address Hold Time from WRn Not Valid	T_{AWNV}	15		ns
Address Valid to PER0_CSn Valid	T_{AC}		5	ns
Address Not Valid to PER0_CSn Not Valid	T_{CNV}		5	ns
Data Valid to WRn Valid	T_{WDV}	15		ns
Data Hold Time from WRn Not Valid	T_{WDNV}	15		ns
WRn Width	T_{WRP}	$2*T_{CP}$		ns

5.6 CLK to DAC_DATA Timing

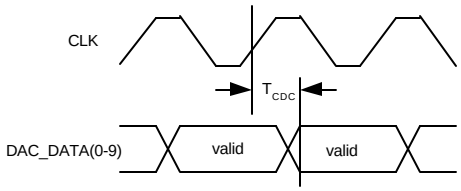


Figure 8 –CLK to DAC_DATA Timing

Parameter	Symbol	Min	Max	Units
CLK to DAC_DATA	T_{CDC}		20	ns

5.7 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Supply Voltage	VDD, VDD_C		-0.3		4.0	Volts
Input Pin Voltage			-0.3		VDD+0.3	Volts
Input Pin Current			-10		10	mA
Storage Temperature			-55°		150°	C
Lead Temperature		For 10 seconds			300°	C

5.8 DC Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Supply Voltage	VDD, VDD_C		3.0		3.6	Volts
Ambient Temperature			0°		70°	C
Junction Temperature			0°		85°	C
Low Level Input Voltage	V_{il}				0.2*VDD	Volts
High Level Input Voltage	V_{ih}		0.8*VDD			Volts
Low Level Input Current	I_{il}				-1.0	uA
High Level Input Current	I_{ih}		1.0			uA
Input Pullup Current	I_{pu}		-29		-71	uA
Input Pull-Down Current	I_{pd}		36		110	uA
Schmitt Hysteresis	Vh		0.9			Volts
Low Level Output Current	I_{ol}	VDD = 3.0V			4	mA
Low Level Output Current*	I_{ol}	VDD = 3.0V			8	mA
High Level Output Current	I_{oh}	VDD = 3.0V			4	mA
High Level Output Current*	I_{oh}	VDD = 3.0V			8	mA
Input Leakage	I_{oz}		-10		10	uA
High Level Output Voltage	V_{oh}	VDD = 3.0V	2.4			Volts
Low Level Output Voltage	V_{ol}	VDD = 3.0V			0.4	Volts
Static Supply Current	IDDS	VDD = 3.0V, CLK stopped		265		uA
Supply Current	IDD	VDD = 3.0V		190		mA

* P2[2] output only

6 Packaging Specifications

6.1 Package Outline Dimensions

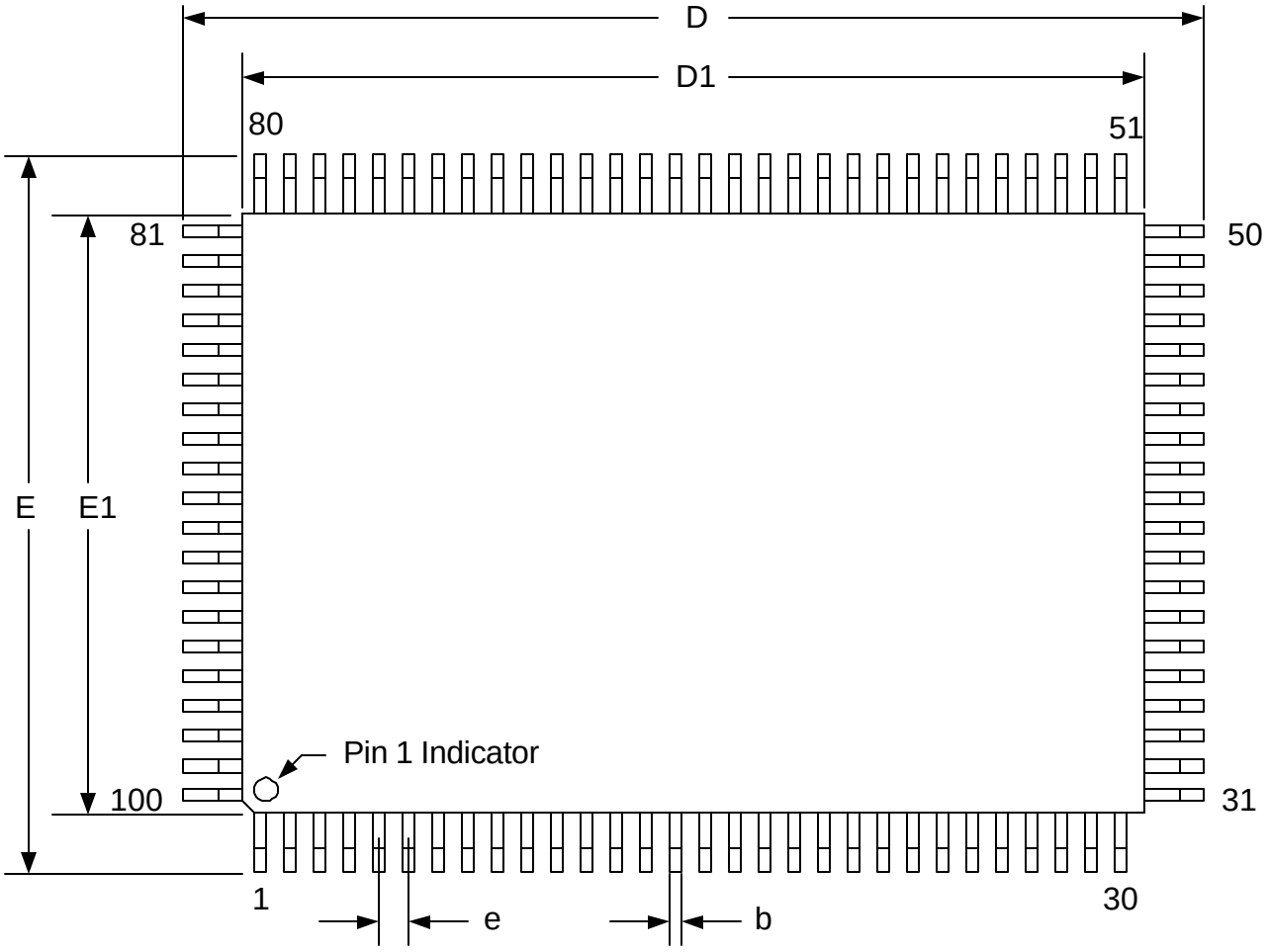


Figure 9 – Package Outline Dimensions – Top View

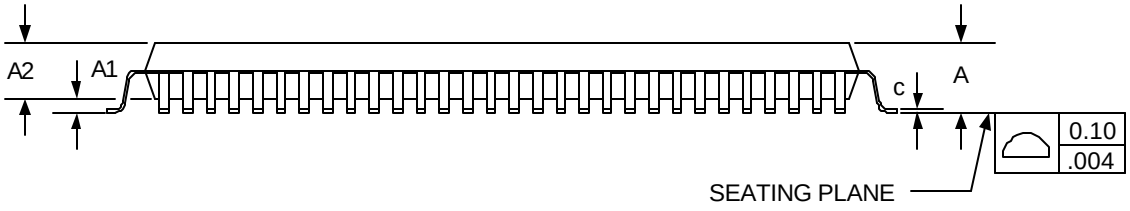


Figure 10 – Package Outline Dimensions – Side View

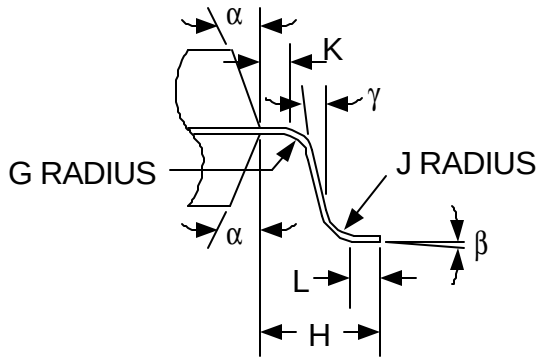


Figure 11 – Package Outline Dimensions – Pin Side View

Symbol	Min	Max	Units
A	-	3.40	mm
A1	0.25	-	mm
A2	2.57	2.87	mm
D	23.65	24.15	mm
D1	19.90	20.10	mm
E	17.65	18.15	mm
E1	13.90	14.10	mm
L	0.65	0.95	mm
e	0.65 BSC		mm
B	0.22	0.38	mm
c	0.13	0.23	mm
	12	16	degrees
	0	7	degrees
	0	-	degrees
G	0.13	-	mm
H	1.95 REF		mm
J	0.13	0.30	mm
K	0.40	-	mm
2H	3.9		mm