μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



FEATURES

- ♦ 2 × 4 bidirectional input/output stages at 24V
- ♦ Input/output mode programmable in 4-bit blocks
- Guaranteed high-side driving capability of 100mAdc and 500mApeak for pulse load
- ♦ Short-circuit-proof drivers with high dielectric strength
- ◆ Low saturation voltage of 0.6V/100mA and 2.0V/500mA
- Integrated flyback circuits
- PWM function with programmable duty cycle
- ♦ Flash mode for the outputs
- Power outputs can be disabled together
- Programmable current sources define logic levels and allow load monitoring
- Digital input filters with externally adjustable filtering times
- Can be bus operated due to the high-speed μP interface
- Programmable interrupt output
- Voltage and two-stage temperature monitoring

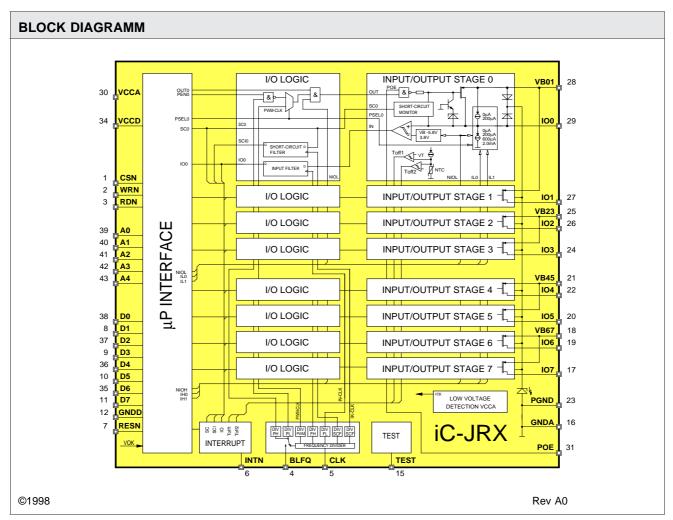
APPLICATIONS

 Dual quad high-side driver as a bidirectional μP interface with digital filtering in industrial 24V applications

PACKAGES



PLCC44



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μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



Rev A0, 2/23

DESCRIPTION

iC-JRX is an 8-fold high-side driver with integrated control logic, internally divided into two independent blocks (nibbles). Both blocks can be individually set to input or output. The μP interface is made up of eight data, five address and three control pins. Two further clock inputs control internal sequences (input filter, pulse operation of the outputs). Starting with reset state, various register partitionings dependent on the selected operating mode are possible.

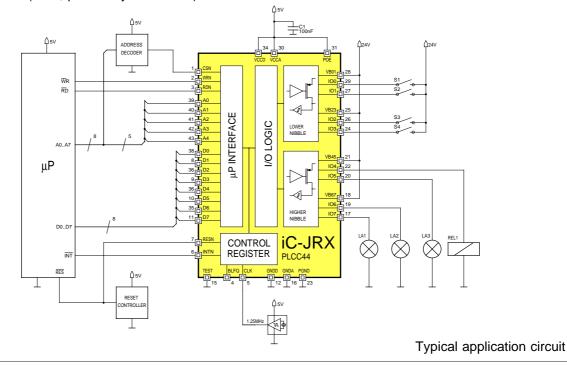
Input mode is used to log logic levels at 24V. An interrupt message can be generated when a signal at the inputs changes. Spurious signals are rejected by the device's adjustable digital filters. When the inputs are open the programmable pull-down current sets defined levels and acts as the bias current for switching contacts.

In output mode the power output stages can drive any desired load to GND (e.g. lamps, long cables or relays) at a continuous current of 100mA or 500mA in pulse operation. Spikes and flyback currents are discharged through the integrated flyback circuits. All output stages are short-circuit-proof and two-stage temperature monitoring (with interrupt messages) protects against thermal damage caused by large power dissipation. A short circuit at one of the outputs can cause an interrupt; the current short circuit status can be scanned via the μP interface. Pulse mode can be selected for each output, such as for indicator lamps in plugboards, in order to offload the control software used. The actual switching level of the output can be read out via the μP interface and be used to check for cable fractures with the pull-up currents. A PWM signal can also be switched to any selected output. All outputs can be switched off via a mutual disable input e.g. by a processor-independent watchdog circuit.

An interrupt pipeline which prevents the loss of interrupts allows reliable processing of interrupts using the applied control software.

With low voltage the voltage monitor resets all registers and in doing so switches off the power output stages.

Diodes protect all inputs and outputs against ESD. The device is also immune to burst transients according to IEC 1000-4-4 (4 kV; previously IEC 801-4).



μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS

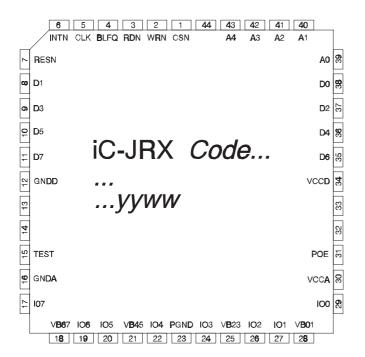


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PACKAGES PLCC44 to JEDEC Standard

PIN CONFIGURATION PLCC44

(top view)



PIN FUNCTIONS PLCC44

No.	Name	Fct.	Description	No.	Name	Fct.	Description
1	CSN	I	Chip Select	23	PGND		Ground (ESD protection circuitry)
2	WRN	I	Write Enable	24	IO3	В	I/O Stage 3
3	RDN	1	Read Enable	25	VB23		Power Supply Driver Stage 2+3
4	BLFQ	1	Clock Flash Mode	26	102	В	I/O Stage 2
5	CLK	I	Clock Filter and PWM Function	27	IO1	В	I/O Stage 1
6	INTN	0	Interrupt Message	28	VB01		Power Supply Driver Stage 0+1
7	RESN	I	Reset	29	100	В	I/O Stage 0
8	D1	В	Data Bus Bit 1	30	VCCA		5V Supply Voltage (analog section)
9	D3	В	Data Bus Bit 3	31	POE	1	Power Output Enable
10	D5	В	Data Bus Bit 5	32	n.c.		·
11	D7	В	Data Bus Bit 7	33	n.c.		
12	GNDD		Ground (digital section)	34	VCCD		5V Supply Voltage (digital section)
13	n.c.		,	35	D6	В	Data Bus Bit 6
14	n.c.			36	D4	В	Data Bus Bit 4
15	TEST	В	Test Pin	37	D2	В	Data Bus Bit 2
16	GNDA		Ground (analog section)	38	D0	В	Data Bus Bit 0
17	107	В	I/O Stage 7	39	A0	1	Address Bus Bit 0
18	VB67		Power Supply Driver Stage 6+7	40	A1	1	Address Bus Bit 1
19	106	В	I/O Stage 6	41	A2	1	Address Bus Bit 2
20	IO5	В	I/O Stage 5	42	A3	1	Address Bus Bit 3
21	VB45		Power Supply Driver Stage 4+5	43	A4	1	Address Bus Bit 4
22	104	В	I/O Stage 4	44	n.c.		
			ŭ				

Functions: I= Input, O= Output, B= bidirectional

External wiring VCCA, VCCD to +5V and GNDA, GNDD, PGND to 0V required.

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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PROGRAMMING

Registe	r Ove	ervie	w									
		Addre										
A(40)d	A4	АЗ	A2	A1	A0	Write	Read					
0	0	0	0	0	0	-	Input Register 1					
1	0	0	0	0	1	-	Change-of-input Message ²					
2	0	0	0	1	0	-	Interrupt Status Register					
3	0	0	0	1	1	-	Overcurrent Message ³					
4	0	0	1	0	0	-	Overcurrent Status					
5	0	0	1	0	1	-	Device ID					
6	0	0	1	1	0	Output	Output Register					
7	0	0	1	1	1	Flash Pu	lse Enable					
8	0	1	0	0	0	Change-of-input	Interrupt Enable ⁴					
9	0	1	0	0	1	Overcurrent In	Overcurrent Interrupt Enable					
10	0	1	0	1	0	Control Word	d 1 (I/O filters)					
11	0	1	0	1	1	Control Word 2	(I/O pin functions)					
12	0	1	1	0	0	Control Word 3 (fl	lash pulse settings)					
13	0	1	1	0	1	Control World 4 (filter setting	ngs for overcurrent message)					
14	0	1	1	1	0	Control Word 5 (PWM e	enable and pin selection)					
15	0	1	1	1	1	PWM I	Register					
16	1	0	0	0	0		-					
							-					
26	1	1	0	1	0		-					
27	1	1	0	1	1	-	A/D Interface					
28	1	1	1	0	0	Test Ro	Test Register 1					
29	1	1	1	0	1	Test Ro	Test Register 2					
30	1	1	1	1	0	Test Ro	egister 3					
31	1	1	1	1	1	Test Cont	rol Register					

Reads the inputs or reads back the outputs, depending on I/O pin mode
 For I/O pins in input mode (register is '0' in output mode)
 For I/O pins in output mode (register is '0' in input mode)

⁴) Only writable in input mode

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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Control	Control Word 1 (I/O filters) Add.: 10											
reset entry:												
	higher nil	bble			lower nibble							
Bit Name	7 BYPH	6 -	5 FH1	4 FH0	3 BYPL	2 -	1 FL1	0 FL0				

higher nibble

Bit 7 BYPH	0	I/O filters a Bypass for		the I/O signals are re	processed in their unfiltered state.	(r)
Bit 54		FH1	FH0	Filter times		
FH10		0	0	14,5 × tc(CLK)	± 1 × tc(CLK)	
		0	1	896,5 × tc(CLK)	\pm 64 \times tc(CLK)	
		1	0	$3.584,5 \times tc(CLK)$	\pm 256 \times tc(CLK)	
		1	1	$7.168,5 \times tc(CLK)$	\pm 512 \times tc(CLK)	

lower nibble

Bit 3 BYPL	0	I/O filters a Bypass for		(r) he I/O signals are reprocessed in their unfiltered state.						
Bit 10		FL1	FL0	Filter times						
FL10		0	0	14,5 × tc(CLK)	\pm 1 \times tc(CLK)	(r)				
		0	1	896,5 × tc(CLK)	\pm 64 \times tc(CLK)					
		1	0	3.584,5 × tc(CLK)	\pm 256 \times tc(CLK)					
		1	1	$7.168,5 \times tc(CLK)$	\pm 512 \times tc(CLK)					

'-' Free memory location without a function. Status after a reset is '0' 'xx'h Indicates hexadecimal data for logic states. 'x' indicates binary data

(r) Status after a reset

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



Rev A0, 6/23

Control	Control Word 2 (I/O pin functions) Add.: 11											
reset entry:												
	higher ni	bble			lower nil	lower nibble						
Bit Name	7 NIOH	6 -	5 IH1	4 IH0	3 NIOL	2 -	1 IL1	0 ILO				

higher nibble

Bit 7 0 Input mode Output mode									
Bit 54		Current sou	rces at I/O p	pins 47					
IH10		IH1		in input mode (sources low-side)	in output mode (sources high-side)				
		0 0 1 1	0 1 0 1	0μΑ 200μΑ 600μΑ 2mA	0μΑ 200μΑ 0μΑ 200μΑ	(r)			

lower nibble

Bit 3 NIOL	0	Input mode Output mod				
Bit 10		Current so	urces at I/O pins	s 03		
IL10		IL1 IL0		in input mode (sources low-side)	in output mode (sources high-side)	
		0	0 1	0μΑ 200μΑ	0μA 200μA	
		1	0 1	600μA 2mA	0μA 200μA	(r)

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



Rev A0, 7/23

Control	Control Word 3 (flash pulse settings) Add.: 12											
reset enti												
	higher nibb	ole			lower nibble							
Bit Name	7 NOBLFQ	6 NOCLK	5 PH1	4 PH0	3 -	2 -	1 PL1	0 PL0				

higher nibble

Bit 7 0 Flash pulse is generated from the external clock signal at BLFQ NOBLFQ 1 Flash Pulse is generated from clock signal CLK										
Bit 6										
Bit 54		Flash frequ	Flash frequency for I/O pins 47							
PH10		PH1	PH0	NOBLFQ= 0		NOBLFQ= 1				
		0	0	f(BLFQ)		f(CLK) / 2 ¹⁹				
		0	1	f(BLFQ) / 2		f(CLK) / 2 ²⁰				
		1	0	f(BLFQ) / 4		f(CLK) / 2 ²¹				
		1	1	f(BLFQ) / 16	(r)	f(CLK) / 2 ²³				

lower nibble

Bit 10	Flash frequency for I/O pins 03								
PL10	PL1	PL0	NOBLFQ= 0	NOBLFQ= 1					
	0	0	f(BLFQ)	f(CLK) / 2 ¹⁹					
	0	1	f(BLFQ) / 2	f(CLK) / 2 ²⁰					
	1	0	f(BLFQ) / 4	f(CLK) / 2 ²¹					
	1	1	f(BLFQ) / 16	(r) f(CLK) / 2 ²³					

Control \	Control Word 4 (filter settings for overcurrent message) Add.: 13											
	reset entry: 00h											
Bit	7	6	5	4	3	2	1	0				
Name	EOI	-	-	SCFH	BYPSCF	-	-	SCFL				

Bit 7	0	No effect	(r)
EOI	1	"DELETE"s the interrupt message (change-of-input message; interrupt status register, overcurrent message), accepts successive interrupts from the pipeline, deletes the message at INTN when the pipe is empty;	line
		Bit automatically resets to '0'.	
Bit 4 SCFH	0	Overcurrent message with 2.3ms filtering (higher nibble) Overcurrent message with 4.6ms Filtering (higher nibble)	(r)
		Gives the filter times with the maximum clock frequency permitted at CLK, i.e. 1.25 MHz: 2.3ms from (2689,5 \pm 192)× t(CLK) and 4.6ms from (5378,5 \pm 384) × t(CLK) respectively	
Bit 3 BYPSCF	0	Filters for the overcurrent message are active Bypass for the filters: overcurrent messages are reprocessed in their unfiltered state	(r)
Bit 0 SCFL	0	Overcurrent message with 2.3ms filtering (lower nibble) Overcurrent message with 4.6ms filtering (lower nibble)	(r)

μΡ INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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Control V	Nord 5	(PWM enable and	d pin selectio	n)				Add.: 14
							res	set entry: 00h
Bit Name	7 -	6 -	5 -	4 PWMEN	3 PWMPN	2 PWM ADR(2)	1 PWM ADR(1)	0 PWM ADR(0)
Bit 4 PWMEN	0	PWM "DISABLE PWM "ENABLE sources are swi	D": the output s	elected with P\	VMADR receiv	ves the PWM s	ignal. The relev	(r) ant current
Bit 3 PWMPN	0	PWM signal act PWM signal act						(r)
Bit 20		PWMADR2	PWMADR1	PWMADRO	Selected I	/O pin		
PWMADR 2	20	1111	0 0 1 1 0	0 1 0 1 0	IO0 (cr IO1 IO2 IO3 IO4 IO5	ontrol line PSE	L0= 1)	

PWM Re	gister							Add.: 15
							re	set entry: 00h
Bit Name	7 PWM7	6 PWM6	5 PWM5	4 PWM4	3 PWM3	2 PWM2	1 PWM1	0 PWM0
Bit 70 PWM70	'00'h ''h 'FF'h	Duration of the	OFF" (continous PWM signal in CON" (continous	n steps of 16× t	t(CLK)			(r)
		The PWM reg		s the pulse leng	gth of the PWM	signal. Output	selection and e	nable are set via

106 107

μΡ INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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	egister (reads)	ad only) output feedba	ack					Add.: 0
							!	eset entry: 00h
Bit Name	7 IN7	6 IN6	5 IN5	4 IN4	3 IN3	2 IN2	1 IN1	0 INO
Bit 70 IN70	0	Input/Output	IOx reads '0' IOx reads '1'	Ox (via I/O filter	or hypaca)			(r)

es in inpu	essage (read ut mode	only)					Add.: 1
						re	set entry: 00h
7 DCH7	6 DCH6	5 DCH5	4 DCH4	3 DCH3	2 DCH2	1 DCH1	0 DCH0
0				•	nessages		(r
	successive int interrupt pipeli	errupts which c ine. If this happ	occur during the ens, the messa	read-out phasinge at INTN car	e and before a nnot be deleted	reset with EOI a by EOI, i.e. IN	are trapped by ar
		DCH7 DCH6 No change of Input IOx has Read access successive intinterrupt pipeli remains on low	DCH7 DCH6 DCH5 No change of state at the inp Input IOx has had a change of Read access gates off chang successive interrupts which of interrupt pipeline. If this happ remains on low. In this instan	DCH7 DCH6 DCH5 DCH4 No change of state at the input IOx or no int Input IOx has had a change of state enabled Read access gates off changes to the regist successive interrupts which occur during the interrupt pipeline. If this happens, the messa remains on low. In this instance, EOI fills the	DCH7 DCH6 DCH5 DCH4 DCH3 O No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt makes access gates off changes to the register; the register successive interrupts which occur during the read-out phase interrupt pipeline. If this happens, the message at INTN car remains on low. In this instance, EOI fills the change-of-inp	DCH7 DCH6 DCH5 DCH4 DCH3 DCH2 No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt messages Read access gates off changes to the register; the register is reenabled or successive interrupts which occur during the read-out phase and before a interrupt pipeline. If this happens, the message at INTN cannot be deleted	7 DCH7 6 DCH6 5 DCH5 4 DCH4 3 DCH3 2 DCH2 DCH1 0 No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt messages Read access gates off changes to the register; the register is reenabled only when reset a successive interrupts which occur during the read-out phase and before a reset with EOI interrupt pipeline. If this happens, the message at INTN cannot be deleted by EOI, i.e. INT remains on low. In this instance, EOI fills the change-of-input message from the pipeline.

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Interrup	t Status Reg	gister (read	only)					Add.: 2
							r	eset entry: 00h
	higher nibble				lower nibble			
Bit Name	7 DCHI	6 IET2	5 IET1	4 ISCI	3 -	2 ET2	1 ET1	0 SCS

higher nibble

overcurr	ent, exces	ssive temperature, change-of-input data (interrupts stored)	
		Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts for IET1 and IET2 which occur during the read-out phase and before a reset wit EOI are trapped (pipeline). If this happens, the message at INTN cannot be deleted by EOI, i.e. INTN constantly remains on low. In this instance, EOI fills the excessive temperatue message from the pipe	h
Bit 7 DCHI	0	No message Interrupt through change-of-input message	(r)
Bit 6 IET2	0	No message Interrupt through excessive temperature level 2	(r)
Bit 5 IET1	0	No message Interrupt through excessive temperature level 1	(r)
Bit 4 ISCI	0	No message Interrupt through overcurrent message	(r)

lower nibble

overcurr	ent status	s, excessive temperature status (real time signals, at the time of readout)	
Bit 2 ET2	0	No error message Excessive temperature level 2 (shutdown)	(r)
Bit 1 ET1	0	No error message Excessive temperature level 1 (warning)	(r)
Bit 0 SCS	0	No error message Overcurrent status (e.g. caused by low-side short circuit)	(r)

Overcur	rent Messa	age (read onl	y)					Add.: 3
							re	eset entry: 00h
Bit Name	7 SCI7	6 SCI6	5 SCI5	4 SCI4	3 SCI3	2 SCI2	1 SCI1	0 SCI0
Bit 70 SCI70	0 1	Read access successive ir an interrupt p remains on lo	gates off chan- terrupts which ipeline. If this how. In this insta or IOx pins in ir	ges to the regis occur during th nappens, the m nce, EOI fills th	ster; the registe e read-out phasessage at INTN	se and before a	only when reset reset with EOI eted by EOI, i.e.	•

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Overcur	rent Statu	s (read only)						Add.: 4
							r	eset entry: 00h
Bit Name	7 SC7	6 SC6	5 SC5	4 SC4	3 SC3	2 SC2	1 SC1	0 SC0
Bit 70 SC70	0	This signal a	in output IOx, e	alysis and does	not generate a	any interrupts (re	eal time, no reç	gister).

Device I	dentificat	ion (read on	ly)					Add.: 5
							re	eset entry: 00h
Bit Name	7 -	6 -	5 DID5	4 DID4	3 DID3	2 DID2	1 DID1	0 DID0
Bit 50 DID50			· iC-JRX: '00 0000 vith RESN= '0' an	` ,	tage			(r)

Output-R		utput function	n					Add.: 6
							re	set entry: 00h
Bit Name	7 OUT7	6 OUT6	5 OUT5	4 OUT4	3 OUT3	2 OUT2	1 OUT1	0 OUT0
Bit 70 OUT70	0		er "OFF" er "ON", i.e. no	-	,			(r)

			Flash Pulse Enable for I/O stages with output function								
						re	set entry: 00h				
7 PEN7	6 PEN6	5 PEN5	4 PEN4	3 PEN3	2 PEN2	1 PEN1	0 PEN0				
Bit 70 0 Flash pulse "DISABLED" (r) PEN70 1 Flash pulse "ENABLED"											
	0 F	PEN7 PEN6 O Flash pulse "DIS Flash pulse "EN.	PEN7 PEN6 PEN5 D Flash pulse "DISABLED" Flash pulse "ENABLED"	PEN7 PEN6 PEN5 PEN4 D Flash pulse "DISABLED"	PEN7 PEN6 PEN5 PEN4 PEN3 D Flash pulse "DISABLED" Flash pulse "ENABLED"	PEN7 PEN6 PEN5 PEN4 PEN3 PEN2 D Flash pulse "DISABLED" Flash pulse "ENABLED"	7				

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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	Change-of-input Interrupt Enable for I/O stages with input function Add.: 8								
							re	eset entry: 00h	
Bit Name	7 IEN7	6 IEN6	5 IEN5	4 IEN4	3 IEN3	2 IEN2	1 IEN1	0 IEN0	
Bit 70 IEN70 IEN70 IEN70 Bit 70 IEN70 IEN70								(r) terrupt.	

Overcurrent Interrupt Enable Add.: 9								
							res	set entry: 00h
Bit Name	7 SCEN7	6 SCEN6	5 SCEN5	4 SCEN4	3 SCEN3	2 SCEN2	1 SCEN1	0 SCEN0
Bit 70 SCEN70	0	"DISABLED" fo	•	ort-circuit at IO:	x triggers an int	terrupt.		(r)
		SCENx enable	s the output IO:	x for interrupt.				

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



Rev A0, 13/23

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

ltem	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
G001	VCCD VCCA	Supply Voltage VCCD, VCCA					V
G002	VB	Supply Voltage VB			-0.3	30	V
G003	V(IO)	Voltage at IO07	IOx= off		-10	30	V
G004	Idc(IO)	Current in IO07		1	-500	100	mA
G005	lpk(IO)	Pulse Current in IOx	IOx= hi (*), τ= 2ms, T≥ 2s	2	-1.0		Α
G006	Imax()	Current in VCCD, VCCA			-50	50	mA
G007	Imax(VB)	Current in VB01, VB23, VB45, VB67			-4	4	Α
G008	Ic()	Current in Clamping Diodes CSN, WRN, RDN, A04, D07, RESN, CLK, BLFQ, POE	D07 with input function		-20	20	mA
G009	I()	Current in D07, INTN	D07 with output function		-25	25	mA
G010	llu()	Pulse Current in CSN, WRN, RDN, A04, D07, RESN, CLK, BLFQ, INTN, POE, IO07 (Latch-Up Strength)	pulse duration < 10μs, all in-/outputs open		-100	100	mA
E001	Vd()	ESD Susceptibility at all Pins	MIL-STD-883.D, Method 3015.7; HBM 100pF discharged through $1.5 \mathrm{k}\Omega$			2	kV
E002	Vb()	Permissible Burst-Transients at IO07	according to IEC 1000-4-4			4	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

^(*) IOx= hi: pin set to output, active high, x=0..7

THERMAL DATA

Operating Conditions: VCCD= VCCA= 5V $\pm 10\%$, VB= 24V $\pm 5\%$, GNDA= GNDD= PGND= 0V, alle inputs wired (to hi respectively to lo)

Item	Symbol	Parameter	Conditions	Fig.				Unit
					Min.	Тур.	Max.	
T1	Та	Operating Ambient Temperature Range			0		70	°C
T2	Rthja	Thermal Resistance Chip to Ambient	surface mounted on PCB, no additional cooling areas			55		K/W

μΡ INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



Rev A0, 14/23

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= $5V \pm 10\%$, VB= $24V \pm 5\%$, GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

ltem	Symbol	Parameter	Conditions	Tj	Fig.				Uni
				°C		Min.	Тур.	Max.	
Total	Device								
001	VCCA	Permissible Supply Voltage VCCA				4.5		5.5	V
002	I(VCCA)	Supply Current in VCCA					7.5	13	m <i>P</i>
003	I(VCCA)	Supply Current in VCCA	no supply voltage VB					25	m/
004	VCCD	Permissible Supply Voltage VCCD				4.5		5.5	V
005	I(VCCD)	Supply Current in VCCD (static)	all logic inputs lo= 0V or hi= VCCD				0.3	3	m/
006	I(VCCD)	Supply Current in VCCD (dynamic)	continously repeated read access: tlo(RDN)= thi(RDN)= 200ns; data word changes every other cycle between "00" and "FF", CL(D07)= 200pF					35	mA
007	I(VCCD)	Supply Current in VCCD	all logic inputs lo= 0.8V				80		m <i>P</i>
800	I(VCCD)	Supply Current in VCCD	all logik inputs hi= 2.0V				100		m/
009	VB	Permissible Supply Voltage VB (operating range)				22.8		25.2	V
010	I(VB)	Supply Current in VB	POE= hi, IOx= hi, no load				8.5	14	m/
011	I(VB)	Supply Current in VB	IOx= off				2	4	m/
012	Vc()lo	ESD Clamp Voltage lo at VCCA, VCCD, VB	I()= -20mA			-1.4		-0.3	V
013	Vc()hi	ESD Clamp Voltage hi at VCCA	I()= 20mA					11	V
014	Vc()hi	ESD Clamp Voltage hi at VB	I()= 20mA			30	47	60	V
015	Vc()lo	ESD Clamp Voltage lo at IOx	I()= -20mA			-30		-10	V
016	Vc()hi	ESD Clamp Voltage hi at IOx	I()= 20mA			30	47	60	V
I/O S1	ages: Hig	h-Side Driver IO07							
101	Vs()hi	Saturation Voltage hi	Vs()hi= VB -V(IOx); I(IOx)= -10mA	1				0.2	V
102	Vs()hi	Saturation Voltage hi	Vs()hi= VB -V(IOx); I(IOx)= -100mA	1				0.6	V
103	Vs()hi	Saturation Voltage hi for pulse load	$Vs()hi= VB -V(IOx); \\ I(IOx)= -500mA, \ \tau= 2ms, \ T \ge 2s$	2				2.0	V
104	lsc()hi	Overcurrent Cut-off	IOx= hi, V(IOx)= 0VB-3V			-1.8		-0.6	Α
105	It()scs	Threshold Current for Overcurrent Message				-1.2		-0.6	А
106	Vc()lo	Free-wheeling Clamp Voltage	I(IOx)= -100mA			-15		-12	V
107	SRhi()	Slew Rate hi	CL= 0100pF, RL= 240Ω1kΩ			15		40	V/µ
108	SRIo()	Slew Rate Io	CL= 0100pF, RL= 240Ω1kΩ			15		40	V/µ
109	tplh()	Propagation Delay until IOx: lo→hi	write cycle, WRN: $Io \rightarrow hi$ until $V(IOx) > V0(IOx) + 1V$					5	μs
110	tphl()	Propagation Delay until IOx= off	write cycle, WRN= lo→hi until V(IOx) < 80% (VB-Vs(IOx)hi)					5	μs

μΡ INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 24V ±5%, GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

ltem	Symbol	Parameter	Conditions	Tj	Fig.				Unit
				°C		Min.	Тур.	Max.	
I/O S	tages: Cui	rrent Sources at IO07							
201	lpd()	Pull-down Current Source (200μA)	IOx with input function, IL1= IH1= 0, IL0= IH0= 1, V(IOx)= 3VVB			120	200	280	μА
202	lpd()	Pull-down Current Source (600μA)	IOx with input function, IL1= IH1= 1, IL0= IH0= 0, V(IOx)= 3VVB			400	600	800	μА
203	lpd()	Pull-down Current Source (2mA)	IOx with input function, IL1= IH1= 1, IL0= IH0= 1, V(IOx)= 3VVB			1.4	2.0	2.7	mA
204	lpu()	Pull-up Current Source (200μA)	IOx with output function and IOx= off, IL0, IH0= 1; V(IOx)= -7VVB-2V			120	200	280	μА
205	tp()lon	Current Source Enable Time (pull-down and pull-up sources)	write cycle, WRN: lo→hi til I(IOx) > 90% lpd(IOx) or I(IOx) > 90% lpu(IOx)					5	μs
206	tp()loff	Current Source Disable Time (pull-down and pull-up sources)	write cycle, WRN: lo→hi til I(IOx) < 10% lpd(IOx) or I(IOx) < 10% lpu(IOx)					5	μs
207	llk()	Leakage Current	IOx with input function or output function with IOx= off and IL1, IH1, IL0, IH0= 0; V(IOx)= -7VVB			-20		20	μА
208	llk()	Leakage Current	logic see item 204; V(IOx)= -10V7V			-100		20	μА
209	llk()	Leakage Current	logic see item 204; V(IOx)= VBVB+0.4V			-20		100	μА
210	llk()	Leakage Current	logic see item 204; V(IOx)= VB30V				200	500	μА
211	llk()	Leakage Current	no supply voltage VB					5	mA
/0 S	tages: Coi	mparator IO07							
301	Vin()	Permissible Input Voltage referenced to VB	V(VB)= 025.2V, (see also max. rating G003)					25.2	V
302	Vt()hi	Threshold Voltage hi	IOx with input function					4.5	V
303	Vt()lo	Threshold Voltage lo	IOx with input function			3.0			V
304	Vt()hys	Hysteresis	IOx with input function, Vt()hys= Vt()hi -Vt()lo			100			m۷
305	Vt()hi	Threshold Voltage hi referenced to VB	IOx with output function, Vt()hi= VB -V(IOx)			5.0			V
306	Vt()Io	Threshold Voltage lo referenced to VB	IOx with output function, Vt()Io= VB -V(IOx)					6.7	V
307	Vt()hys	Hysteresis	IOx with output function, Vt()hys= Vt()lo -Vt()hi			100			mV
308	tp(IOx -Dx)	Propagation Delay Input IOx to Data Output Dx	I/O filter inactive, CSN= lo, RDN= lo, A04= lo					10	μs

μΡ INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= $5V \pm 10\%$, VB= $24V \pm 5\%$, GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

tem	Symbol	Parameter	Conditions	Tj	Fig.		ı		Unit
				°C		Min.	Тур.	Max.	
Ther	nal Shutdo	own							
401	Toff1	Over-Temperature Threshold Level 1: warning				105		130	°C
402	Toff1	Level 1 Release				100		125	°C
403	Thys1	Level 1 Hysteresis	Thys1= Ton1 -Toff1			2		7	°C
404	Toff2	Over-Temperature Threshold Level 2: shutdown				130		155	°C
405	Ton2	Level 2 Release				100		125	°C
406	Thys2	Level 2 Hysteresis	Thys2= Toff2 -Ton2			22		37	°C
407	ΔΤ	Temperatur Difference Level 2 to Level 1	$\Delta T = Toff2 - Toff1$			20		30	°C
Bias	and Low V	oltage Detection							
501	VCCAon	Turn-on Threshold VCCA (Power-on release)				3.9	4.1	4.4	V
502	VCCAoff	Undervoltage Threshold VCCA (Power-down reset)				3.8	4.0	4.3	V
503	VCCAhys	Hysteresis	VCCAhys= VCCAon -VCCAoff			80	100	130	mV
504	toff	Power Down Time required for low voltage detection	VCCA= 2.5VVCCAoff			1			μs
505	tdoff	Propagation Delay until Reset after Low Voltage at VCCA						12	μs
μP In	terface, I/C	Logic, Frequency Divider, Inter	rupt						
701	IIk(Dx)	Leakage Current in Dx	D07 with input function			-5		5	μΑ
702	li()	Input Current in Schmitt-Trigger Input CSN, WRN ,RDN, A04, RESN, CLK, BLFQ, D07	V()= 0VVCCD, D07 with input function			-1		1	μА
703	Vt()hi	Threshold Voltage hi at Schmitt-Trigger Input CSN, WRN, RDN, A04, RESN, CLK, BLFQ, D07	D07 with input function					2.2	V
704	Vt()lo	Threshold Voltage lo at Schmitt-Trigger Input CSN, WRN, RDN, A04, RESN, CLK, BLFQ, D07	D07 with input function			0.8			V
705	Vt()hys	Schmitt-Trigger Input Hysteresis CSN, WRN, RDN, A04, RESN, CLK, BLFQ, D07	Vt()hys= Vt()hi-Vt()lo; D07 with input function			300			mV
706	Vs()hi	Saturation Voltage hi at INTN	Vs()hi= VCCD -V(INTN); I(INTN)= -2mA					0.80	V
707	Vs()lo	Saturation Voltage lo at INTN	I(INTN)= 100μA I(INTN)= 2mA					0.20 0.49	V V
708	Vs()hi	Saturation Voltage hi at Dx	Vs()hi= VCCD -V(Dx); I(Dx)= -4mA					0.80	V
709	Vs()lo	Saturation Voltage lo at Dx	I(Dx)= 4mA					0.49	V

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= $5V \pm 10\%$, VB= $24V \pm 5\%$, GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

ltem	Symbol	Parameter	Conditions	Tj	Fig.				Unit
				°C		Min.	Тур.	Max.	
μP In	terface, I/0	D Logic, Frequency Divider, Inter	rupt (cont'd)						
710	Vc()hi	ESD Clamp Voltage hi at CSN, WRN, RDN, A04, RESN, CLK, BLFQ, D07, INTN	Vc()hi= V() -VCCD; D07 with input function, I()= 20mA			0.4		1.5	V
711	Vc()lo	ESD Clamp Voltage lo at CSN, WRN, RDN, A04, RESN, CLK, BLFQ, D07, INTN	D07 with input function, I()= -20mA			-1.5		-0.4	V
Input	POE								
F01	Vt()hi	Threshold Voltage hi						2.2	V
F02	Vt()lo	Threshold Voltage lo				0.8			V
F03	Vt()hys	Hysteresis	Vt()hys= Vt()hi -t()lo			300			mV
F04	Rpd()	Pull-Down Resistor				24		72	kΩ
F05	tw()lo	Disable/Enable Pulse Width				600			ns
F06	tsup()	Permissible Interference Pulse Width						100	ns
F07	td(POE- IOx)	Power Output Switch-off Delay	POE: hi \rightarrow lo until IOx disabled, ie. V(IOx)< 80% (VB -Vs(IOx)hi), RL= 240 Ω 1k Ω					5	μs
F08	Vc()hi	ESD Clamp Voltage hi	Vc()hi= V(POE) -VCCA; I(POE)= 20mA			0.4		1.5	V
F09	Vc()lo	ESD Clamp Spannung Io	I(POE)= -20mA			-1.5		-0.4	V
Switc	hing Char	acteristics							
801	td()	Permissible Cycle Duration at CLK				800			ns
802	tw()	Permis. Pulse Width lo at CLK				400			ns
803	td()	Permissible Cycle Duration at BLFQ				100			ms
804	tw()	Permis. Pulse Width lo at BLFQ				50			ms

ELECTRICAL CHARACTERISTICS: WAVEFORMS

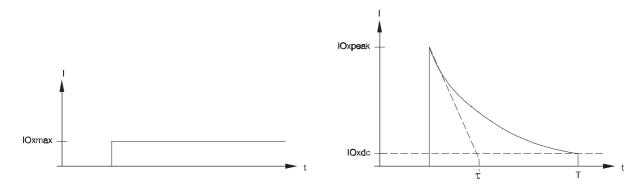


Fig. 1: DC load Fig. 2: Pulse load, pulse duration 2ms

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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OPERATING REQUIREMENTS: µP INTERFACE

Operating Cconditions: VCCD, VCCA= 5V \pm 10%, VB= 24V \pm 5%, GNDA= GNDD= PGND= 0V, Ta= 0..70°C, CL()= 150pF, input levels lo= 0.45V, hi= 2.4V, see Fig. 3 for reference levels

ltem	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
Data	Word Rea	nd Timing					
l1	tAR1 tAR2	Setup Time: CSN, A04 set before RDN hi→lo		4	30		ns
12	tra	Hold Time: CSN, A04 stable after RDN lo→hi		4	10		ns
13	tRD	Read Data Access Time: data valid after RDN hi→lo		4		120	ns
14	tDF	Read Data Hold Time: ports high impedance after RDN lo→hi		4		65	ns
15	tRL	Required Read Signal Duration at RDN			50		ns
Data	Word Wri	te Timing					
16	tAW1 tAW2	Setup Time: CSN, A04 set before WRN hi→lo		4	30		ns
17	tDW	Write Data Setup Time: data valid before WRN lo→hi		4	100		ns
18	tWA	Hold Time: CSN, A04 stable after WRN lo→hi		4	10		ns
19	twD	Write Data Hold Time: data valid after WRN lo→hi		4	10		ns
I10	tWL	Required Write Signal Duration at WRN		4	50		ns
Read	d/Write Tin	ning	1				
I11	tcyc	Recovery Time between cycles: RDN lo→hi to RDN hi→lo, RDN lo→hi to WRN hi→lo, WRN lo→hi to WDN hi→lo, WRN lo→hi to RDN hi→lo		4	165		ns

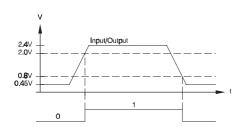


Fig. 3: Reference levels

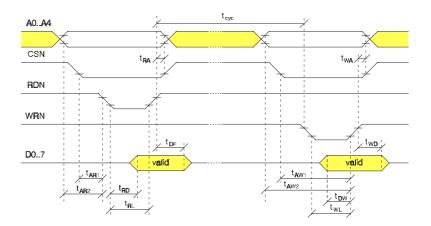


Fig. 4: Data word read/write timing

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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DESCRIPTION OF FUNCTIONS

iC-JRX is a bidirectional device which can analyze signals at the I/O pins and drive loads connected to ground. The input and output modes can be set in blocks of 4 bits (using nibbles).

I/O stages in input mode pass on the external signal via digital filtering which can be switched off as required by way of a bypass. Changes of level at any one input can generate an interrupt at the INTN port – providing that messaging is enabled. Individually programmable low-side current sources are available for each pin, enabling logic levels for the inputs to be defined (ranges $200\mu A$, $600\mu A$ and 2mA).

I/O stages in output mode can switch currents of up to 500mA. A $200\mu A$ high-side current source can be activated to check the load for any interruptions. A PWM function and a flash mode for indicator lamps are integrated in the device, both of which can be selected for any chosen output pin. If overcurrent is determined at any of the outputs, caused for example by a short-circuit, this can be reported as an interrupt if suitably enabled. If the device exceeds normal operating temperature, an interrupt gives a temperature warning; if, following this, the device continues to overheat, the outputs are shutdown.

I/O stages in input mode

Input register (add. 0): reads the inputs

A hi level at IOx generates a hi signal at Dx. Any change to an input signal is accepted via digital filtering only after the chosen filter time has ended. Doing this, the input comparator of each I/O stage switches the count direction of a 3-bit counter. The counter output changes only when the final status is reached. The counters are reset to a value of 3 by a lo signal at the RESN reset input. The counter is clocked externally via the CLK pin.

The scaling factor for the clock frequency and the input filter bypass can be programmed separately for both nibbles (the bypass with BYPH or BYPL in control word 1). Switching the bypass permits operation without an external clock signal (see below).

After the change-of-input message has been enabled (add. 8) a change of level at one of the I/O pins is signaled via an interrupt to the microcontroller.

I/O stages in output mode

Input register (add. 0): reads the output feedback

A hi level at IOx generates a hi signal at Dx. Through this, the microcontroller can make a direct check of the switching state and, in conjunction with the $200\mu A$ high-side current source, can monitor the channel for any cable fractures. As with the input read, the read-back signals can be reprocessed in their filtered or unfiltered state.

Output register (add. 6): switches the various output stages on and off (for POE= 1)

Flash pulse enable (add. 7): enables flash mode

With this, each of the various output stages can be set to flash mode, providing the value of the corresponding output register is '1'. The flash frequency is derived from BLFQ or, alternatively, can be generated from CLK (via NOBLFQ in control word 3). Different flash frequencies can be set for both nibbles (ports 0..3 and 4..7).

PWM enable (add. 14)

A PWM signal for any chosen output stage can be activated with the aid of PWMEN in control word 5. The I/O stage is selected using PWMADR2..0. PWMPN determines the direction of the PWM signal (active hi or active lo). The shape of the PWM signal is given by the value of the PWM register (add. 15), multiplied by 16xtd(CLK).

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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Interrupts

Interrupt outputs at INTN can be triggered by a change of (filtered) input signal, by overcurrent, signaled at an I/O pin (e.g. due to a short circuit), or by exceeding maximum temperature levels (2 stages).

For each individual I/O stage, interrupt outputs can be caused by a change of input, or, with stages in output mode, also by a short circuit. The relevant interrupt enables determine which messages are stored and displayed. The display of interrupt messages caused by excessive temperature is not maskable; it is permanently enabled.

When an event occurs which is enabled to produce an interrupt output, pin INTN is set to '0'. An interrupt status register read-out (add. 2) enables the nature of the message to be determined and the I/O stage causing the interrupt to be located. Thus with a change-of-input message the initiating I/O stage is shown in the corresponding register (add. 1); with an overcurrent interrupt, the overcurrent message register (add. 3) pinpoints the I/O stage with a short circuit.

Interrupts are deleted by simply setting EOI in control word 4. This bit then automatically resets to '0'. If during operation the I/O mode is switched, i.e. from input to output mode, all interrupt messages are deleted via EOI.

To avoid interrupt messages caused by other sources in the time between the read-out of an interrupt register and the deletion of the current interrupt being overlooked, successive interrupts are stored in a pipeline. In the event of there being any successive interrupts, output INTN remains at '0' after the current interrupt has been deleted using EOI. The new interrupt source is shown in the interrupt status register and in the type-specific status registers.

Overcurrent messages

With an overload at one of the outputs the current in IOx is limited. In this instance an interrupt message is displayed, providing relevant interrupt enables have been set for overcurrent messages (add. 9) and the filter time set with control word 4 has elapsed. If this happens, ISCI is set in the interrupt status register (add. 2) and the relevant bit is set for the initiating I/O stage in the overcurrent message register (add. 3).

Under address 4 the current, unfiltered overcurrent status of each I/O stage can be read; an overall scan of all the I/O stages is also possible via bit SCS of the interrupt status register. This shows whether any of the I/O stages have overcurrent at the time of the readout. This short-circuit messaging allows permanent monitoring of the output transistors and clear allocation of the error message to the I/O stage affected.

Filtering of the overcurrent message can be shutdown via a bypass; this bypass can be activated for all I/O stages together using BYPSCF in control word 4 (add. 13).

Temperature monitoring

iC-JRX has a two-stage temperature monitor circuit.

Stage 1: A warning interrupt (INTN= 0) is generated if the first temperature level (Toff 1 at ca. 125°C)

is exceeded. Suitable measures to decrease the power dissipation of the driver can be

implemented via the microcontroller.

Stage 2: If the second temperature level is exceeded (Toff 2 at ca. 150°C), a second interrupt is

generated (INTN= 0). At the same time the output transistors and the I/O stage current

sources are shutdown, the output register and flash mode enable deleted.

Once the temperature level has returned to below that of Toff1 the current sources are reactivated. The output register and flash pulse enable have to be respecified to activate the

output stages.

The interrupt status register (add. 2) gives information as to the stage of temperature interrupt but also on the current status of the temperature monitor. ET2 and ET1 statically indicate when Toff2 and Toff1 are exceeded, whereby the stored interrupt messages IET2 and IET1 and the display at INTN via EOI= 1 can be deleted (control word 4).

μP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS



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Low voltage detection

When the supply voltage at VCC is switched on, the output transistors are only released by the low voltage detector after the power-on enable VCCon has been reached. Should the supply voltage drop to VCCoff during operation, the I/O stages are disabled, i.e. the output transistors are turned off and the device reset (signal VOK). If the supply voltage should then rise to VCCon, iC-JRX is in its reset state.

Identification of the device

An identification code has been introduced to enable identification of device iC-JRX. Bit pattern '000000'b can be read out under address 5.

Reset

A reset (RESN= 0) sets the register entries to the reset values given in the tables. The output transistors and the current sources in the I/O stages are shutdown and all stages switched to input mode.

Operation without the BLFQ signal

Should no clock signal be available at pin BLFQ, iC-JRX can generate the flash pulse internally from the clock signal at pin CLK. To this end, NOBLFQ in control word 3 must be set to '1'. The flash period is then calculated from the clocking pulse at CLK by division by 2¹⁹.

Operation without the CLK signal

iC-JRX is operable without a clocking pulse at the CLK pin. With NOCLK in control word 3 the clocked filtering for the I/O signals and overcurrent messaging is deactivated. The device remains fully functional with one exception; the PWM cannot be activated, as this is dependent on CLK.

The same behavior can be obtained by setting BYPH and BYPL in control word 1 together with BYPSCF in control word 4; all filters are avoided by way of a bypass circuit. This has one disadvantage, namely that interferences in the load lines, for example, can lead to the unwanted display of interrupts.

Forced shutdown of output stages

The output stages can be forcibly shutdown at input POE. A '1' enables logic access to the drivers; an '0' disables this. With this, a processor-independent watchdog can lock the outputs in the event of error, for example. An integrated pull-down resistor increases safety.

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Pulse-width modulation

This function can be activated for any chosen I/O stage in output mode.

First the duty cycle is determined via the PWM register in 256 steps within one PWM period. Pulse direction and the address for the desired driver stage is selected via control word 5 (PWMPN, PWMADR2..0).

The PWM enable bit can now also be set via control word 5. With this enable, the current source and any active flash mode for the selected output are automatically switched off.

The set duty cycle is activated when a new PWM period is started.

A PWM signal is set at the selected output, whose frequency is determined by the clock signal at CLK and whose duty cycle follows the PWM register.

The following correlations apply:

$$f_{PWM} = \frac{f_{CLK}}{4096} \; ; \qquad \Delta t_{PWM} = \frac{1}{f_{PWM} \times 256} \; ; \qquad$$

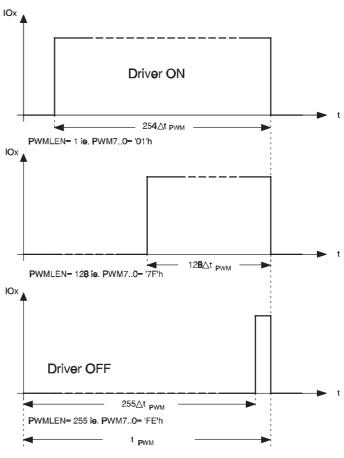


Fig. 5: PWM signal form

$$t_{PWMIo}$$
 = (PWMLEN +1) $\times \Delta t_{PWM}$

f_{CLK} : Clock frequency CLK

 f_{PWM} : Frequency for the PWM signal at IOx

 $\Delta t_{\mbox{\tiny PWM}}$: Smallest possible pulse duration 'lo' (8 μ s with a 2MHz clock)

t_{PWMIo} : Pulse duration 'lo' (IOx= OFF with PWMPN= 1)

PWMLEN: Count for pulse duration 'lo' stored in register PWM7..0

Selectable Pulse	Selectable Pulse-Pause Ratios								
PWM70	PWMPN	Output signal							
1001-	0	Output stage "ON", Pin IOx= '1' (reset entry)							
'00'h	1	Output stage "OFF", Pin IOx= '0'							
10411 15511	0	Output pin IOx goes for (PWMLEN + 1) \times Δt_{PWM} to '0', and then for (255 - PWMLEN) \times Δt_{PWM} to '1'							
'01'h 'FE'h	1	Output pin IOx goes for (PWMLEN + 1) \times Δt_{PWM} to '1', and then for (255 - PWMLEN) \times Δt_{PWM} to '0'							
,CC,F	0	Output stage "OFF", Pin IOx= '0'							
'FF'h	1	Output stage "ON", Pin IOx= '1'							

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Rev A0, 23/23

ORDERING INFORMATION

Туре	Package	Order designation
iC-JRX	PLCC44	iC-JRX-PLCC44

For information about prices, terms of delivery, options for other case types, etc., please contact:

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