Integrated Circuit Systems, Inc.

ICS8602

LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-LVCMOS ZERO DELAY BUFFER

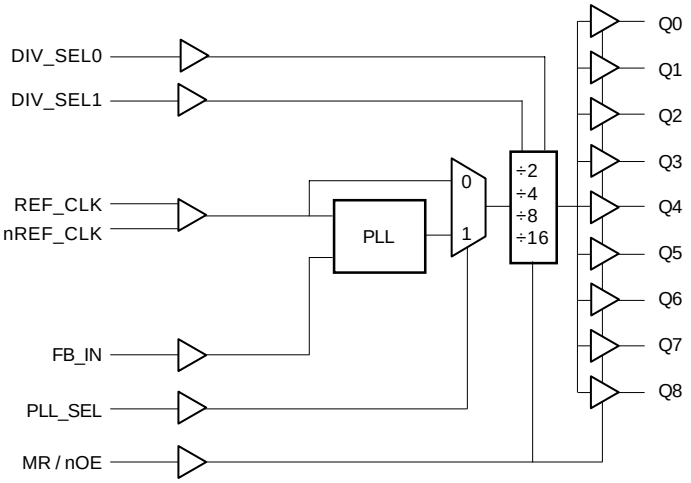
GENERAL DESCRIPTION

The ICS8602 is a high performance LVCMOS zero delay buffer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The VCO operates at a frequency range of 250MHz to 450MHz. Utilizing one of the outputs as feedback to the PLL output frequencies up to 225MHz can be regenerated with zero delay with respect to the input. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fan-out can be doubled by utilizing the ability of the outputs to drive two series terminated lines. The differential reference clock input will accept any differential signal levels.

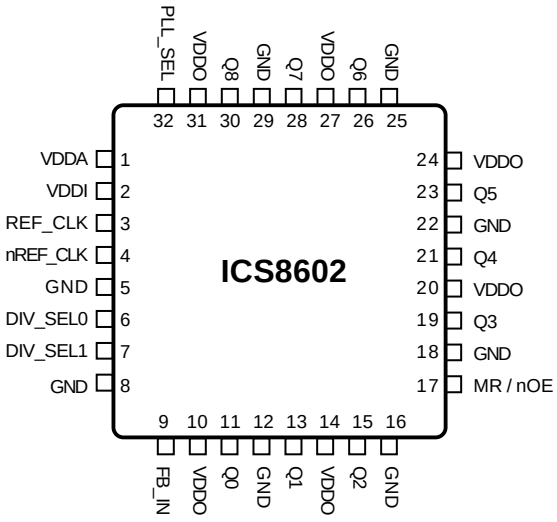
FEATURES

- Fully integrated PLL
- 9 LVCMOS outputs
- 15.625MHz to 225MHz output frequency range
- Spread Smart™ for regenerating spread spectrum clocks
- Differential reference clock input accepts any differential signal levels
- 15.625MHz to 225MHz input frequency range
- LVCMOS / LVTTL control inputs
- 3.3V supply voltage
- 32 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VDDA	Power		PLL power supply pin. Connect to 3.3V.
2	VDDI	Power		Input and core power supply pin. Connect to 3.3V.
3	REF_CLK	Input	Pulldown	Non-inverting differential clock input.
4	nREF_CLK	Input	Pullup	Inverting differential clock input.
5, 8, 12 16, 18, 22, 25, 29	GND	Power		Ground pins. Connect to ground.
6, 7	DIV_SEL0, DIV_SEL1	Input	Pulldown	Determines output divider valued in Table 3. LVCMOS / LVTTL interface levels.
9	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay" LVCMOS / LVTTL interface levels.
10, 14, 20, 24, 27, 31	VDDO	Power		Output power supply pins. Connect to 3.3V.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Output		Clock outputs. 7Ω typical output impedance. LVCMOS interface levels.
17	MR/nOE	Input	Pulldown	Resets dividers and determine state of the outputs. LVCMOS / LVTTL interface levels.
32	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH select PLL. When LOW selects reference clock. LVCMOS / LVTTL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	REF_CLK, nREF_CLK			TBD		pF
		DIV_SEL0, DIV_SEL1, PLL_SEL, MR/nOE					
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ
CPD	Power Dissipation Capacitance (per output)		VDDA, VDDI, VDDO = 3.47V		TBD		pF
			VDDA, VDDI = 3.47V, VDDO = 2.63V		TBD		pF
ROUT	Output Impedance				7		Ω

TABLE 3. CONTROL INPUTS FUNCTION TABLE

DIV_SEL1	DIV_SEL0	DIVIDE VALUE	INPUT/OUTPUT FREQUENCY (MHz)	
			MIN	MAX
0	0	2	125	225
0	1	4	62.5	125
1	0	8	31.25	62.5
1	1	16	15.625	31.25

TABLE 4. PLL INPUT REFERENCE CHARACTERISTICS, VDDI=VDDA=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fREF	Input Reference Frequency		20		225	MHz
tR	Input Rise Time	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	Measured at 20% to 80% point			TBD	ns
tDC	Input Reference Duty Cycle		TBD		TBD	%

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDD	Input Power Supply Current					mA

TABLE 5B. DIFFERENTIAL DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	REF_CLK	VIN = 3.465V			150	µA
		nREF_CLK	VIN = 3.465V			1	µA
IIL	Input Low Current	REF_CLK	VIN = 0V	-1			µA
		nREF_CLK	VIN = 0V	-150			µA
VPP	Peak-to-Peak Input Voltage		f = 225MHz				
VCMR	Common Mode Input Voltage		f = 225MHz				

NOTE 1: The inputs are designed to accept single ended signal level with a resistor bias on one of the differential inputs. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and using the nREF_CLK input connect a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The REF_CLK input will now switch against the VDDI/2 threshold set by the resistor network.

TABLE 5C. LVCMOS / LVTTL DC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SEL0, DIV_SEL1, FB_IN, PLL_SEL MR/nOE		2		3.765	V
VIL	Input Low Voltage	DIV_SEL0, DIV_SEL1, FB_IN, PLL_SEL MR/nOE		-0.3		0.8	V
IIH	Input High Current	DIV_SEL0, DIV_SEL1, FB_IN, MR/nOE	VIN = 3.465V			150	µA
		PLL_SEL	VIN = 3.465V			5	µA
IIL	Input Low Current	DIV_SEL0, DIV_SEL1, FB_IN, MR/nOE	VIN = 0V	-5			µA
		PLL_SEL	VIN = 0V	-150			µA
VOH	Output High Voltage		VDDO = 3.135V IOH = -36mA	2.6			V
VOL	Output Low Voltage		VDDO -3.135V IOL = 36mA			0.5	V

TABLE 6. AC CHARACTERISTICS, VDDI=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Output Frequency					225	MHz
tpLH	Propagation Delay, Low-to-High		PLL_SEL=0V, 0MHz ≤ f ≤ 225MHz	TBD		TBD	ns
tpHL	Propagation Delay, High-to-Low		PLL_SEL=0V, 0MHz ≤ f ≤ 225MHz	TBD		TBD	ns
t(Ø)	PLL Reference Zero Delay; NOTE 2	REF_CLK, nREF_CLK	PLL_SEL = 3.3V, fREF = 133MHz, fVCO = 133MHz	-170	TBD	+120	ps
			PLL_SEL = 3.3V, fREF = 50MHz, fVCO = 50MHz	-220		+115	ps
tsk(o)	Output Skew; NOTE 3		Measured on rising edge at VDDO/2			125	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4		Measured on rising edge at VDDO/2		50		ps
tL	PLL Lock Time					TBD	ps
tR	Output Rise Time			TBD		TBD	ps
tF	Output Fall Time			TBD		TBD	ps
tPW	Output Pulse Width		0MHz ≤ f ≤ 225MHz	tCYCLE/2 -TBD	tCYCLE/2	tCYCLE/2 +TBD	ns
			f = 225MHz	TBD	2.08	TBD	ns
tEN	Output Enable Time					TBD	ns
tDIS	Output Disable Time					TBD	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent pairs of cycles.

PACKAGE OUTLINE - Y SUFFIX

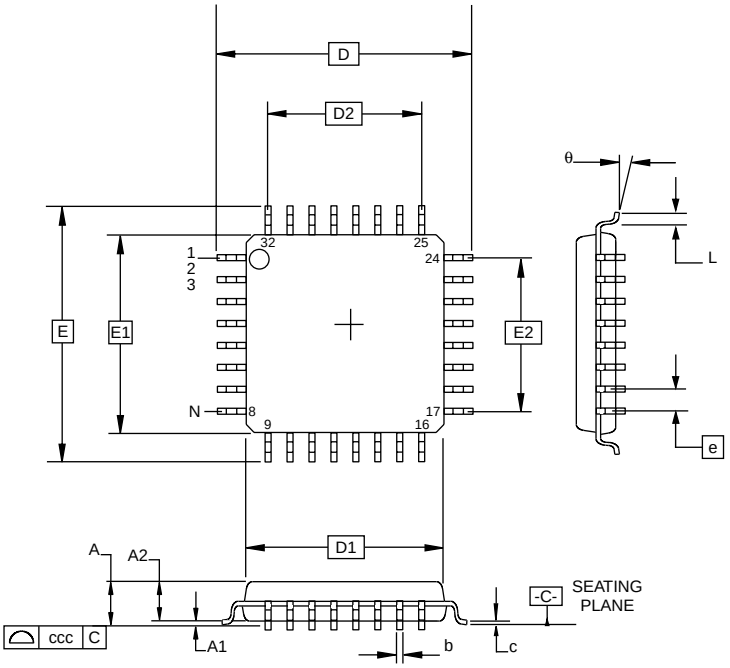


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8602AY	ICS8602AY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8602AYT	ICS8602AY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C