ICS377
Quad PLL with VCXO
Quick Turn Clock Synthesizer

Description

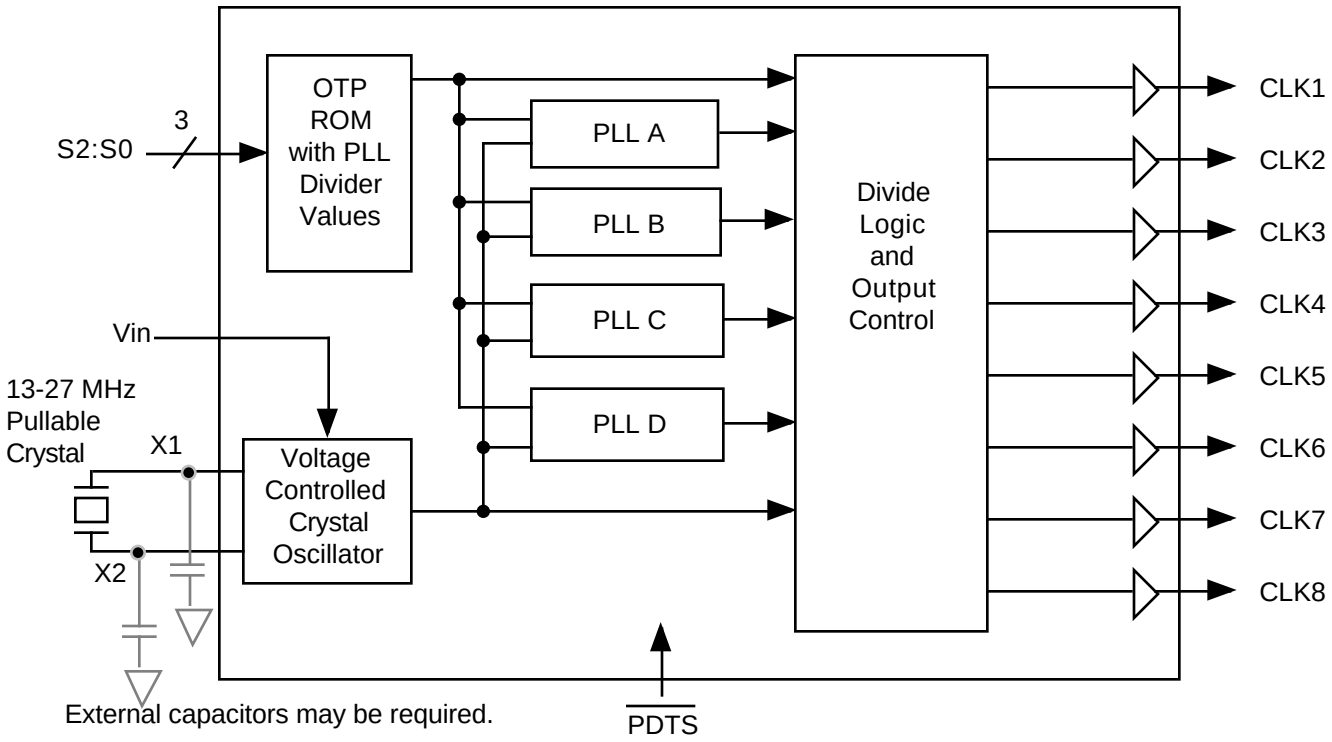
The ICS377 QTClock™ generates up to 8 high quality, high frequency clock outputs. It is designed to replace a VCXO, crystals, and crystal oscillators in most electronic systems. The ICS377 contains a One Time Programmable (OTP) ROM, factory programmed with PLL divider values to output a broad range of frequencies (up to 200 MHz). Quick Turn factory programming allows customer sample requests to be shipped in 1-3 days. Programming features include a selectable frequency table and two banks of up to 4 low-skew outputs.

Using ICS' patented VCXO and Phase-Locked-Loop (PLL) techniques, the device runs from a pullable crystal. It can replace a VCXO and multiple crystals and oscillators, saving board space and cost.

Features

- Packaged in 28 pin SSOP (QSOP)
- Quick turn frequency programming allows samples as quickly as one day
- Two banks, up to 4 outputs each, can be low-skew
- Can include 8 selectable output frequencies
- Up to 4 reference outputs
- Replaces a VCXO plus multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3 V
- Input crystal frequency of 13 - 27 MHz
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



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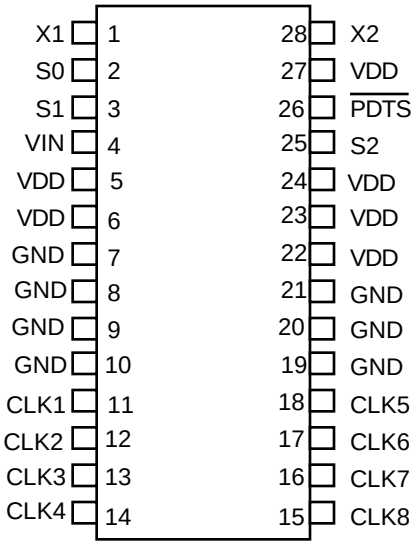
Pin Assignments



28 pin (150 mil) SSOP (QSOP)

Pin Descriptions

Number	Name	Type	Description
1	X1	XI	Crystal connection. Connect to fundamental mode pullable crystal.
2	S0	I	Select pin 0 for frequency table/chip control. Internal pull-up resistor.
3	S1	I	Select pin 1 for frequency table/chip control. Internal pull-up resistor.
4	VIN	VI	VCXO Voltage input. Zero to 3.3V analog control voltage for VCXO
5, 6	VDD	P	Connect to +3.3V.
7-10	GND	P	Connect to ground.
11	CLK1	O	Clock output 1. Independent output or part of low skew bank A.
12	CLK2	O	Clock output 2. Independent output or part of low skew bank A.
13	CLK3	O	Clock output 3. Independent output or part of low skew bank A.
14	CLK4	O	Clock output 4. Independent output or part of low skew bank A.
15	CLK8	O	Clock output 8. Independent output or part of low skew bank B.
16	CLK7	O	Clock output 7. Independent output or part of low skew bank B.
17	CLK6	O	Clock output 6. Independent output or part of low skew bank B.
18	CLK5	O	Clock output 5. Independent output or part of low skew bank B.
19-21	GND	P	Connect to ground.
22-24	VDD	P	Connect to +3.3V.
25	S2	I	Select pin 2 for frequency table/chip control. Internal pull-up resistor.
26	$\overline{\text{PDTS}}$	I	All-chip power down when low. See Note 1.
27	VDD	P	Connect to +3.3V.
28	X2	XO	Crystal connection. Connect to fundamental mode pullable crystal.

Key: XI, XO = crystal connections, I = Input, O = output, P = power supply connection
Note 1: All outputs are internally high impedance with a weak internal pull-down resistor. When $\overline{\text{PDTS}}$ is active, it is possible to overdrive the output pins for board-level testing.

Device Configuration

The ICS377 QTClock provides the facility for up to 8 clock outputs. The outputs are derived from either the reference input or from one of the 4 PLLs. All chip functions are controlled from an OTP ROM which has 3 input control lines (S2, S1, S0), giving a total of 8 address locations. Each address location gives control of the following:

1) Each output can be turned off individually.
2) The internal dividers for each PLL are controlled to generate any required frequency.
3) Each PLL can be turned off (powered down) individually.
4) The output divide and control logic can be configured to bring the appropriate clock to the correct pin.
5) Up to four low skew copies of the same clock can be enabled.

This chip architecture provides the user with unrivaled flexibility. For example, one of the input pins could be used to control the power of the chip by shutting down PLLs and outputs when not used. A second could be used to change the output clock frequencies.

The specification is complete when the ICS377 QTClock Order Form accompanies this data sheet. The order form lists the input and CLK actual frequencies, as well as any other available options. This unique configuration is given a two character alphanumeric programming code (ICS377-xx), which must be specified when referring to samples.

Frequency Select Table

The ICS377 can be configured so that one PLL provides up to 8 frequency selections. For example, CPU frequencies of 66.7 MHz, 100.0 MHz, 133.3 MHz, and 166.7 MHz could be included. This information should be indicated on the Order Form when the ICS377 is initially defined.

External Components / Crystal Selection

The ICS377 requires five 0.01µF decoupling capacitors to be connected between VDD and GND pairs. It is recommended that these be placed between VDD and GND pairs on pin 5 and 8, pin 6 and 10, pin 22 and 19, pin 23 and 21, and pin 24 and 20. These must be connected close to the ICS377 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω series terminating resistor can be used next to each CLK pin. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel mode, pullable, AT cut, with 14 pF load capacitance. See previous page for crystal specifications. Consult ICS for recommended suppliers. IMPORTANT - read application note MAN05 before laying out the PCB.

Crystal Specifications

Correlation (load) capacitance	14 pF
Initial accuracy	±20 ppm maximum
Drift over temperature and aging	±50 ppm maximum
C0/C1 ratio	250 maximum
ESR	35 Ω maximum

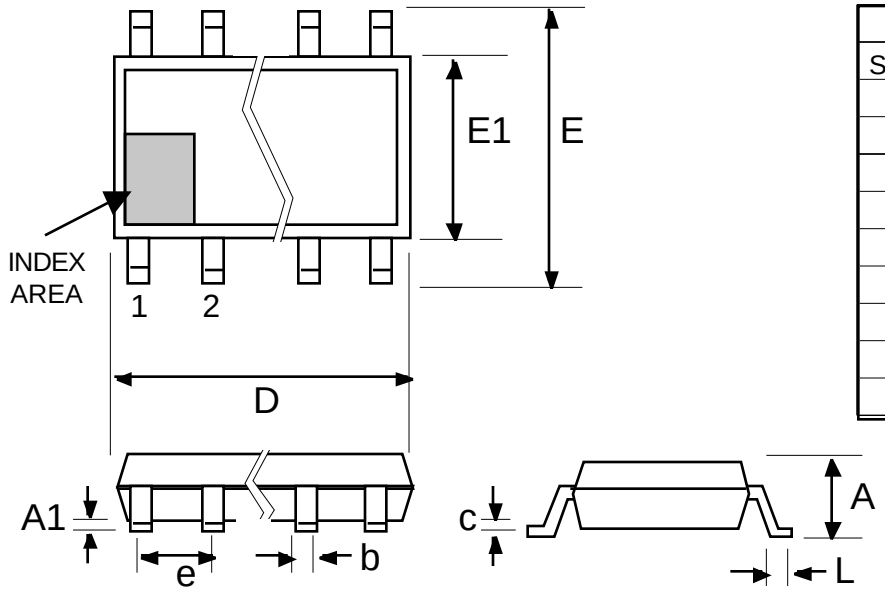
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	Commercial version	0		70	ºC
Soldering Temperature	Max of 10 seconds			260	ºC
Storage temperature		-65		150	ºC
DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Operating Voltage, VDD		3.13		3.46	V
Input High Voltage, VIH	$\overline{PDTS}$, S0, S1, S2	2			V
Input Low Voltage, VIL	$\overline{PDTS}$, S0, S1, S2			0.8	V
Output High Voltage, VOH	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
IDD Operating Supply Current			TBD		mA
Short Circuit Current	CLK output		±50		mA
On-Chip Pull-up Resistor, inputs			TBD		kΩ
On-Chip Pull-down Resistor, outputs			TBD		Ω
Input Capacitance, inputs			4		pF
AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Input Frequency, crystal input		13		27	MHz
Output Frequency		2		200	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle (Note 1)	at VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter	Deviation from mean		±TBD		ps
One Sigma Clock Period Jitter			TBD		ps
Pin to Pin Skew	Low skew outputs	-250		250	ps
Power-up time, $\overline{PDTS}$ goes high until CLKout			8	20	ms

Note 1: These are typical values. The actual minimum and maximum duty cycle limits are shown on the ICS377 QTClock Order Form for each programmed version.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
D	0.386	0.394	9.80	10.00
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27

Ordering Information

Part/Order Number	Marking	Package	Shipping	Temperature
ICS377R-xx	ICS377R-xx	28 pin SSOP	Tubes	0 to 70 °C
ICS377R-xxT	ICS377R-xx	28 pin SSOP	Tape and Reel	0 to 70 °C

xx represents a 2 character alphanumeric programming code assigned by the factory, which indicates the output frequencies on all CLKs and other features. All samples are shipped with an ICS377 order form describing the characteristics of the device.