600V, SMPS II LGC Series N-Channel IGBT with Anti-Parallel Stealth™ Diode

The ISL9H2060EG3 is a Low Gate Charge (LGC) SMPS II IGBT combining the fast switching speed of the SMPS IGBTs along with lower gate charge and avalanche capability (UIS). These LGC devices shorten delay times, and reduce the power requirement of the gate drive. These devices are ideally suited for high voltage switched mode power supply applications where low conduction loss, fast switching times and UIS capability are essential. SMPS II LGC devices have been specially designed for:

- Power Factor Correction (PFC) Circuits
- Full Bridge Topologies
- Half Bridge Topologies
- Push-Pull Circuits
- Uninterruptible Power Supplies
- Zero Voltage and Zero Current Switching Circuits

Formerly Developmental Type TA49340.

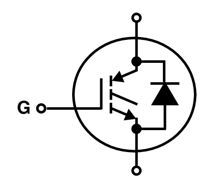
Ordering Information

PART NUMBER	PACKAGE	BRAND
ISL9H2060EG3	TO-247	H2060EG3

Features

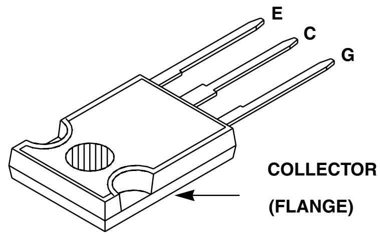
- >100kHz Operation at 390V, 20A
- 200kHz Operation at 390V, 9A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . .75ns at T_J = 125°C
- Low Gate Charge . . . . .37nC at V_{GE} = 15V
- UIS Rated 260mJ
- Low Conduction Loss

Symbol



Packaging

JEDEC STYLE TO-247



INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	75	A
At $T_C = 110^oC$	I_{C110}	35	A
Collector Current Pulsed (Note 1)	I_{CM}	180	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 2	SSOA	100A at 600V	
Single Pulse Avalanche Energy at $T_C = 25^oC$	E_{AS}	260mJ at 20A	
Power Dissipation Total at $T_C = 25^oC$	P_D	290	W
Power Dissipation Derating $T_C > 25^oC$		2.33	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Tech Brief 334	T_{PKG}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. Pulse width limited by maximum junction temperature.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = 600V$	$T_J = 25^oC$	-	-	100	µA
			$T_J = 125^oC$	-	-	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 20A$, $V_{GE} = 15V$	$T_J = 25^oC$	-	1.9	2.7	V
			$T_J = 125^oC$	-	1.7	2.0	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = 600V$		4.5	6.6	7.0	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 3\Omega$, $V_{GE} = 15V$ $L = 100\mu H$, $V_{CE} = 600V$		100	-	-	A
Pulsed Avalanche Energy	E_{AS}	$I_{CE} = 20A$, $L = 2.1mH$, $V_{DD} = 50V$		260	-	-	mJ
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = 20A$, $V_{CE} = 300V$		-	9.3	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = 20A$, $V_{CE} = 300V$	$V_{GE} = 15V$	-	37	46	nC
			$V_{GE} = 20V$	-	46	58	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^oC$ $I_{CE} = 20A$ $V_{CE} = 390V$ $V_{GE} = 15V$ $R_G = 3\Omega$ $L = 200\mu H$ Test Circuit - Figure 26		-	10	-	ns
Current Rise Time	t_{rI}			-	17	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	39	-	ns
Current Fall Time	t_{fI}			-	44	-	ns
Turn-On Energy (Note 2)	E_{ON1}			-	105	-	µJ
Turn-On Energy (Note 2)	E_{ON2}			-	200	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	210	-	µJ

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 125^oC$ $I_{CE} = 20A$ $V_{CE} = 390V$ $V_{GE} = 15V$ $R_G = 3\Omega$ $L = 200\mu H$ Test Circuit - Figure 26	-	12	-	ns
Current Rise Time	t_{rI}		-	15	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	65	100	ns
Current Fall Time	t_{fI}		-	75	85	ns
Turn-On Energy (Note 2)	E_{ON1}		-	115	-	μJ
Turn-On Energy (Note 2)	E_{ON2}		-	360	430	μJ
Turn-Off Energy (Note 3)	E_{OFF}		-	380	490	μJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 20A$	-	2.1	2.5	V
Diode Reverse Recovery	t_{rr}	$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$, $V_{CE} = 30V$	-	30	35	ns
		$I_{EC} = 20A$, $dI_{EC}/dt = 200A/\mu s$, $V_{CE} = 30V$	-	39	48	ns
Thermal Resistance Junction To Case	$R_{\theta JC}$	IGBT	-	-	0.43	$^oC/W$
		Diode	-	-	1.25	$^oC/W$

NOTES:

2. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 26.
3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves Unless Otherwise Specified

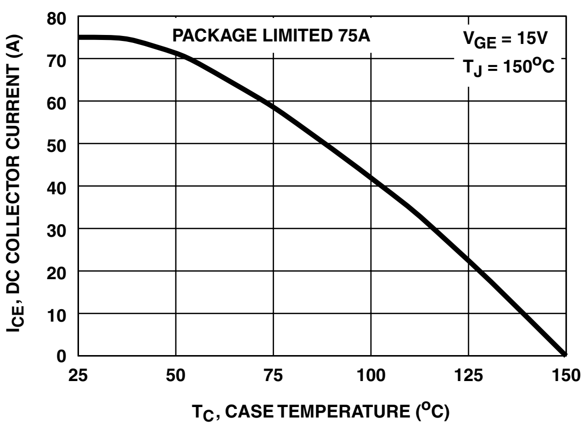


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

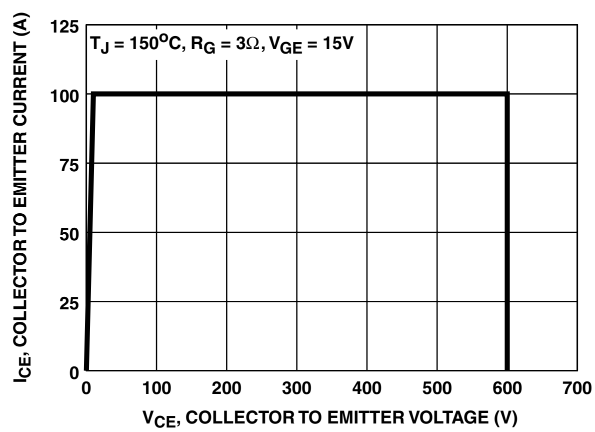


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

Typical Performance Curves Unless Otherwise Specified **(Continued)**

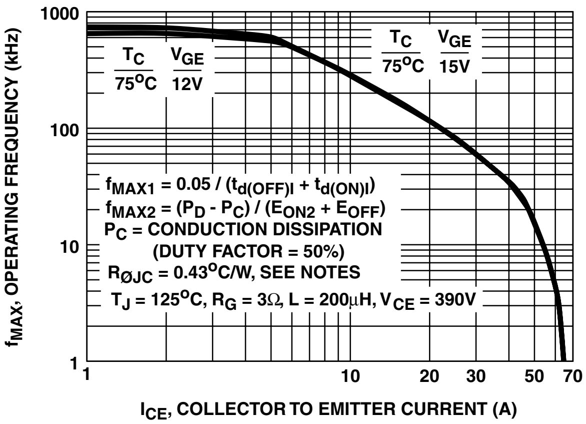


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

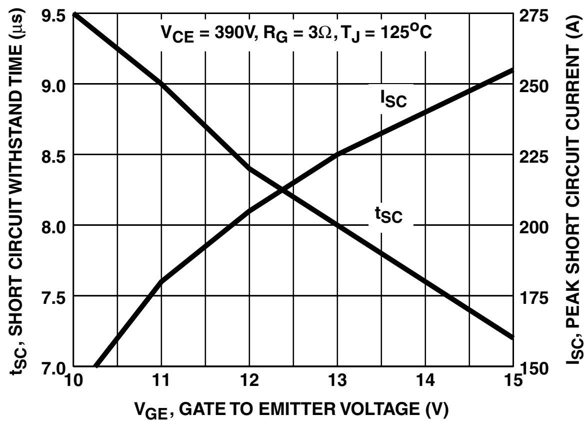


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

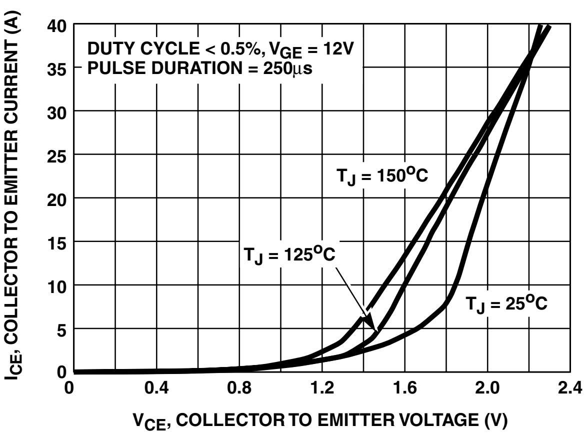


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

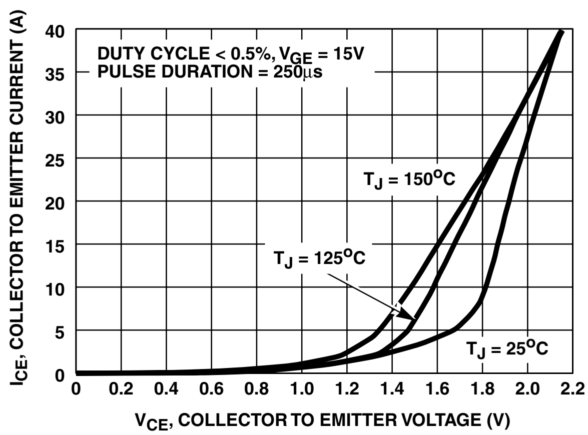


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

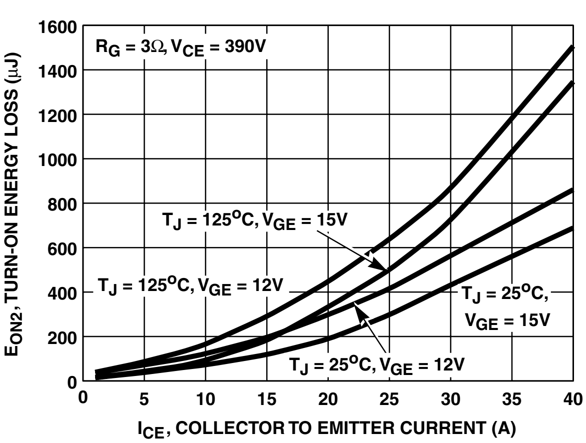


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

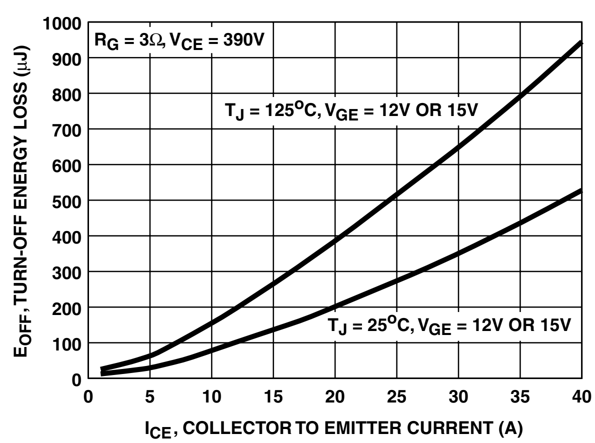


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

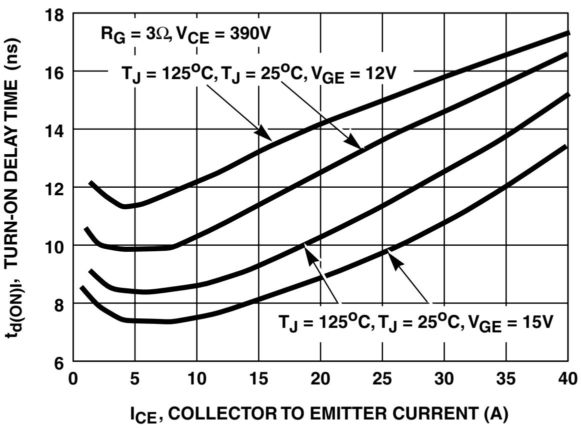


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

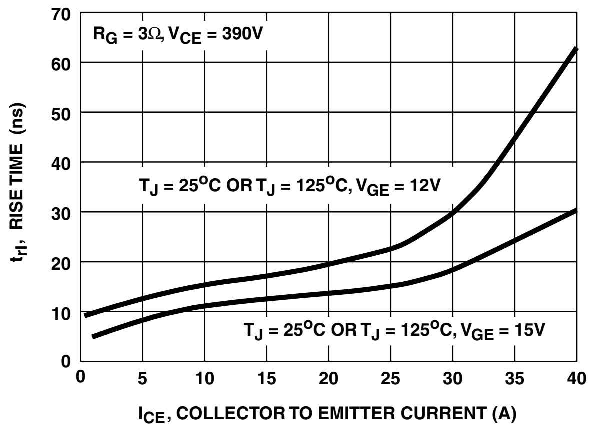


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

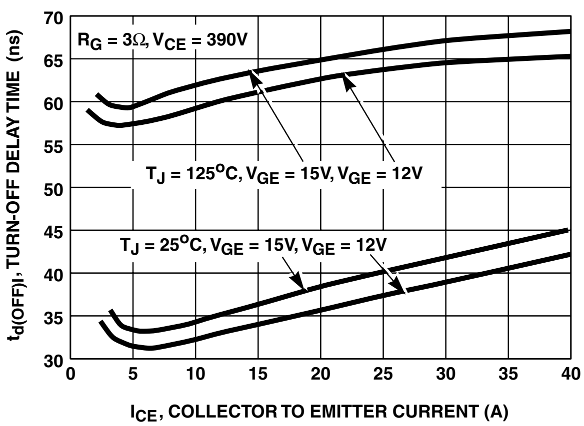


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

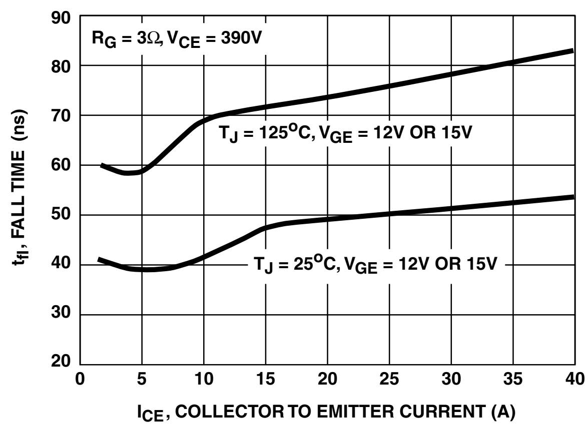


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

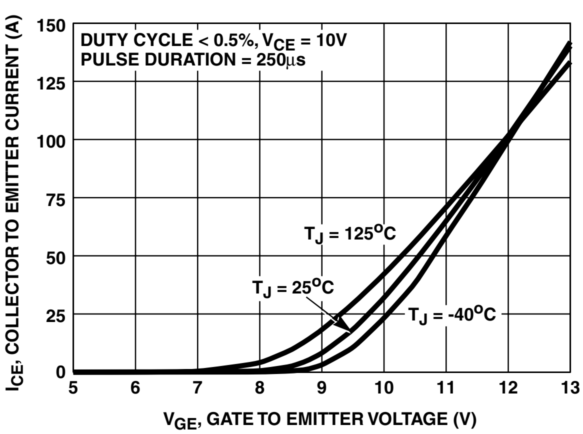


FIGURE 13. TRANSFER CHARACTERISTIC

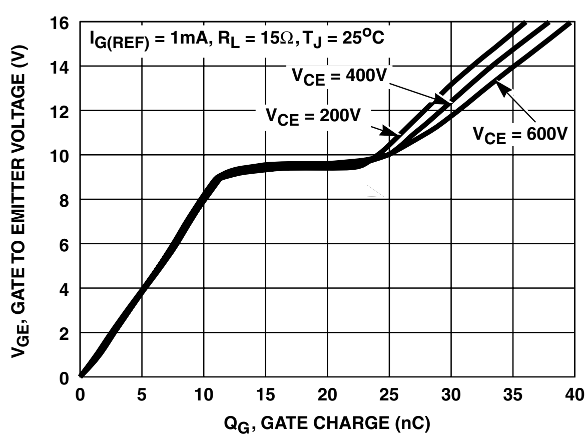


FIGURE 14. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified **(Continued)**

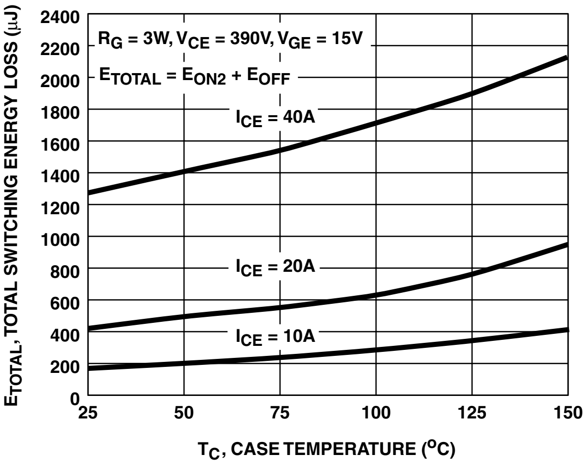


FIGURE 15. TOTAL SWITCHING LOSS vs CASE TEMPERATURE

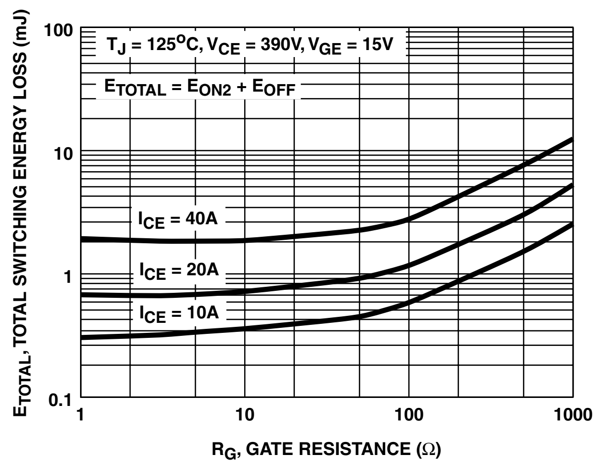


FIGURE 16. TOTAL SWITCHING LOSS vs GATE RESISTANCE

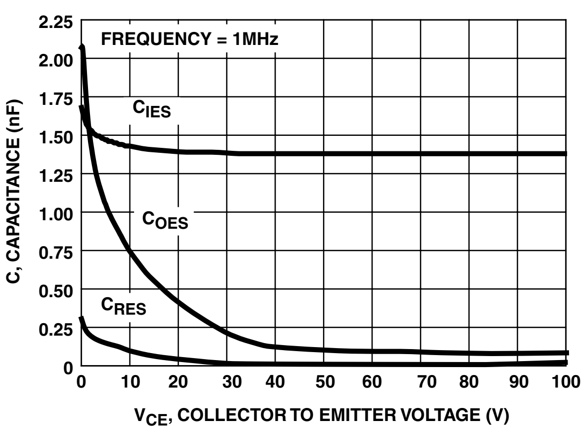


FIGURE 17. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

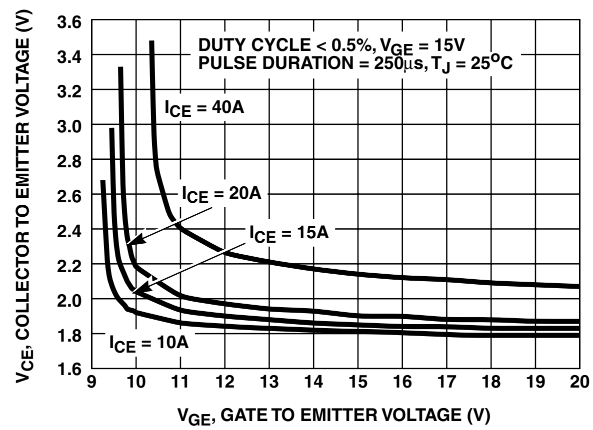


FIGURE 18. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs GATE TO EMITTER VOLTAGE

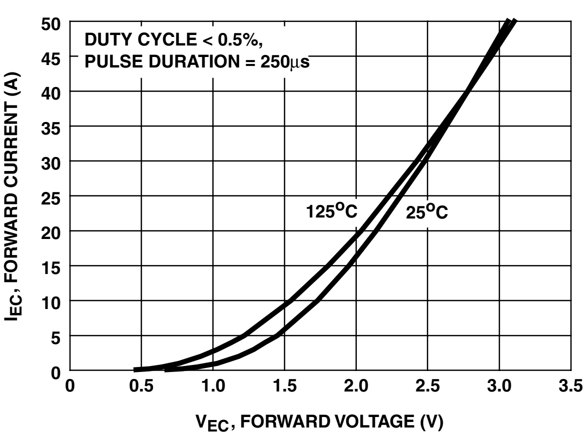


FIGURE 19. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

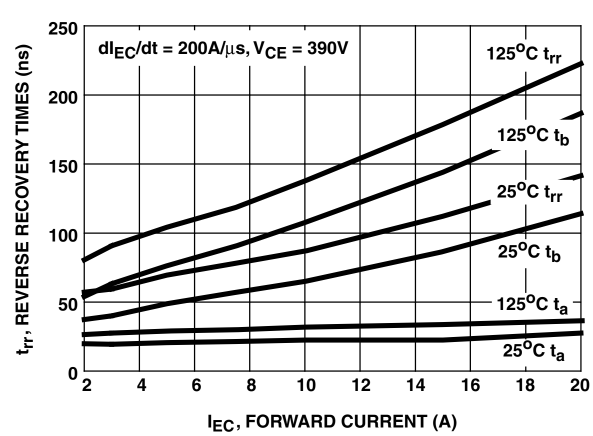


FIGURE 20. REVERSE RECOVERY TIMES vs DIODE FORWARD CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

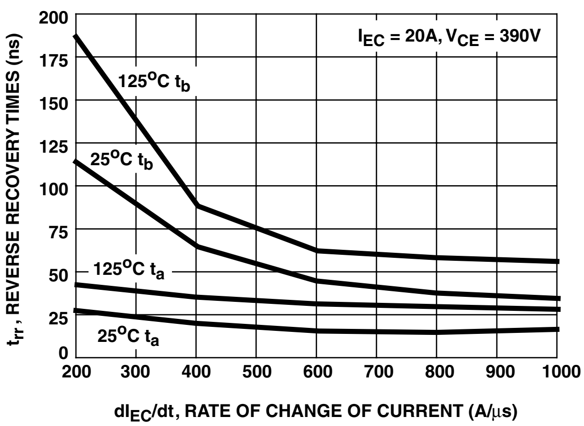


FIGURE 21. REVERSE RECOVERY TIMES vs RATE OF CHANGE OF CURRENT

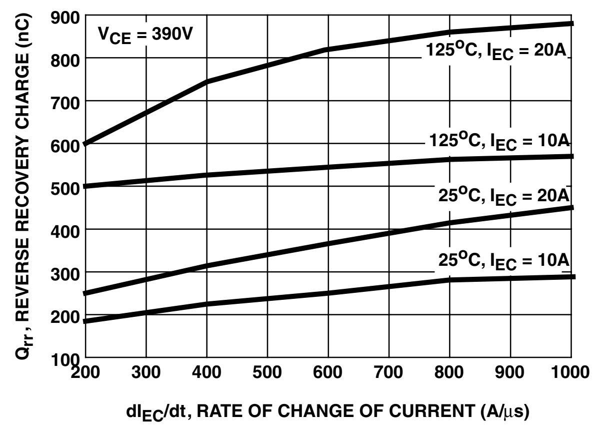


FIGURE 22. STORED CHARGE vs RATE OF CHANGE OF CURRENT

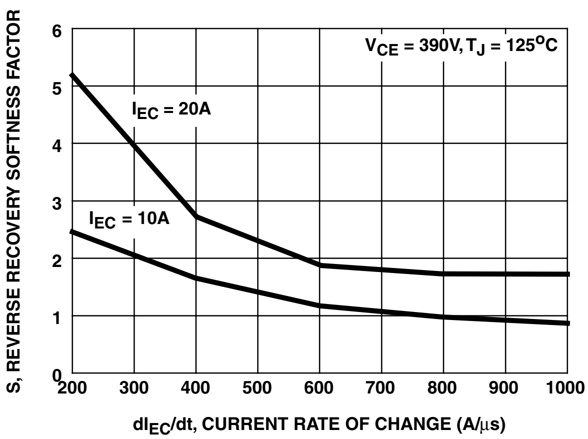


FIGURE 23. REVERSE RECOVERY SOFTNESS FACTOR vs RATE OF CHANGE OF CURRENT

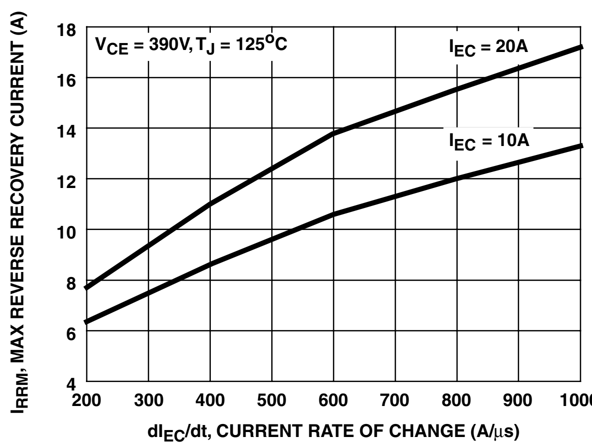


FIGURE 24. MAXIMUM REVERSE RECOVERY CURRENT vs RATE OF CHANGE OF CURRENT

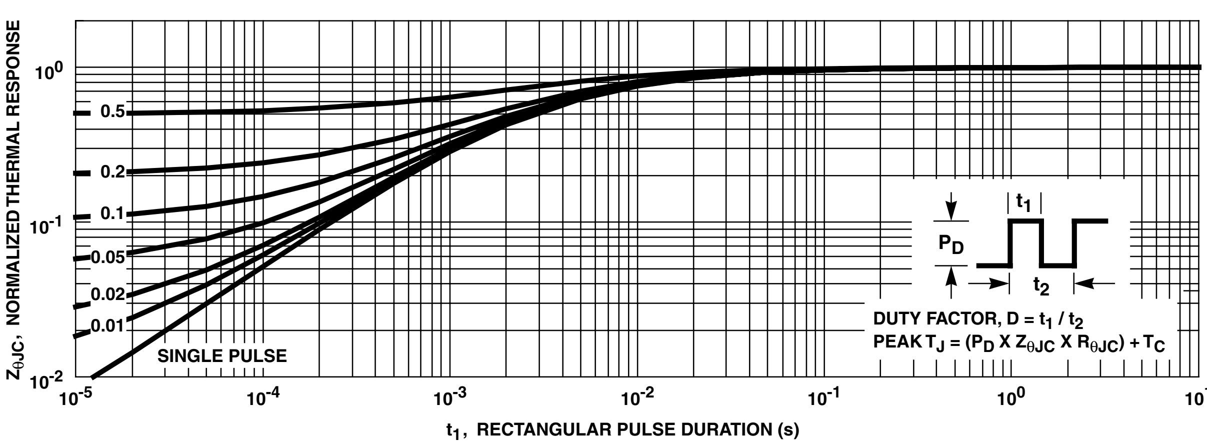


FIGURE 25. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuit and Waveforms

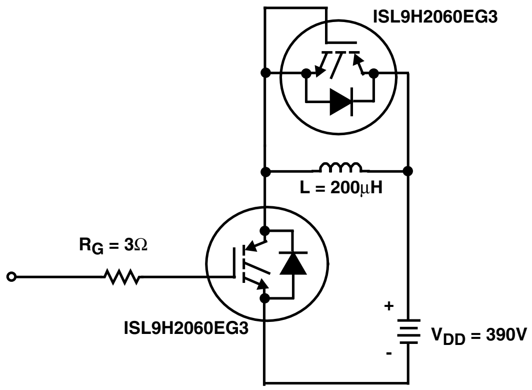


FIGURE 26. INDUCTIVE SWITCHING TEST CIRCUIT

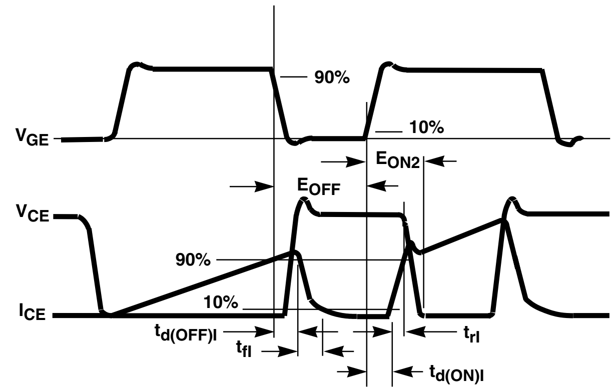


FIGURE 27. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

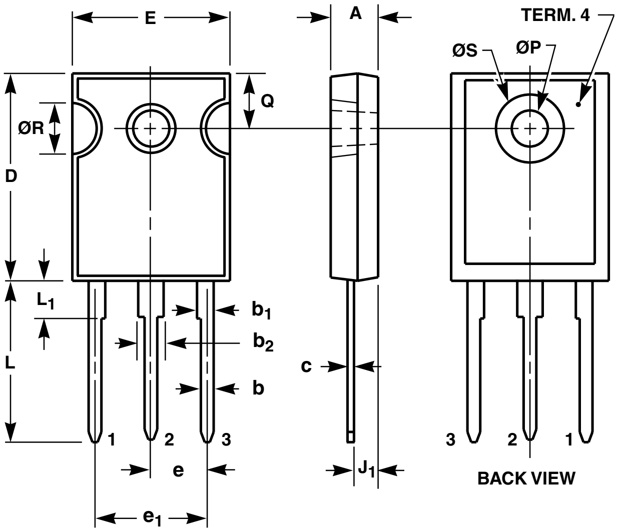
f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 27. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 27. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

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CoolFET™	GlobalOptoisolator™	PowerTrench ®	SuperSOT™-8
CROSSVOLT™	GTO™	QFET™	SyncFET™
DenseTrench™	HiSeC™	QS™	TinyLogic™
DOME™	ISOPLANAR™	QT Optoelectronics™	UHC™
EcoSPARK™	LittleFET™	Quiet Series™	UltraFET ®
E^2CMOS™	MicroFET™	SILENT SWITCHER ®	VCX™
EnSigna™	MICROWIRE™	SMART START™	
FACT™	OPTOLOGIC™	Star* Power™	
FACT Quiet Series™	OPTOPLANAR™	Stealth™	

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LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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